PD - 93863A

International
IOR Rectifier

RADIATION HARDENED POWER MOSFET SURFACE MOUNT(LCC-18)

IRHE57Z30
30V, N-CHANNEL
R5™ TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHE57Z30	100K Rads (Si)	0.07Ω	12A
IRHE53Z30	300K Rads (Si)	0.07Ω	12A
IRHE54Z30	600K Rads (Si)	0.07Ω	12A
IRHE58Z30	1000K Rads (Si)	0.07Ω	12A


LCC-18

International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm²)). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:
- Single Event Effect (SEE) Hardened
- Low $R_{DS(on)}$
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Surface Mount
- Light Weight

Absolute Maximum Ratings　　　　Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	12	
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	8.0	A
I_{DM}	Pulsed Drain Current ①	48	
P_D @ T_C = 25°C	Max. Power Dissipation	25	W
	Linear Derating Factor	0.2	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	350	mJ
I_{AR}	Avalanche Current ①	12	A
E_{AR}	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	2.3	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	0.42 (Typical)	g

For footnotes refer to the last page

12/08/00

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.025	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.07	Ω	V_{GS} = 12V, I_D = 8.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	8.0	—	—	S (℧)	V_{DS} > 15V, I_{DS} = 8.0A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS}= 24V ,V_{GS}=0V
		—	—	25		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	65	nC	V_{GS} =12V, I_D = 12A V_{DS} = 15V
Q_{gs}	Gate-to-Source Charge	—	—	20		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	10		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = 15V, I_D = 12A V_{GS} =12V, R_G = 7.5Ω
t_r	Rise Time	—	—	100		
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		
t_f	Fall Time	—	—	30		
$L_S + L_D$	Total Inductance	—	6.1	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	2184	—	pF	V_{GS} = 0V, V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	940	—		
C_{rss}	Reverse Transfer Capacitance	—	35	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	12	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	48		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	T_j = 25°C, I_S = 12A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	102	ns	T_j = 25°C, I_F = 12A, di/dt ≥100A/µs V_{DD} ≤ 25V ④
Q_{RR}	Reverse Recovery Charge	—	—	196	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	5.0	°C/W	
R_{thJPCB}	Junction-to-PC Board	—	19	—		Solder to a copper clad PC Board

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 600K Rads(Si)[1]		1000K Rads (Si)[2]		Units	Test Conditions
		Min	Max	Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	30	—	30	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.5	4.0		$V_{GS} = V_{DS}$, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V_{GS} = -20 V
I_{DSS}	Zero Gate Voltage Drain Current	—	10	—	10	µA	V_{DS}= 24V, V_{GS} =0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.024	—	0.042	Ω	V_{GS} =12V, I_D =8.0A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (LCC-18)	—	0.07	—	0.088	Ω	V_{GS} =12V, I_D =8.0A
V_{SD}	Diode Forward Voltage ④	—	1.8	—	1.8	V	V_{GS} = 0V, I_S =12A

1. Part numbers IRHE57Z30, IRHE53Z30 and IRHE54Z30
2. Part number IRHE58Z30

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V) @V_{GS}=0V	@V_{GS}=-5V	@V_{GS}=-10V	@V_{GS}=-15V	@V_{GS}=-20V
Br	37.9	255	33.4	30	30	30	25	20
I	59.4	290	28.8	25	25	20	15	10
Au	80.3	313	26.5	22.5	22.5	15	10	—

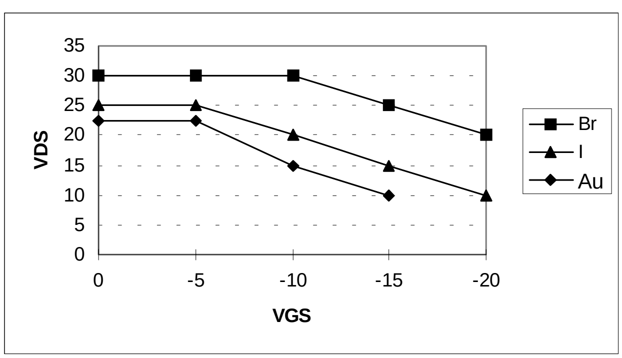


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

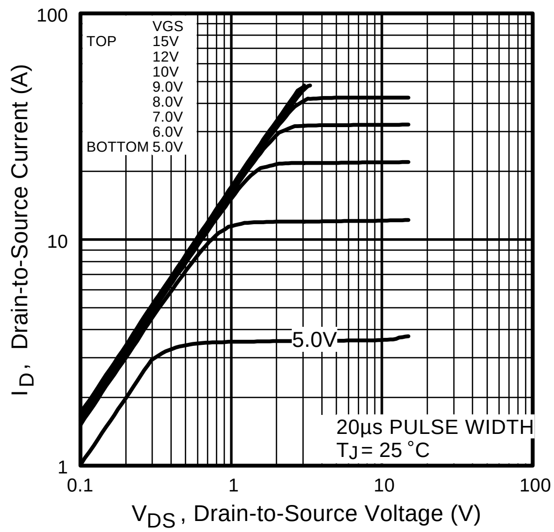


Fig 1. Typical Output Characteristics

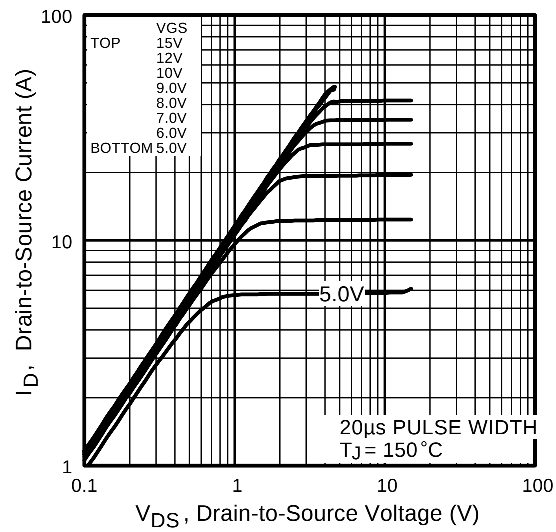


Fig 2. Typical Output Characteristics

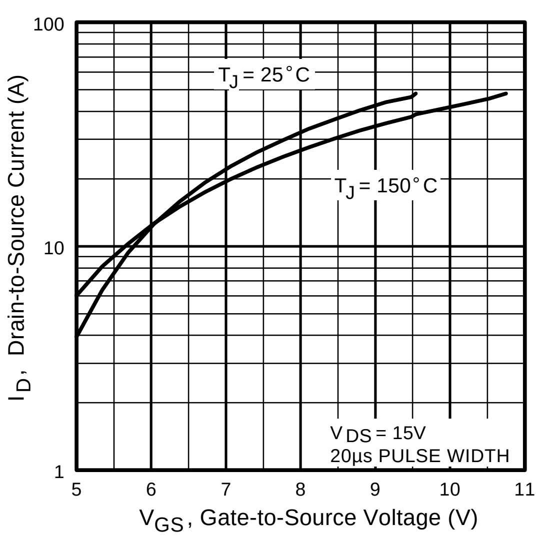


Fig 3. Typical Transfer Characteristics

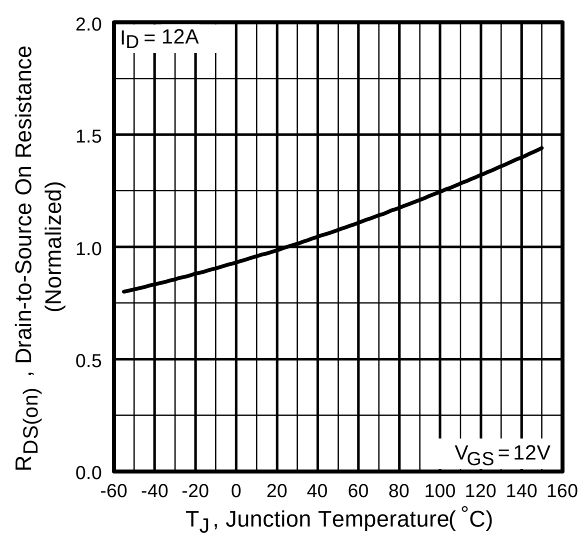


Fig 4. Normalized On-Resistance Vs. Temperature

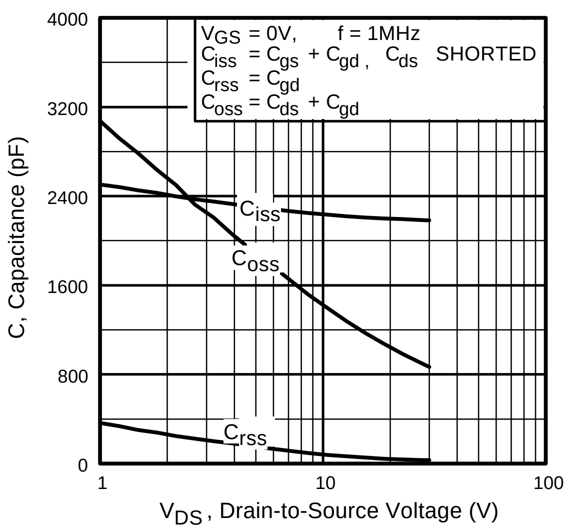


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

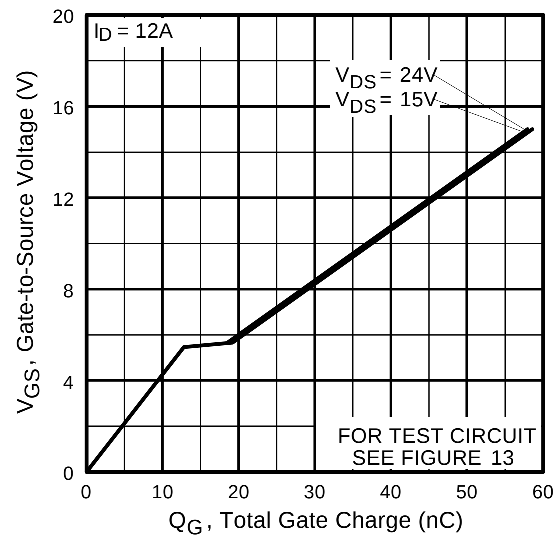


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

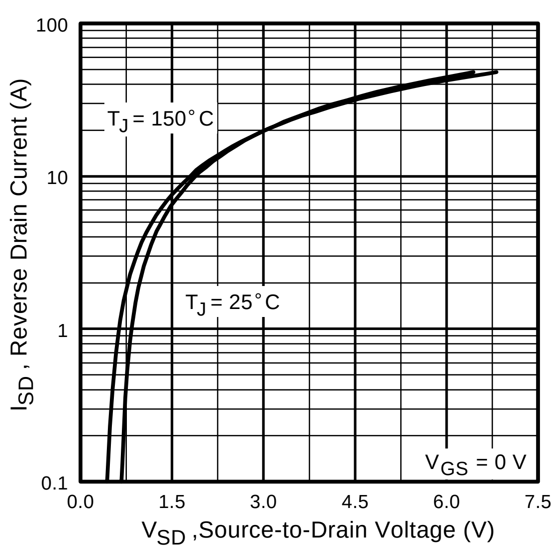


Fig 7. Typical Source-Drain Diode Forward Voltage

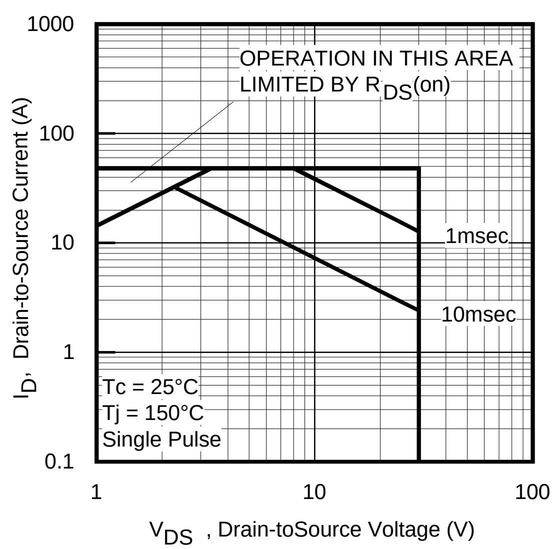


Fig 8. Maximum Safe Operating Area

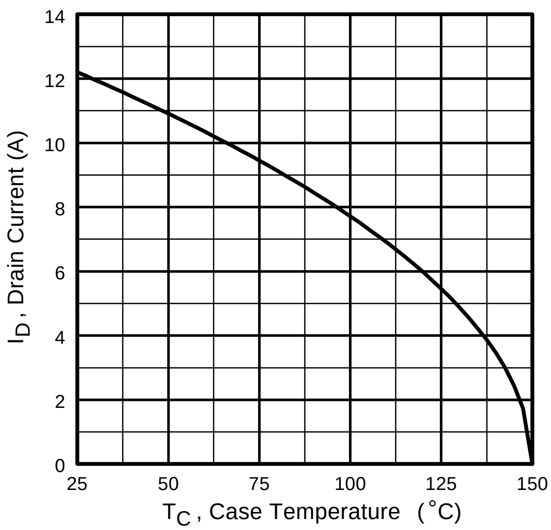


Fig 9. Maximum Drain Current Vs. Case Temperature

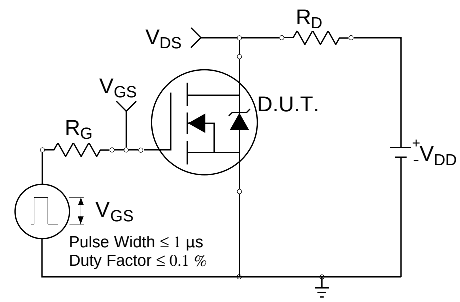


Fig 10a. Switching Time Test Circuit

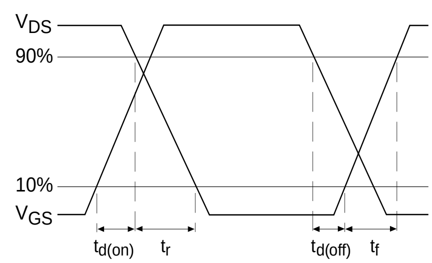


Fig 10b. Switching Time Waveforms

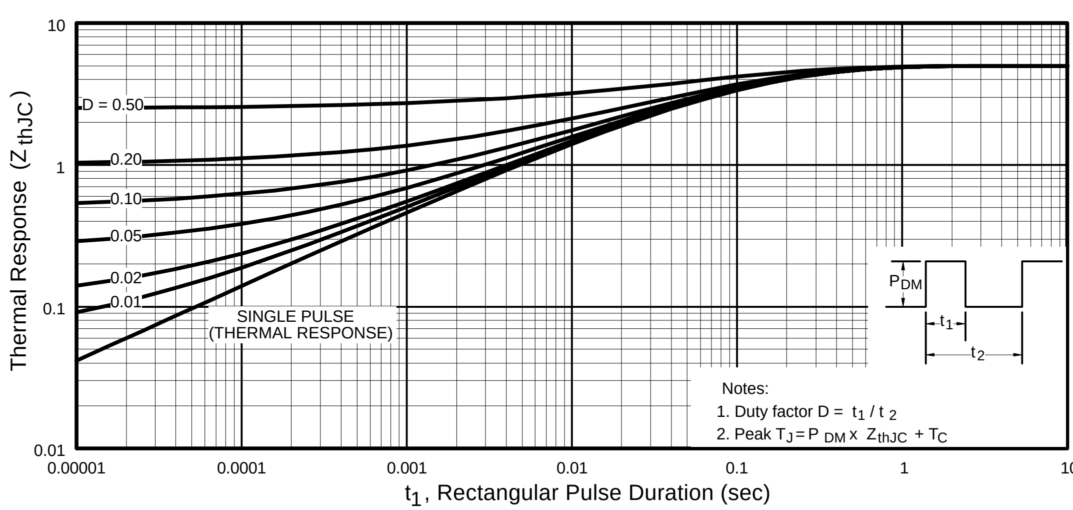


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

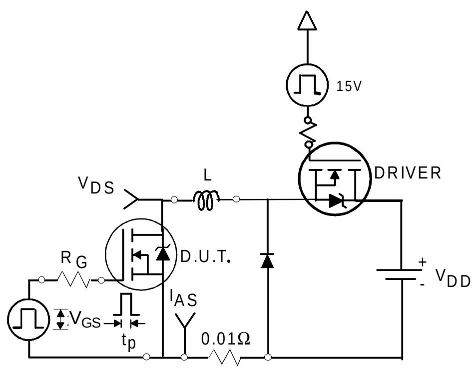


Fig 12a. Unclamped Inductive Test Circuit

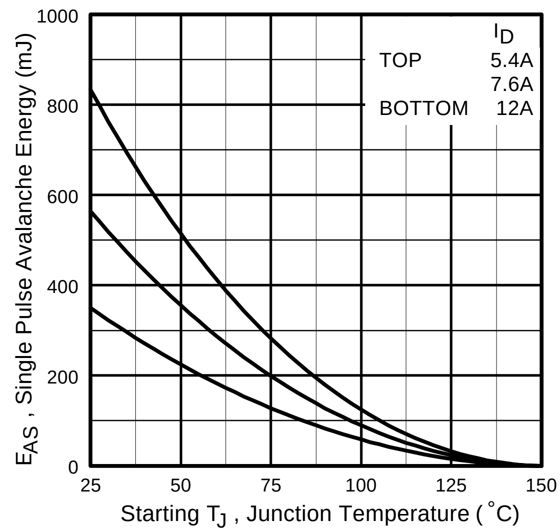


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

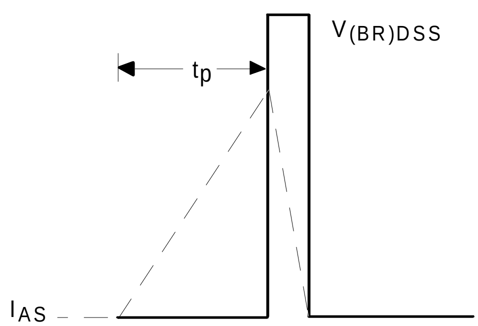


Fig 12b. Unclamped Inductive Waveforms

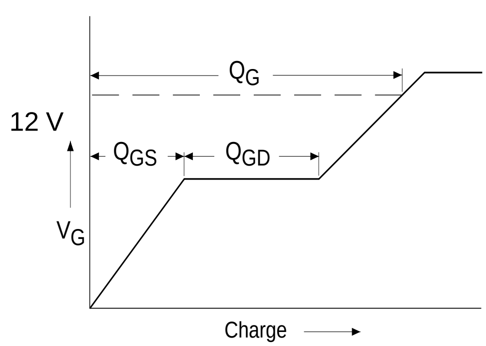


Fig 13a. Basic Gate Charge Waveform

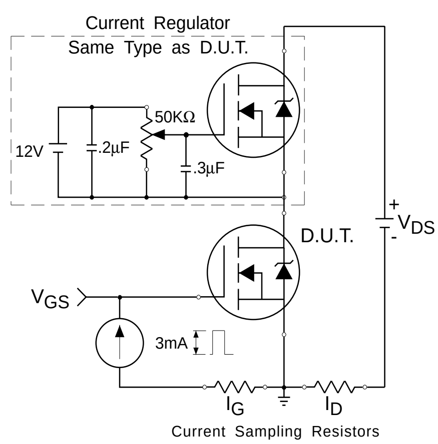


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 20V, starting T_J = 25°C, L= 4.9mH Peak I_L = 12A, V_{GS} = 12V

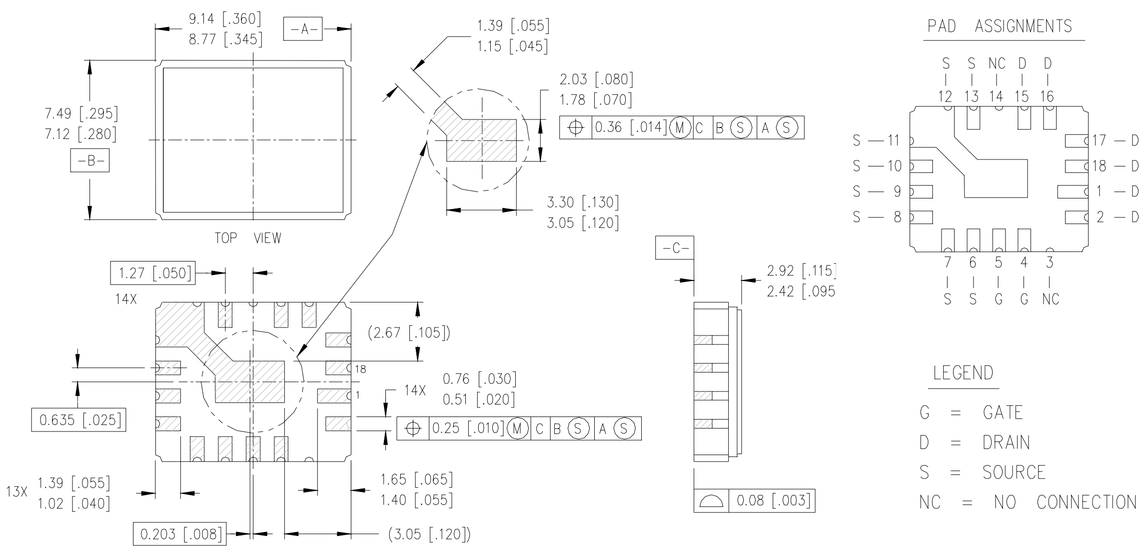
③ $I_{SD} \le$ 12A, di/dt $\le$ 110A/µs, $V_{DD} \le$ 30V, $T_J \le$ 150°C

④ Pulse width $\le$ 300 µs; Duty Cycle $\le$ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** 24 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — LCC-18



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

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Data and specifications subject to change without notice. 12/00