

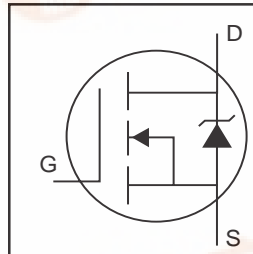
International IR Rectifier

PD- 91842

IRLBA1304/P

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Ultra Low On-Resistance
- Same outline as TO-220
- 50% greater current in typ. application conditions vs. TO-220
- Fully Avalanche Rated

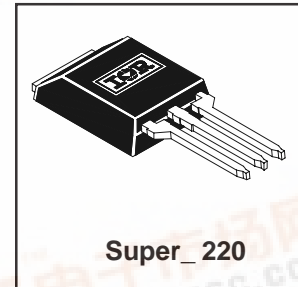


$V_{DSS} = 40V$
$R_{DS(on)} = 0.004\Omega$
$I_D = 185A$ ⑤

Description

The HEXFET® is the most popular power MOSFET in the world.

This particular HEXFET® is in the Super220™ and has the same outline and pinout as the industry standard TO-220. It has increased current handling capability over both the TO-220 and the much larger TO-247 package. This makes it ideal to reduce component count in multiparalleled TO-220 applications, reduce system power dissipation, upgrade existing designs or have TO-247 performance in a TO-220 outline. This package has also been designed to meet automotive qualification standard Q101.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	185, pkg limited to 95A*	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	130, pkg limited to 95A*	
I_{DM}	Pulsed Drain Current ①	740	
$P_D @ T_C = 25^\circ C$	Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②	1160	mJ
I_{AR}	Avalanche Current①	100	A
E_{AR}	Repetitive Avalanche Energy①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Recommended clip force	20	N

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient	—	58	

* Current capability in normal application, see Fig.9.



Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.043	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.0040	Ω	$V_{GS} = 10V, I_D = 110A$ ④
		—	—	0.0065		$V_{GS} = 4.5V, I_D = 93$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	120	—	—	S	$V_{DS} = 25V, I_D = 110A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 32V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -16V$
Q_g	Total Gate Charge	—	—	140	nC	$I_D = 110A$
Q_{gs}	Gate-to-Source Charge	—	—	39		$V_{DS} = 32V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	79		$V_{GS} = 4.5V$, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	21	—		$V_{DD} = 20V$
t_r	Rise Time	—	350	—		$I_D = 110A$
$t_{d(off)}$	Turn-Off Delay Time	—	45	—		$R_G = 0.9\Omega$
t_f	Fall Time	—	103	—		$R_D = 0.18\Omega$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	2.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	5.0	—		
C_{iss}	Input Capacitance	—	7660	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	2150	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	460	—		$f = 1.0\text{MHz}$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	185*	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	740		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 110A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	100	150	ns	$T_J = 25^\circ\text{C}, I_F = 110A$
Q_{rr}	Reverse Recovery Charge	—	250	380	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25^\circ\text{C}$, $L = 230\mu H$
 $R_G = 25\Omega$, $I_{AS} = 100A$. (See Figure 12)

③ $I_{SD} \leq 110A$, $di/dt \leq 170A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

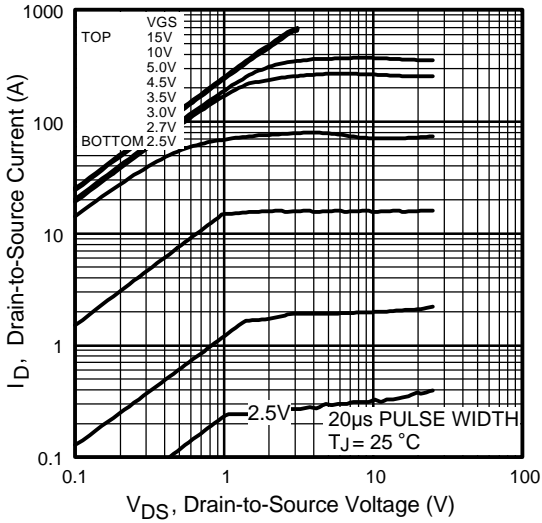


Fig 1. Typical Output Characteristics

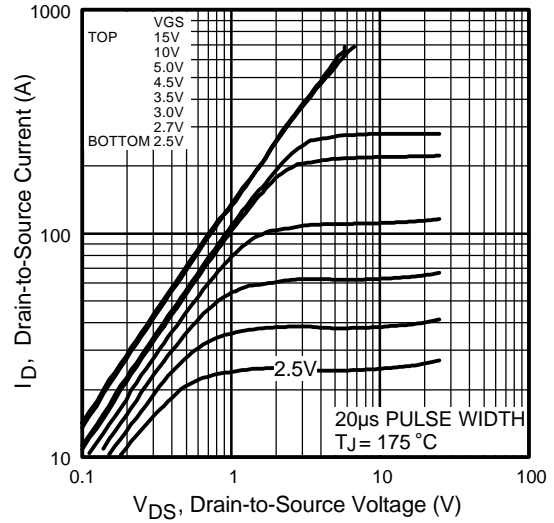


Fig 2. Typical Output Characteristics

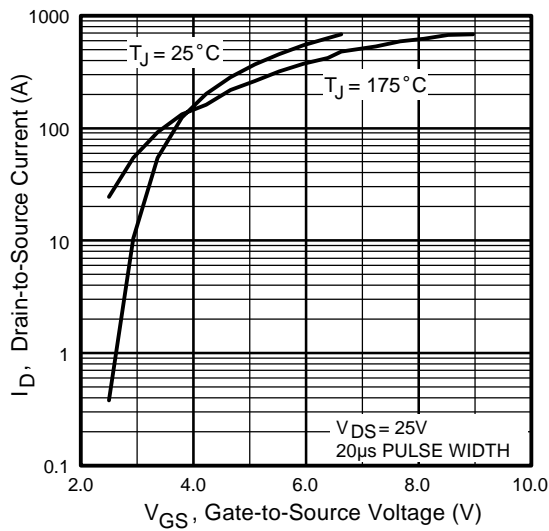


Fig 3. Typical Transfer Characteristics

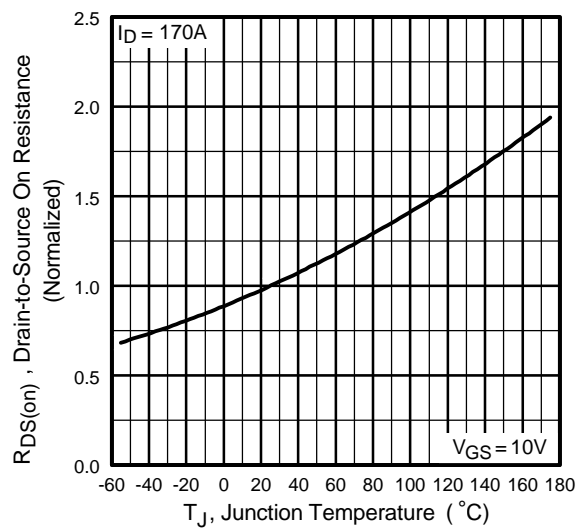


Fig 4. Normalized On-Resistance Vs. Temperature

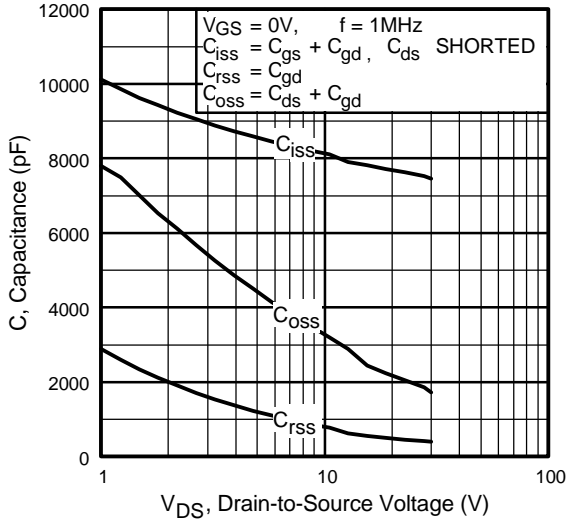


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

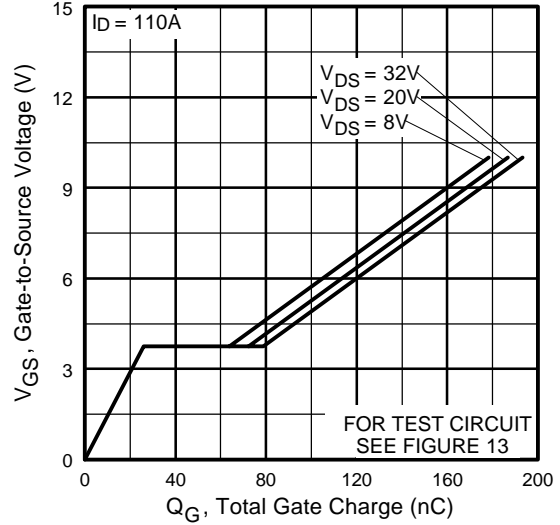


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

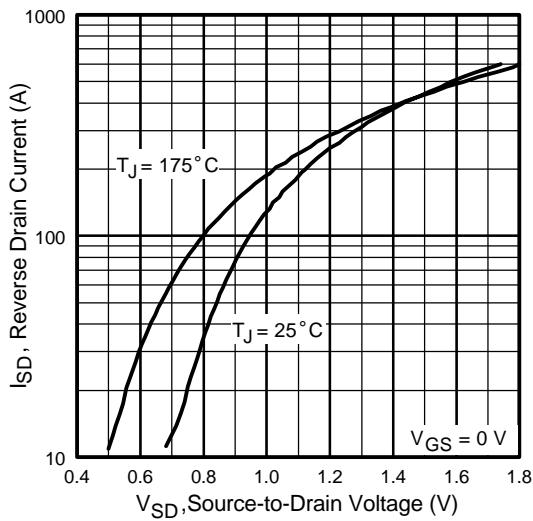


Fig 7. Typical Source-Drain Diode Forward Voltage

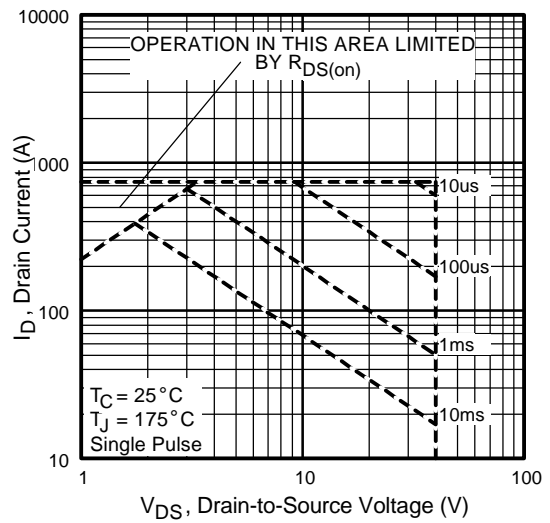


Fig 8. Maximum Safe Operating Area

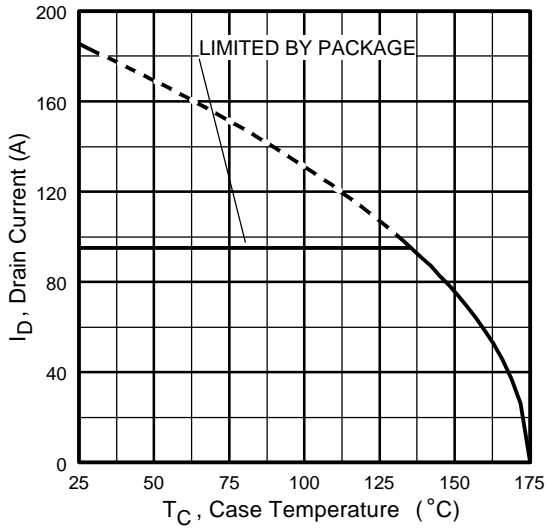


Fig 9. Maximum Drain Current Vs. Case Temperature

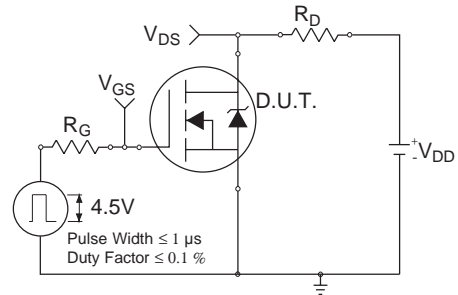


Fig 10a. Switching Time Test Circuit

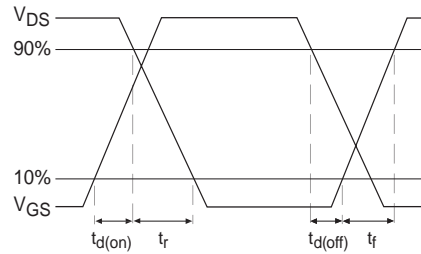


Fig 10b. Switching Time Waveforms

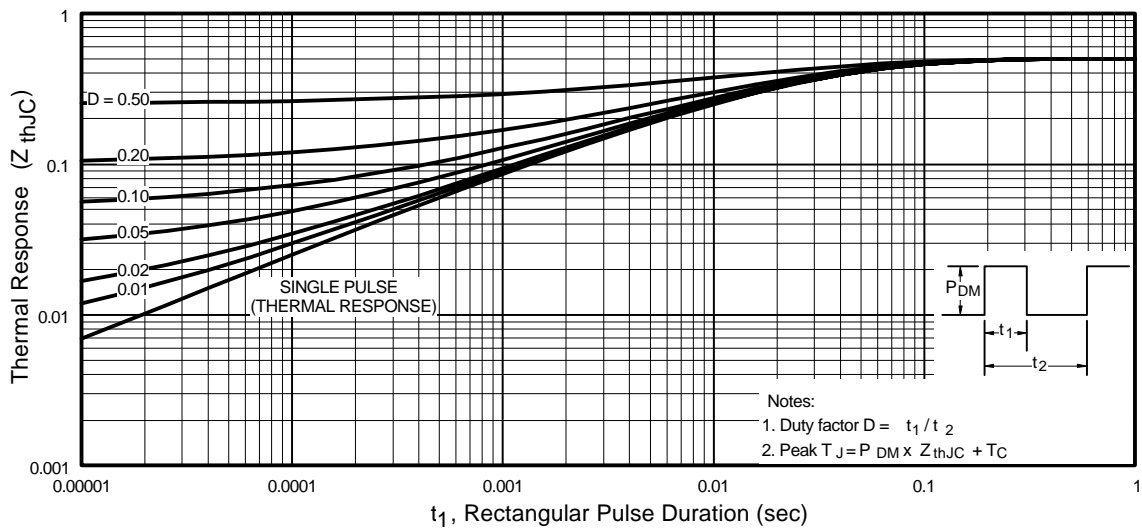


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

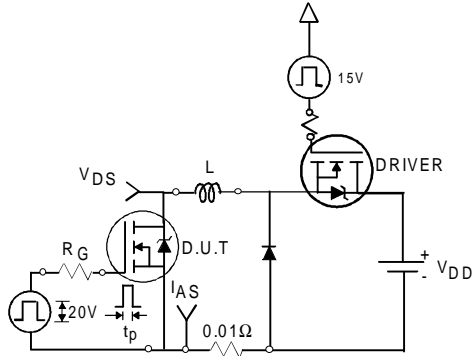


Fig 12a. Unclamped Inductive Test Circuit

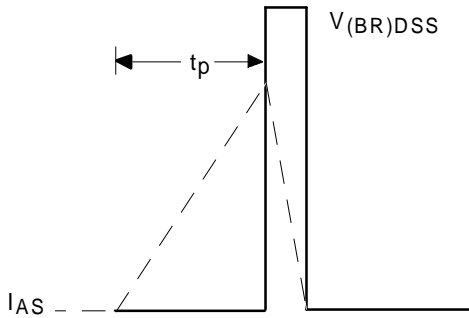


Fig 12b. Unclamped Inductive Waveforms

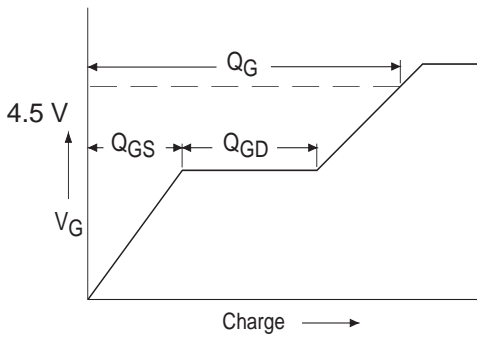


Fig 13a. Basic Gate Charge Waveform

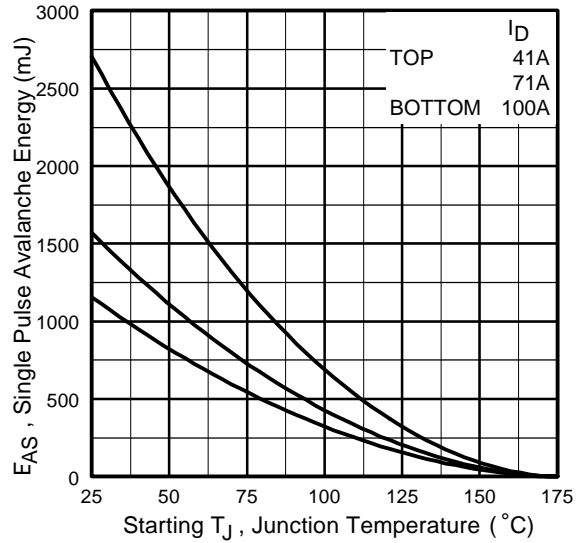


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

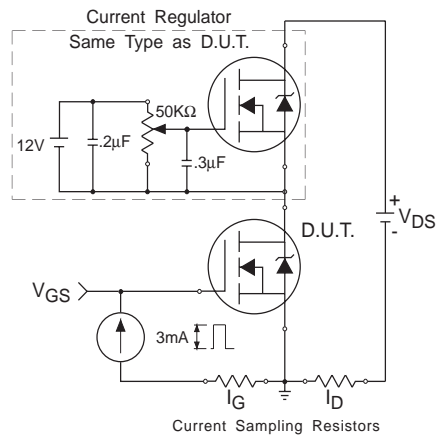
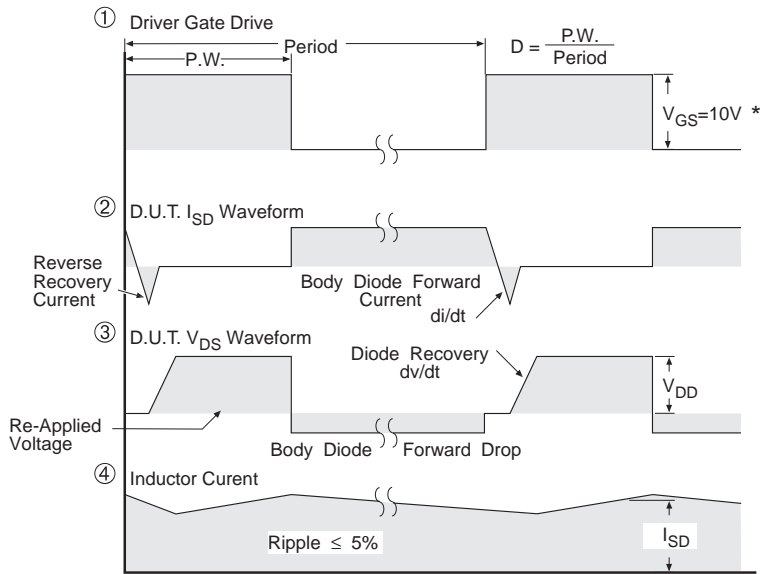
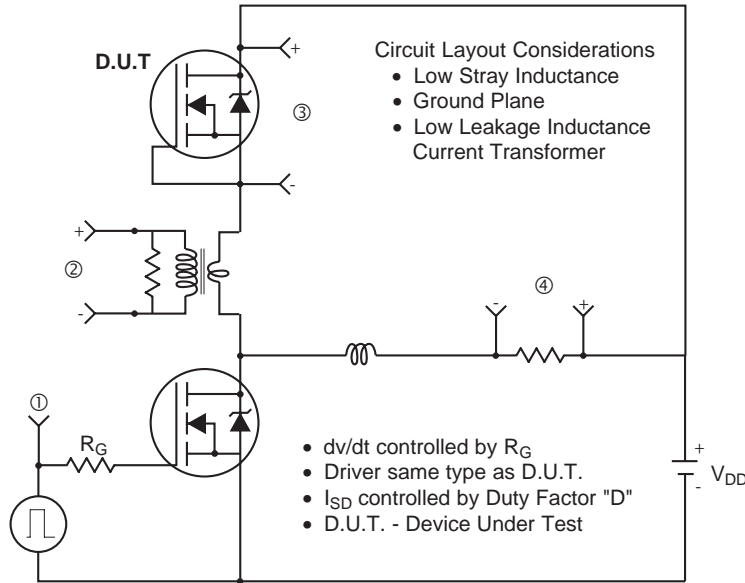


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



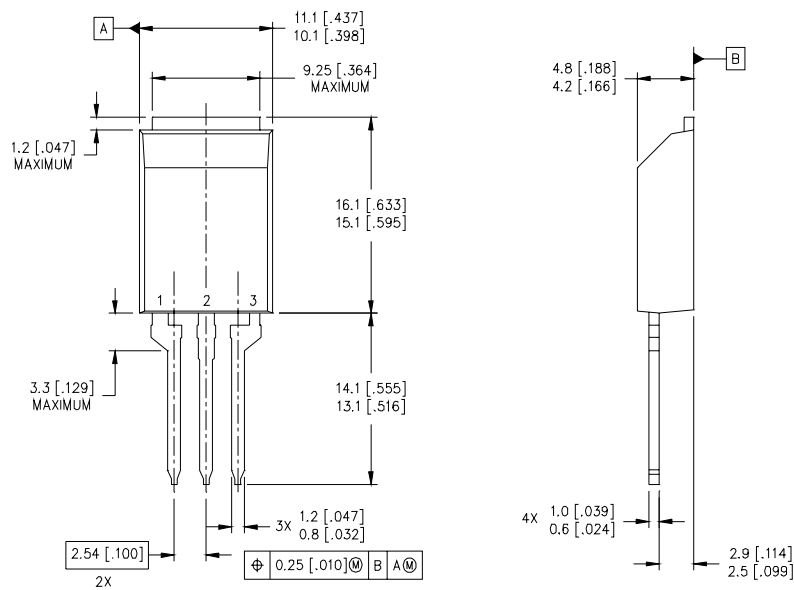
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

IRLBA1304/P

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Super_220 Package Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

IR GREAT BRITAIN: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 15 Lincoln Court, Brampton, Ontario L6T3Z2, Tel: (905) 453 2200

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

IR SOUTHEAST ASIA: 1 Kim Seng Promenade, Great World City West Tower, 13-11, Singapore 237994 Tel: ++ 65 838 4630

IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673, Taiwan Tel: 886-2-2377-9936

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