Ordering number:EN3188

PNP Epitaxial Planar Silicon Transistor
NPN Triple Diffuesd Planar Silicon Transistor

2SA1740/2SC4548

High-Voltage Driver Applications

Features

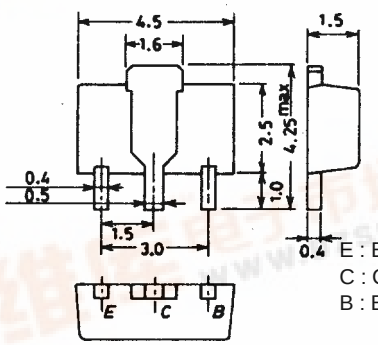
- High breakdown votlage.
- Adoption of MBIT process.
- Excellent h_{FE} linearlity.

Package Dimensions

unit:mm

2038

[2SA1740/2SC4548]



E : Emitter
C : Collector
B : Base

SANYO : PCP
(Bottom view)

( ) : 2SA1740

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		(–)400	V
Collector-to-Emitter Voltage	V_{CEO}		(–)400	V
Emitter-to-Base Voltage	V_{EBO}		(–)5	V
Collector Current	I_C		(–)200	mA
Collector Current (Pulse)	I_{CP}		(–)400	mA
Collector Dissipation	P_C	Mounted on ceramic board (250mm²×0.8mm)	1.3	W
Junction Temperature	Tj		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=(–)300V, I_E=0			(–)0.1	μA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(–)4V, I_C=0			(–)0.1	μA
DC Current Gain	h_{FE}	V_{CE}=(–)10V, I_C=(–)50mA	60*		200*	
Gain-Bandwidth Product	f_T	V_{CE}=(–)30V, I_C=(–)10mA		70		MHz
Output Capacitance	C_{ob}	V_{CB}=(–)30V, f=1MHz		(5)4		pF
Reverse Transfer Capacitance	C_{re}	V_{CB}=(–)30V, f=1MHz		(4)3		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=(–)50mA, I_B=(–)5mA		(–)0.8		V
				0.6		V

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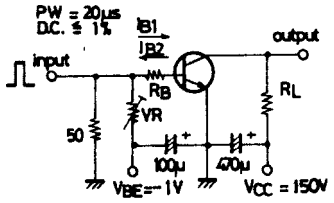
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=(–)50mA, I_B=(–)5mA			(–)1.0	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=(–)10μA, I_E=0	(–)400			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=(–)1mA, R_{BE}=∞	(–)400			V
Emiiter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=(–)10μA, I_C=0	(–)5			V
Turn-ON Time	t_{on}	See specified Test Circuit		0.25		μs
Turn-OFF Time	t_{off}	See specified Test Circuit		5.0		μs

* The 2SA1740/2SC4548 are classified by 50mA h_{FE} as follows :

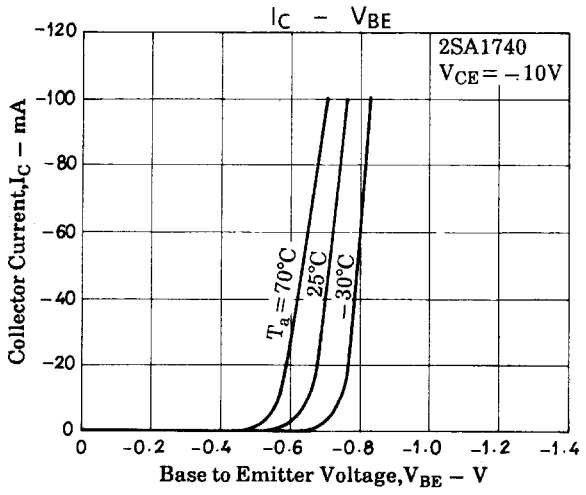
60	D	120	100	E	200

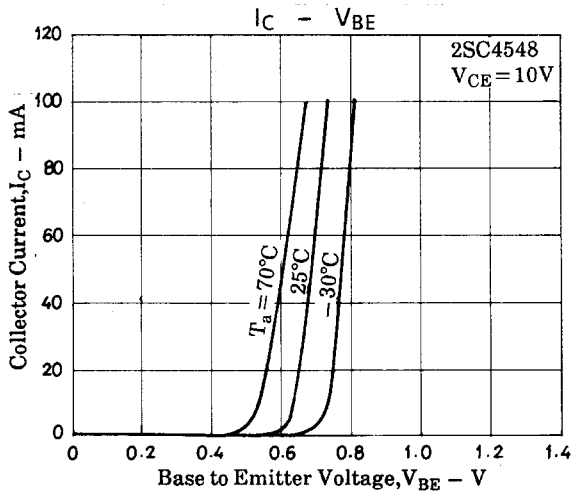
Marking 2SA1740 : AK
2SC4548 : CN
h_{FE} rank : D, E

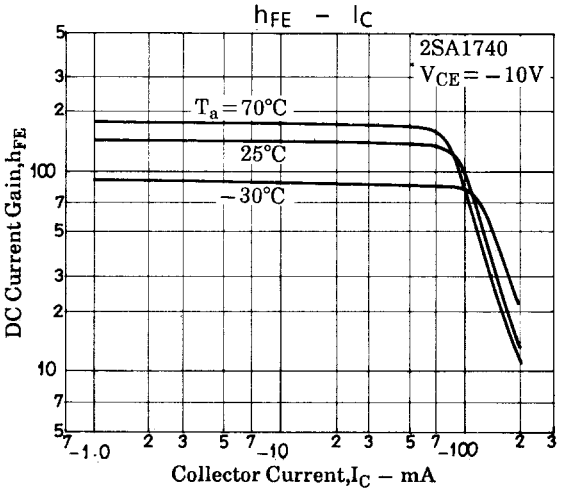
Switching Time Test Circuit

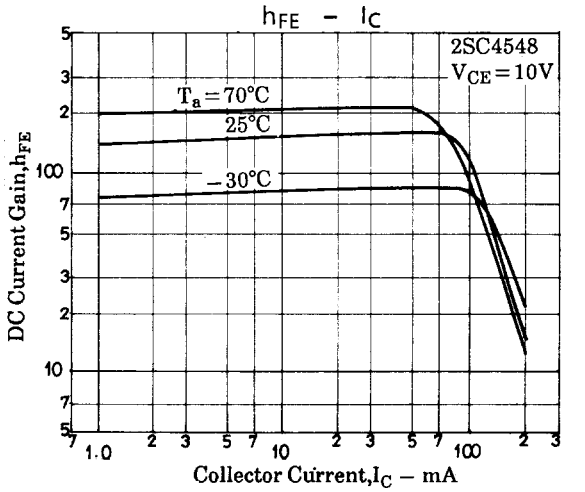


$10I_{B1} = -10I_{B2} = I_C = 50mA$
$R_L = 3k\Omega$, $R_B = 200\Omega$ at $I_C = 50mA$
For PNP, the polarity is reversed.
Unit (resistance : Ω, capacitance : F)

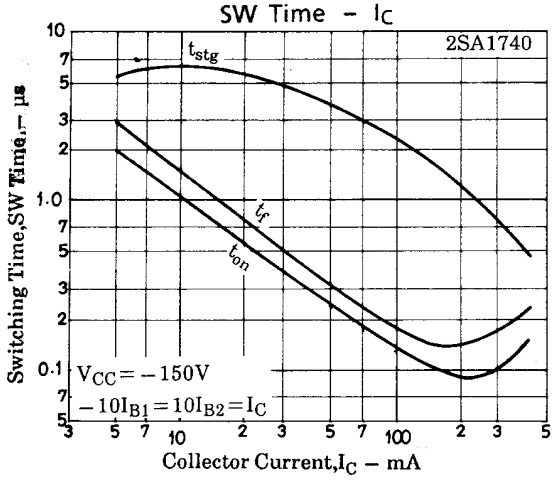




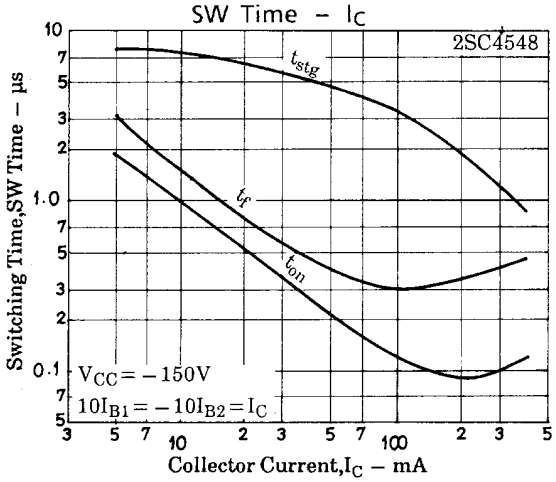




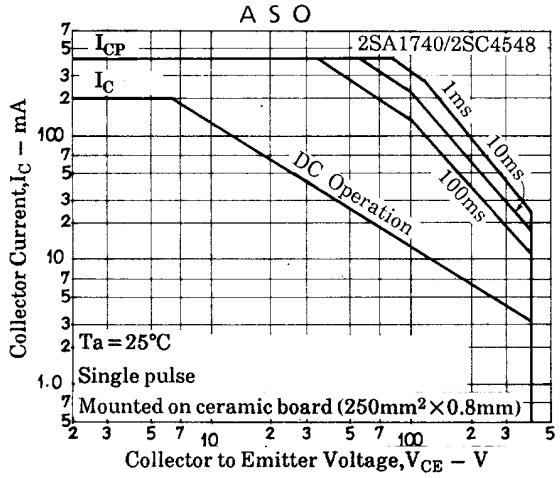
SW Time – I_C



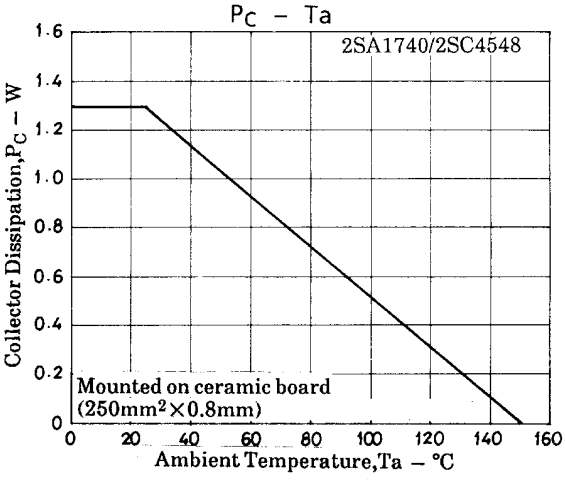
SW Time – I_C



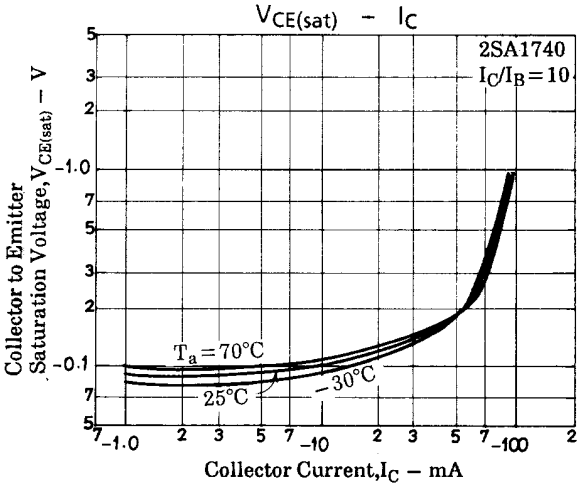
A S O



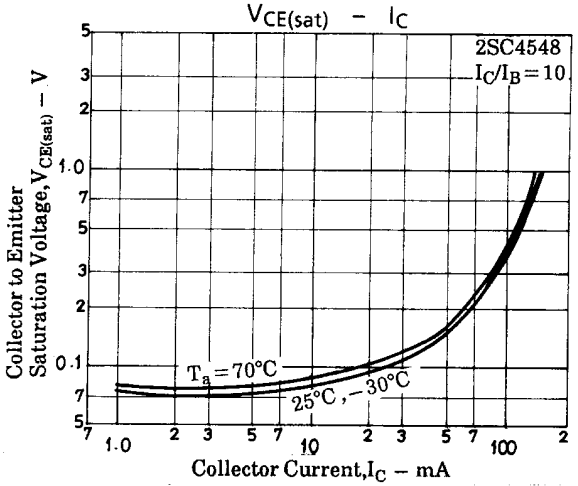
P_C – Ta



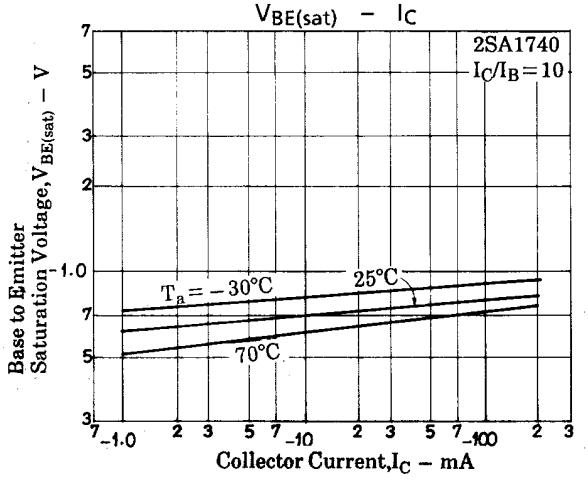
$V_{CE(sat)}$ – I_C



$V_{CE(sat)}$ – I_C



$V_{BE(sat)}$ – I_C



$V_{BE(sat)}$ – I_C