Ordering number : ENN6976A

CMOS IC

LC72151V

PLL Frequency Synthesizer for Electronic Tuning in Car Audio Systems

Overview

The LC72151V is a PLL frequency synthesizer for car audio systems. It can implement high-performance multifunction tuners such as RDS tuners and features a fast locking circuit.

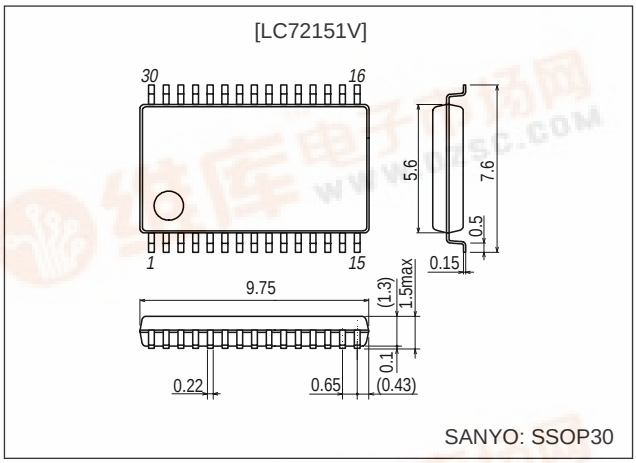
Functions

- High-speed programmable divider
  - — FMIN: 10 to 160 MHz: Pulse swallower type
  - — AMIN: 2 to 40 MHz: Pulse swallower type
    0.5 to 10 MHz: Direct division type
- IF counter
  - — HCTR: 0.4 to 25 MHz: for FM IF count
  - — LCTR: 10 to 500 kHz: for AM IF count
    1.0 to 20×10^3 Hz: for frequency measurement
- Reference frequency
  - — One of 11 frequencies may be selected (when a 10.25 or 10.35 MHz crystal is used)
    50, 30*, 25, 12.5, 10, 9*, 6.25, 5, 3.125, 3*, 1 kHz
    Note: Cannot be used when a 10.25 MHz crystal is used
- Phase comparator
  - — Supports dead band control
  - — Built-in unlock detection circuit
  - — Built-in deadlock clearing circuit
- Built-in amplifier for forming an active low-pass filter
  - — Built-in operational amplifier for FM high-speed locking
  - — Built-in MOS transistor for AM tuning
- Built-in crystal oscillator output buffer
- I/O ports — General-purpose I/O: 2 pins
  - — Four input ports (maximum)
  - — Three output ports (maximum)
- Serial data I/O
  - — Supports communication with the controller in the CCB format.
- Operating ranges
  - — Supply voltage: 4.5 to 5.5 V (V_{DD})
    7.5 to 9.5 V (AV_{DD})
  - — Operating temperature: –40 to +85°C
- Package
  - — SSOP30

Package Dimensions

unit: mm

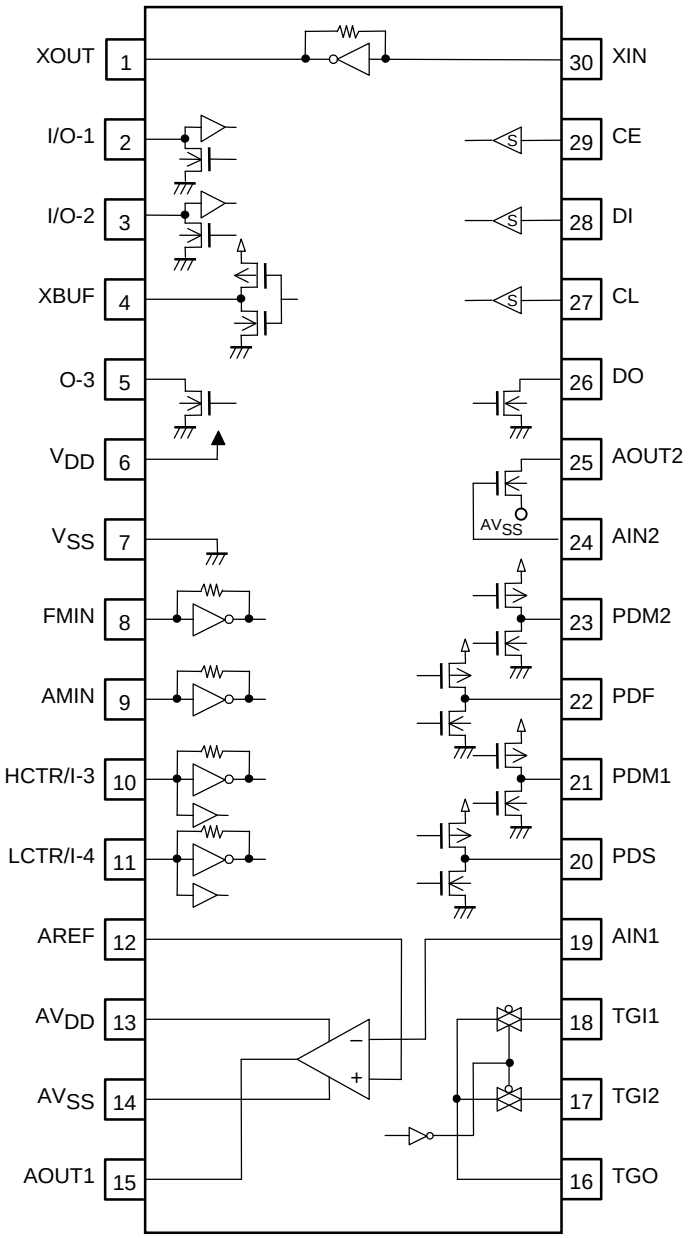
3191A-SSOP30



- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

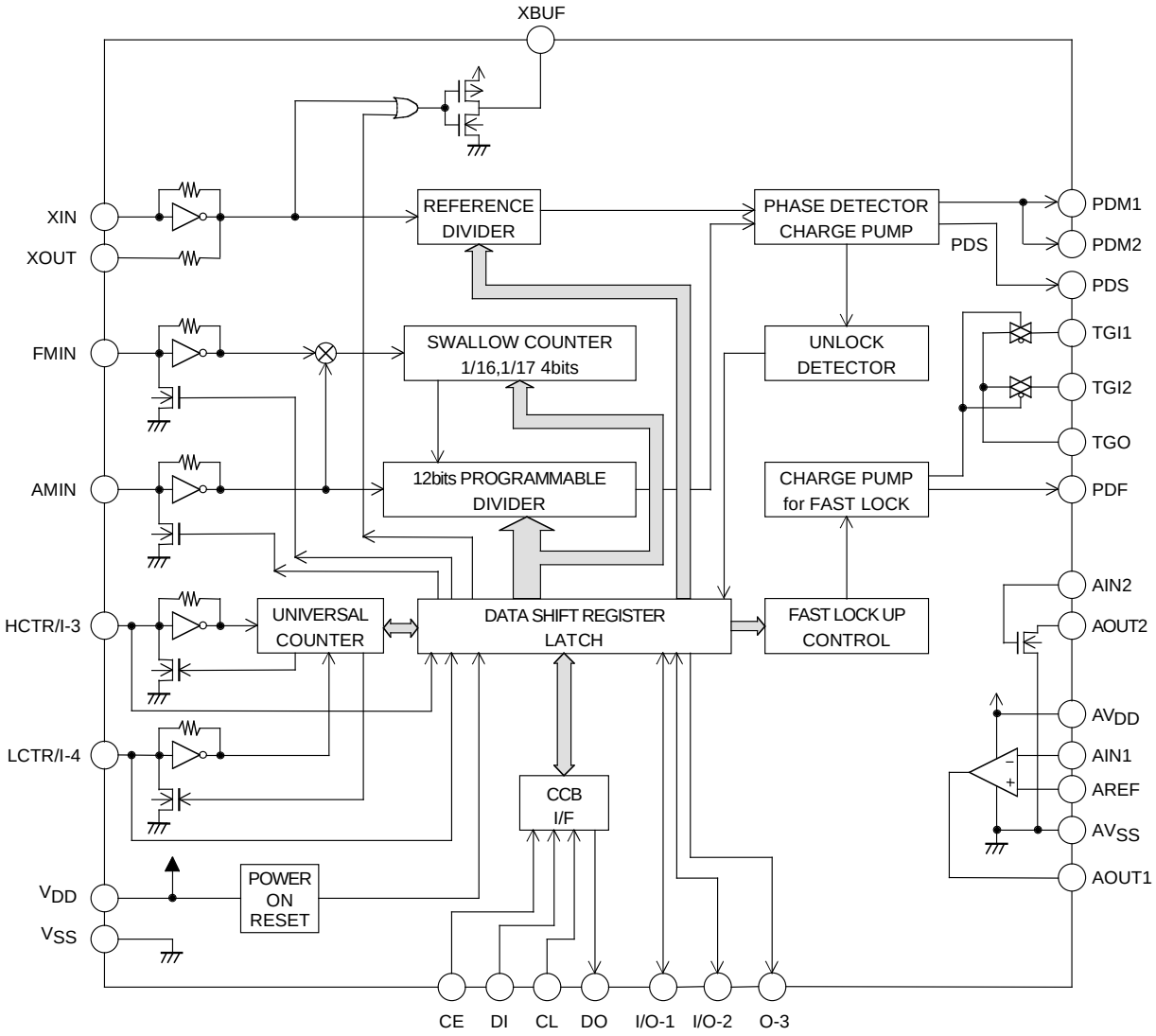
Pin Assignment

LC72151V



(Top view)

Block Diagram



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = AV_{SS} = 0 V

Parameter	Symbol	Pin	Ratings	Unit
Supply voltage	V_{DD} max	V_{DD} *	–0.3 to +6.5	V
		AV_{DD} *	–0.3 to +11.0	
Maximum input voltage	$V_{IN}1$ max	CE, CL, DI	–0.3 to +7.0	V
	$V_{IN}2$ max	XIN, FMIN, AMIN, HCTR/I-3, LCTR/I-4, AIN2, TGI1, TGI2, TGO	–0.3 to V_{DD} + 0.3	
	$V_{IN}3$ max	I/O-1, I/O-2	–0.3 to +15.0	
	$V_{IN}4$ max	AIN1, AREF	–0.3 to +6.5	
Maximum output voltage	V_O1 max	DO	–0.3 to +7.0	V
	V_O2 max	XOUT, PDM1, PDM2, PDS, PDF, XBUF, TGI1, TGI2, TGO	–0.3 to V_{DD} + 0.3	
	V_O3 max	I/O-1, I/O-2, O-3, AOUT2	–0.3 to +15.0	
	V_O4 max	AOUT1	–0.3 to +11.0	
Maximum output current	I_O1 max	I/O-1, I/O-2, O-3	0 to 10.0	mA
	I_O2 max	DO, TGI1, TGI2, TGO, AOUT1, AOUT2	0 to 5.0	
	I_O3 max	XBUF	0 to 3.0	
Allowable power dissipation	Pd max	(Ta ≤ 85°C)	SSOP30 :160	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–55 to +125	°C

Note: Power must be applied to AV_{DD} before applying to V_{DD} and AV_{DD} must be higher than or equal to V_{DD}.
Capacitors of at least 0.1 µF must be inserted between the V_{DD} and V_{SS}, and between the AV_{DD} and AV_{SS} power supply pins.

Allowable Operating Ranges at Ta = –40 to 85°C, V_{SS} = AV_{SS} = 0 V

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Supply voltage	$V_{DD}1$	V_{DD}	$V_{DD} \le AV_{DD}$	4.5		5.5	V
	$V_{DD}2$	AV_{DD}	$V_{DD} \le AV_{DD}$	7.5	8.5	9.5	
	$V_{DD}3$	V_{DD}	Serial data retention voltage	2.0			
High-level input voltage	$V_{IH}1$	CE, CL, DI		0.7V_{DD}		6.5	V
	$V_{IH}2$	I/O-1, I/O-2		0.7V_{DD}		13	
	$V_{IH}3$	HCTR/I-3, LCTR/I-4		0.7V_{DD}		V_{DD}	
Low-level input voltage	$V_{IL}1$	CE, CL, DI, I/O-1, I/O-2, LCTR/I-4		0		0.3V_{DD}	V
	$V_{IL}2$	HCTR/I-3		0		0.2V_{DD}	
Output voltage	V_O1	DO		0		6.5	V
	V_O2	AOUT1		0		9.5	
	V_O3	I/O-1, I/O-2, O-3, AOUT2		0		13	
Input frequency	$f_{IN}1$	XIN	$V_{IN}1$ *1	7		11	MHz
	$f_{IN}2$	FMIN	$V_{IN}2$ *1	10		160	
	$f_{IN}3$	AMIN (SNS=1)	$V_{IN}3$ *1	2		40	
	$f_{IN}4$	AMIN (SNS=0)	$V_{IN}4$ *1	0.5		10	
	$f_{IN}5$	HCTR/I-3	$V_{IN}5$ *1	0.4		25	
	$f_{IN}6$	LCTR/I-4	$V_{IN}6$ *1	10		500	kHz
	$f_{IN}7$	LCTR/I-4	$V_{IN}7$ *2	1.0		20×10^3	Hz

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Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Input amplitude	$V_{IN}1$	XIN	$f_{IN}1$	200		1500	mVrms
	$V_{IN}2$-1	FMIN	f = 10 to 50 MHz	40		1500	
	$V_{IN}2$-2	FMIN	f = 50 to 130 MHz	20		1500	
	$V_{IN}2$-3	FMIN	f = 130 to 160 MHz	40		1500	
	$V_{IN}3$	AMIN (SNS=1)	$f_{IN}3$	40		1500	
	$V_{IN}4$	AMIN (SNS=0)	$f_{IN}4$	40		1500	
	$V_{IN}5$-1	HCTR/I-3	f = 0.4 to 25 MHz *3	40		1500	
	$V_{IN}5$-2	HCTR/I-3	f = 8 to 12 MHz *4	70		1500	
	$V_{IN}6$-1	LCTR/I-4	f = 10 to 400 kHz *3	40		1500	
	$V_{IN}6$-2	LCTR/I-4	f = 400 to 500 kHz *3	20		1500	
	$V_{IN}6$-3	LCTR/I-4	f = 400 to 500 kHz *4	70		1500	
Guaranteed crystal oscillator frequency ranges	X'tal	XIN, XOUT	*5	10.25		10.35	MHz

Notes: 1. Sine wave with capacitor coupled.
2. Pulse wave with DC coupled.
3. Serial data: CTC = 0
4. Serial data: CTC = 1
5. Recomended CI value for the crystal oscillator: CI ≤ 70 Ω
The circuit constants for the crystal oscillator circuit depend on the crystal used, the printed circuit board pattern, and other items.
Therefore we recommend consulting with the manufacturer of the crystal for evaluation and reliability.

Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Internal feedback resistance	Rf1	XIN			1		MΩ
	Rf2	FMIN			500		kΩ
	Rf3	AMIN			500		
	Rf4	HCTR/I-3			500		
	Rf5	LCTR/I-4			500		
Internal pull-down resistance	Rpd1	FMIN		50	100	300	kΩ
	Rpd2	AMIN		50	100	300	
Hysteresis	V_{HIS}	CE, CL, DI, LCTR/I-4			0.1 V_{DD}		V
High-level output voltage	$V_{OH}1$	PDM1, PDM2, PDS, PDF	I_O = – 1 mA	V_{DD} – 1.0			V
			I_O = – 2 mA	V_{DD} – 2.0			
	$V_{OH}2$	AOUT1	I_O = – 1 mA	AV_{DD} – 1.0			
	$V_{OH}3$	XBUF	I_O = – 0.5 mA	V_{DD} – 1.5			
Low-level output voltage	$V_{OL}1$	PDM1, PDM2, PDS, PDF	I_O = 1 mA			1.0	V
			I_O = 2 mA			2.0	
	$V_{OL}2$	AOUT1	I_O = 1 mA			1.0	
	$V_{OL}3$	XBUF	I_O = 0.5 mA			1.5	
	$V_{OL}4$	I/O-1, I/O-2, O-3	I_O = 1 mA			0.2	
			I_O = 5 mA			1.0	
			I_O = 8 mA			1.6	
	$V_{OL}5$	DO	I_O =1 mA			0.2	
			I_O = 5 mA			1.0	
	$V_{OL}6$	AOUT2	I_O = 1 mA, AIN2 = 1.3 V			0.5	
High-level input current	$I_{IH}1$	CE, CL, DI	V_I = 6.5 V			5.0	μA
	$I_{IH}2$	I/O-1, I/O-2	V_I = 13 V			5.0	
	$I_{IH}3$	HCTR/I-3, LCTR/I-4	V_I = V_{DD}			5.0	
	$I_{IH}4$	XIN	V_I = V_{DD}	0.11		0.9	
	$I_{IH}5$	FMIN, AMIN, HCTR/I-3, LCTR/I-4	V_I = V_{DD}	1.8		15	
	$I_{IH}6$	AIN1, AREF	V_I = 5.5 V		0.01	100	nA
	$I_{IH}7$	TGI1, TGI2, TGO	V_I = V_{DD}			3.0	μA

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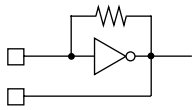
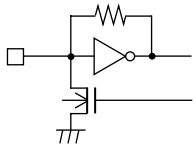
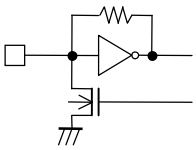
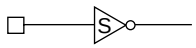
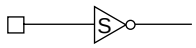
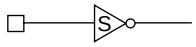
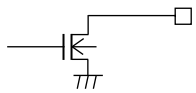
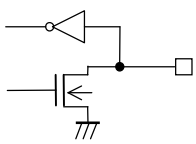
Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Low-level input current	$I_{IL}1$	CE, CL, DI	V_I = 0 V			5.0	µA
	$I_{IL}2$	I/O-1, I/O-2	V_I = 0 V			5.0	
	$I_{IL}3$	HCTR/I-3, LCTR/I-4	V_I = 0 V			5.0	
	$I_{IL}4$	XIN	V_I = 0 V	0.11		0.9	
	$I_{IL}5$	FMIN, AMIN, HCTR/I-3, LCTR/I-4	V_I = 0 V	1.8		15	
	$I_{IL}6$	AIN1, AREF	V_I = 0 V		0.01	100	nA
	$I_{IL}7$	TGI1, TGI2, TGO	V_I = 0 V			3.0	µA
Analog switch on resistance	R_{ON}	TGI1, TGI2, TGO	V_{IN} = 8.5 V, I = ±3 mA, AV_{DD} = 8.5 V		70	140	Ω
			V_{IN} = 4.5 V, I = ±3 mA, AV_{DD} = 8.5 V		50	100	
			V_{IN} = 0.5 V, I = ±3 mA, AV_{DD} = 8.5 V		70	140	
Output off leakage current	$I_{OFF}1$	AOUT1	V_O = 6.5 V			5.0	µA
	$I_{OFF}2$	I/O-1, I/O-2, O-3, AOUT2	V_O = 13 V			5.0	
	$I_{OFF}3$	DO	V_O = 6.5 V			5.0	
High-level 3-state off leakage current	I_{OFFH}	PDM1, PDM2, PDS, PDF	$V_O = V_{DD}$		0.01	200	nA
Low-level 3-state off leakage current	I_{OFFL}	PDM1, PDM2, PDS, PDF	V_O = 0 V		0.01	200	nA
Input capacitance	C_{IN}	FMIN			6		pF
Supply current	$I_{DD}1$	V_{DD}	X'tal = 10.35 MHz $f_{IN}2$ = 160 MHz $V_{IN}2$ = 40 mVrms		10	18	mA
	$I_{DD}2$	V_{DD}	PLL block stopped (PLL INHIBIT) X'tal OSC operating (X'tal = 10.35 MHz)		0.5	1.5	
	$I_{DD}3$	AV_{DD}	PLL block stopped (PLL INHIBIT) X'tal OSC stopped On-chip op-amp stopped			1.5	
	$I_{DD}4$	V_{DD}	PLL block stopped (PLL INHIBIT) X'tal OSC stopped On-chip op-amp stopped			10	µA

Pin Functions

Pin No.	Symbol	Usage	Function	Pin circuit
30 1	XIN XOUT	X'tal OSC	• Crystal oscillator connection. (10.25 or 10.35 MHz)	
8	FMIN	Local oscillator signal input	• FMIN is selected by setting DVS in the control data to 1. • Enters high-speed locking mode by setting SNS in the control data to 1. • Enters normal mode by setting SNS in the control data to 0. • Input frequency: 10 to 160 MHz • The signal is transmitted to the swallow counter. • The divisor can be set to a value in the range 272 to 65,535.	
9	AMIN	Local oscillator signal input	• AMIN is selected by setting DVS in the control data to 0. • When SNS in the control data is set to 1: Input frequency: 2 to 40 MHz The signal is directly transmitted to the swallow counter. • When SNS in the control data is set to 0: Input frequency: 0.5 to 10 MHz The signal is directly transmitted to the 12-bit programmable divider. The divisor can be set to a value in the range 5 to 4,095.	
29	CE	Chip enable	• This pin must be set to the high level when inputting serial data to the LC72151V DI pin and when outputting serial data from the DO pin.	
28	DI	Input data	• Serial data input for transferring data from the controller to the LC72151V.	
27	CL	Clock	• Data synchronization clock signal used when inputting serial data to the LC72151V DI pin and when outputting serial data from the DO pin.	
26	DO	Output data	• Serial data output for transferring data from the LC72151V to the controller.	
6	V_{DD}	Power	• LC72151V power supply. A voltage in the range 4.5 to 5.5 V must be provided when the PLL circuit is operating. • The power-on reset circuit operates when power is first applied. Note: Power must be applied to AV_{DD} before applied to V_{DD} and AV_{DD} must be higher than or equal to V_{DD}.	———
7	V_{SS}	Ground	• LC72151V ground.	———
2 3	I/O-1 I/O-2	I/O ports	• Input/output dual function pins • The function will be selected according to IOC1 and IOC2 in the control data. Data = 0: Input port 1: Output port • When specified as an input port: The input pin state is transmitted to the system microcontroller from DO pin. Input state = Low: data is 0 = High: data is 1. • When specified as an output port: The output state will be determined according to I/O-1 and I/O-2 in the control data. Data = 0: Low = 1: Open • These pin function as an input port at a power-on reset.	

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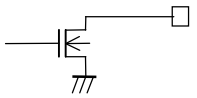
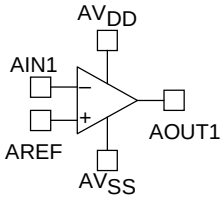
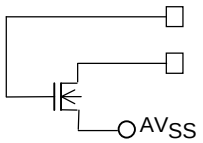
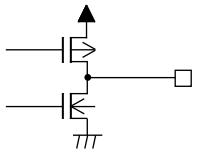
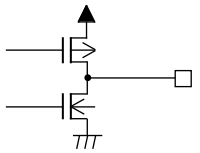
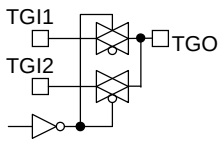
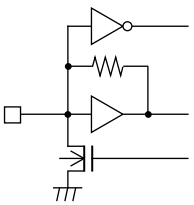
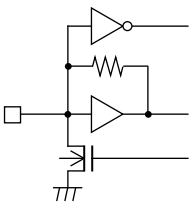
Pin No.	Symbol	Usage	Function	Pin circuit
5	O-3	Output port	• Dedicated output pin • Latches OUT3 in the control data and outputs data from O-3 pin. • This pin goes open state at a power-on reset.	
19 12 13 14 15	AIN1 AREF AV_{DD} AV_{SS} AOUT1	Op-amp for low-pass filter amp	• Op-amp for PLL active low-pass filter • AV_{SS} is the analog system ground pin shared with low-pass filter Nch MOS transistor. • Voltage applied to AREF pin must be 1/2 that to V_{DD} pin. Note: Power must be applied to AV_{DD} before applied to V_{DD}, and AV_{DD} must be higher than or equal to V_{DD}.	
24 25	AIN2 AOUT2	Transistor for low-pass filter amp	• PLL active low-pass filter Nch MOS transistor • Source of the transistor is connected to AV_{SS} pin. Note: Connect AV_{SS} pin to ground in use.	
21 23 20	PDM1 PDM2 PDS	Charge pump output	• PLL charge pump output When the frequency created by dividing the local oscillator signal frequency by N is higher than the reference frequency, a high level is output from the PD pin. When lower, a low level is output. The PD pin goes to the high-impedance state when the frequencies match.	
22	PDF	PLL high-speed locking charge pump output	• PLL high-speed locking charge pump output When the high-speed locking mode is selected, signal pulses is output according to the frequency variation. This pin enters high-impedance state when the local oscillation frequency enters the set frequency range.	
18 17 16	TGI1 TGI2 TGO	PLL high-speed locking TG	• PLL high-speed locking active low-pass filter transmission gate input/output dual function pins Note: Connect AV_{SS} pin to ground in use.	
10	HCTR/I-3	General-purpose counter	• HCTR is selected by setting CTS1 in the control data to 1. Input frequency: 0.4 to 25 MHz The signal is input to a divide-by-2 circuit and the result is input to a general-purpose counter. This counter can also be used as an integrating counter. The counter value is output as the result of the count, MSB first, from the DO pin. There are four measurement periods: 4, 8, 32, and 64 ms. • When H/I-3 in the control data is set, this pin functions as an input port, and the value is output from the output pin DO.	
11	LCTR/I-4	General-purpose counter	• LCTR is selected by setting CTS1 in the control data to 1. • When the LCTR is selected as described above and CTS0 is set to 1: This pin enters the frequency measurement mode. Input frequency: 10 to 500 kHz The signal is directly transmitted to the general-purpose counter. • When CTS0 is set to 0 This pin enters period measurement mode. Input frequency: 1 Hz to 20 kHz Period can be measured either in single period or in double period. If double period measurement is selected, the frequency is 2 Hz to 40 kHz. The counter value is output as the result of the count, MSB first, from the DO pin. • When L/I-4 in the control data is set: This pin functions as an input port, the value is output from the output pin DO.	

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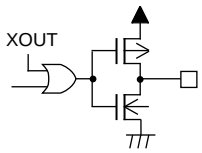
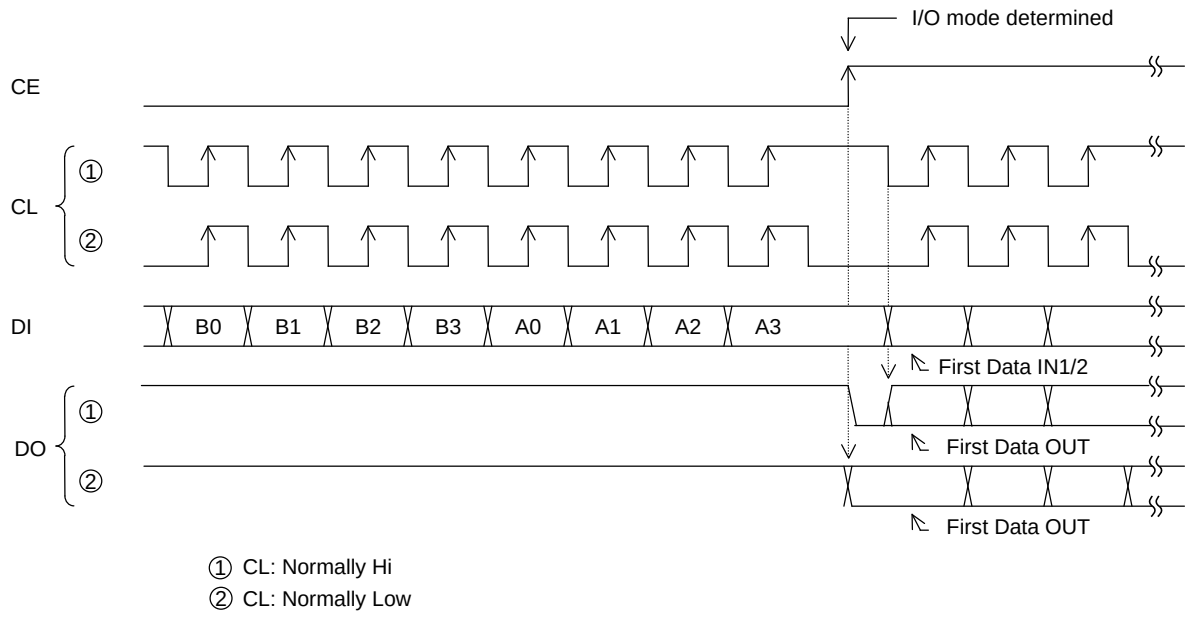
Pin No.	Symbol	Usage	Function	Pin circuit
4	XBUF	Crystal oscillator buffer	• Output buffer for the crystal oscillator circuit • When XB in the serial data is set to 1, the output buffer operates and the crystal oscillator signal (a pulse signal) is output. When XB is 0, XBUF outputs a low level. After the power-on reset, the output buffer is fixed at the low level.	

Serial Data I/O Methods

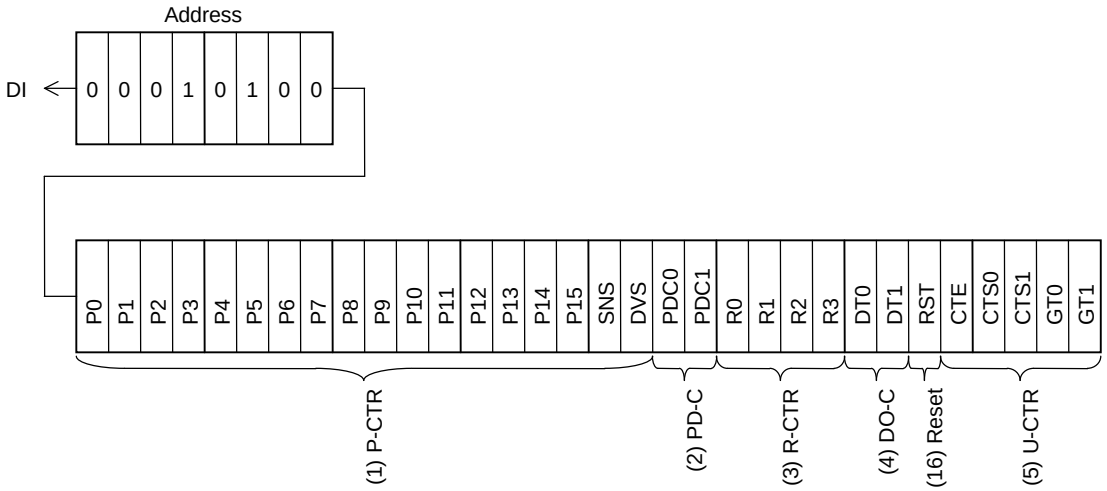
Data is input to and output from the LC72151V using the Sanyo CCB (Computer Control Bus) format, which is the serial bus format used by SANYO audio ICs. This IC adopts a CCB format with an 8-bit address.

	I/O mode	Address								Content
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1 (82)	0	0	0	1	0	1	0	0	• Control data input (serial input) mode. • 32 bits of data are input. • See the “DI Control Data (Serial Data Input) Structure” item for details on the content of the input data.
[2]	IN2 (92)	1	0	0	1	0	1	0	0	• Control data input (serial input) mode. • 32 bits of data are input. • See the “DI Control Data (Serial Data Input) Structure” item for details on the content of the input data.
[3]	OUT (A2)	0	1	0	1	0	1	0	0	• Data output (serial data output) mode. • The number of bits output is equal to the number of clock cycles. • See the “DO Output Data (Serial Data Output) Structure” item for details on the content of the output data.

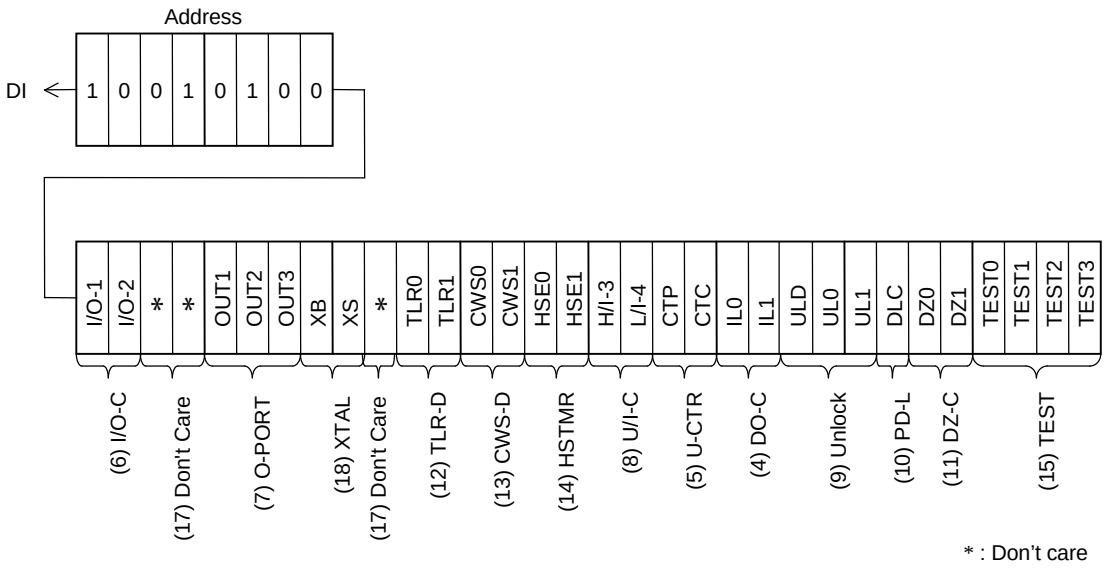


DI control data (serial data input) structure

(1) IN1 mode



(2) IN2 mode



DI control data description

<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15
DVS, SNS</td><td>
• This data sets the divisor for the programmable divider and P15 is the MSB of this binary value. LSB will change according to the DVS and SNS.
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Set divisor (N)</th></tr>
<tr><td>1</td><td>1</td><td>P0</td><td>272 to 65535</td></tr>
<tr><td>1</td><td>0</td><td>P0</td><td>272 to 65535</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td></tr>
</table>
*: When the LSB is P4, P0 to P3 are invalid.
• Used to select programmable divider signal input pins (FMIN, AMIN) and to switch the input frequency range.
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input pin frequency range</th></tr>
<tr><td>1</td><td>1</td><td>FMIN</td><td>10 to 160 MHz (High-speed mode)</td></tr>
<tr><td>1</td><td>0</td><td>FMIN</td><td>10 to 160 MHz (Normal mode)</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr>
</table>
*: When the DVS and SNS are set to 1, the high-speed locking mode is selected, the high-speed control data becomes valid.
By setting DVS to 1 and SNS to 0 this pin enters FMIN mode, the sub-charge pump control data is valid, the high-speed locking control data becomes invalid.
</td><td></td></tr>
<tr><td>(2)</td><td>Sub-charge pump control data
PDC0, PDC1</td><td>
• This data controls the sub-charge pump.
<table>
<tr><th>PDC1</th><th>PDC0</th><th>Sub-charge pump state</th></tr>
<tr><td>0</td><td>*</td><td>High impedance</td></tr>
<tr><td>1</td><td>1</td><td>Charge pump operating (at all times)</td></tr>
<tr><td>1</td><td>0</td><td>Charge pump operating (when PLL unlocked)</td></tr>
</table>
(* : don't care)
• The sub-charge pump can be used in conjunction with the PDM1 or the PDM2 pin (main charge pump pin) to form a high-speed locking circuit.
*: FMIN(High-speed mode): Setting DVS and SNS to 1 forces the sub-charge pump to operate for the time set due to the high-speed locking end flag output wait time, and allows the locking time to be reduced after switching to the normal PLL mode.
See the "Charge Pump Structure" item for details.
</td><td>HSE0
HSE1</td></tr>
<tr><td>(3)</td><td>Reference divider data
R0 to R3</td><td>
• Reference frequency selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency (kHz)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>30</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL inhibit + X'tal OSC stop</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL inhibit</td></tr>
</table>
Note: PLL inhibit (backup mode)
The programmable divider block is stopped, the FMIN and AMIN pins are pulled down to ground, and the charge pump output is set to the floating state.
</td><td></td></tr>
</table>

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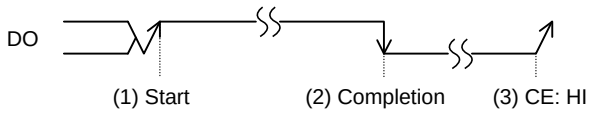
<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(4)</td><td>DO pin control data
ULD
DT0, DT1
IL0, IL1</td><td>
• Data that determines the output of the DO pin
<table>
<tr><th>ULD</th><th>DT1</th><th>DT0</th><th>DO pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Low when unlocked</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC *1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>IN *2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>end-UC *1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>IN *2</td></tr>
</table>
*Note: Open state will be selected at the power-on reset.
Note: *1. end-UC: General-purpose counter operation completion check


(1) When the count operation starts by setting end-UC with CTE set to 1 from 0, DO pin automatically goes to open state.
(2) When the general-purpose counter operation ends, the DO pin goes low, it is allowed to check the count end.
(3) DO pin goes to open state according to the serial data input/output state: CE pin = high.
Note: *2.
<table>
<tr><th>IL1</th><th>IL0</th><th>IN</th></tr>
<tr><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>I-1 (pin state)</td></tr>
<tr><td>1</td><td>0</td><td>I-2 (pin state)</td></tr>
<tr><td>1</td><td>1</td><td>DO goes low when I-1 changes.</td></tr>
</table>
However, if I/O-1 and I/O-2 are set to output mode, they change from IN to the open state.
*: DO pin state during data input (IN1, IN2 modes, CE = high) keeps open regardless of the DO pin control data.
In addition, Do pin during data input (OUT mode, CE = high) outputs the value for the internal DO serial data synchronized with the CL regardless of the DO pin control data.
Caution: Cannot be used in crystal oscillator stop mode: R0 = 0, R1 = R2 = R3 = 1 (The DO pin will not change state.)
</td><td>CTE
I/O-1
I/O-2</td></tr>
</table>

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<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(5)</td><td>General-purpose counter
control data
CTS0, CTS1
CTE
GT0, GT1
CTP
CTC</td><td>
• Selects the general-purpose counter input pins (HCTR, LCTR).
<table>
<tr><th>CTS1</th><th>CTS0</th><th>Input pin</th><th>Measurement mode</th></tr>
<tr><td>1</td><td>*</td><td>HCTR</td><td>Frequency</td></tr>
<tr><td>0</td><td>1</td><td>LCTR</td><td>Frequency</td></tr>
<tr><td>0</td><td>0</td><td>LCTR</td><td>Period</td></tr>
</table>
• General-purpose counter measurement start data
CTE = 1: Starts the counter.
CTE = 0: Resets the counter.
• Determines the measurement time (frequency mode) and number of periods (period mode).
<table>
<tr><th rowspan="3">GT1</th><th rowspan="3">GT0</th><th colspan="3">Frequency measurement</th><th rowspan="3">Period measurement mode</th></tr>
<tr><th rowspan="2">Measurement time</th><th colspan="2">Wait time</th></tr>
<tr><th>CTP = 0</th><th>CTP = 1</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td><td>1 to 2 ms</td><td>One period</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4 ms</td><td>1 to 2 ms</td><td>One period</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8 ms</td><td>1 to 2 ms</td><td>Two periods</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8 ms</td><td>1 to 2 ms</td><td>Two periods</td></tr>
</table>
• When CTE = 0, input pull-down is disabied by setting CTP to 1
Note: Wait time: 1 to 2ms.
However, CTP must be set to 1 4ms before CTE is set to 1.
• The input sensitivity is reduced when CTC is set to 1. (Sensitivity: 10 to 30 mV rms)
*: Refer to the General-purpose counter stracture on page 22 for details.
</td><td></td></tr>
<tr><td>(6)</td><td>I/O port control data
IO-1, I/O-2</td><td>
• Data that specifies the I/O direction of the I/O ports (I/O-1, I/O-2).
[Data] = 0: Input port
1: Output port
*: After the power-on reset, the I/O-1 and I/O-2 are set up as input ports.
</td><td>OUT1, OUT2</td></tr>
<tr><td>(7)</td><td>Output port data
OUT1 to OUT3</td><td>
• Data that determines the output from output ports O-1 to O-3.
[Data] = 0: Open
1: Low
*: Invalid when the corresponding port is set up as an input port.
*: At a power-on reset, open state is selected by selling the data to 0
</td><td>I/O-1, I/O-2</td></tr>
<tr><td>(8)</td><td>General-purpose counter
control data
H/I-3, L/I-4</td><td>
• Data that switch the function between general-purpose counter and input port.
H/I-3 = 0: I-3 (input port)
1: HCTR (gereal-purpose counter)
L/I-4 = 0: I-4 (input port)
1: LCTR (gereal-purpose counter)
</td><td>CTS0, CTS1</td></tr>
</table>

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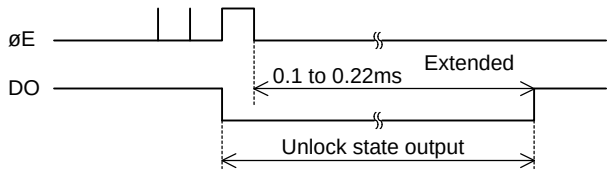
<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(9)</td><td>Unlock state detection data
UL0, UL1</td><td>
• Width selection for the phase error (øE) detection function used to determine the PLL locked/unlocked state. When a phase error greater than the øE detection width from the table occurs, the PLL circuit is seen as in the unlocked state.
<table>
<tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detection output</th><th>X'tal</th></tr>
<tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td><td>10.25 M/10.35 MHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Directly outputs øE</td><td>10.25 M/10.35 MHz</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">0</td><td>±0.49 µs</td><td>øE is extended by 0.1 to 0.2 ms.</td><td>10.25 MHz</td></tr>
<tr><td>±0.49 µs</td><td>øE is extended by 0.11 to 0.22 ms.</td><td>10.35 MHz (fr = 30/9/3 k)</td></tr>
<tr><td>±0.43 µs</td><td>øE is extended by 0.1 to 0.2 ms.</td><td>10.35 MHz (Other than fr = 30/9/3 k)</td></tr>
<tr><td rowspan="3">1</td><td rowspan="3">1</td><td>±0.98 µs</td><td>øE is extended by 0.1 to 0.2 ms.</td><td>10.25 MHz</td></tr>
<tr><td>±0.97 µs</td><td>øE is extended by 0.11 to 0.22 ms.</td><td>10.35 MHz (fr = 30/9/3 k)</td></tr>
<tr><td>±0.87 µs</td><td>øE is extended by 0.1 to 0.2 ms.</td><td>10.35 MHz (Other than fr = 30/9/3 k)</td></tr>
</table>


*: When unlocked, the DO pin goes low and the serial data output is UL = 0.
</td><td>ULD
DT0, DT1</td></tr>
<tr><td>(10)</td><td>Charge pump control data
DLC</td><td>
• Bit that forcible sets the charge pump output to the low level.
DLC = 1: Low level
DLC = 0: Normal operation
*: If a deadlock occurs due to the VCO control voltage (Vtune) going to zero and stopping the VCO oscillator, set the charge pump output to the low level and set Vtune to V_{CC} to escape from the deadlocked state (deadlock clearing circuit). Normal operation is selected after the power-on reset.
</td><td></td></tr>
<tr><td>(11)</td><td>Phase comparator control data
DZ0, DZ1</td><td>
• Controls the phase comparator dead band.
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead band mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
*: The phase comparator operates in DZA mode after the power-on reset. (Recomended modes: DZD, DZC)
</td><td></td></tr>
<tr><td>(12)</td><td>High-speed locking convergence range control data
TLR0, TLR1</td><td>
• Data to control the frequency in the convergence range to judge the high-speed locking control completion. This data is valid when FMIN (high-speed mode) is selected by setting DVS and SNS to 1.
<table>
<tr><th>TLR1</th><th>TLR0</th><th>Convergence range [kHz]</th></tr>
<tr><td>0</td><td>0</td><td>50</td></tr>
<tr><td>0</td><td>1</td><td>100</td></tr>
<tr><td>1</td><td>0</td><td>150</td></tr>
<tr><td>1</td><td>1</td><td>200</td></tr>
</table>
*:The convergence range is 200 kHz at a power-on reset.
Refer to Description of the High-Speed Locking Control System (P.19) for details.
</td><td>DVS
SNS</td></tr>
</table>

Continued on next page.

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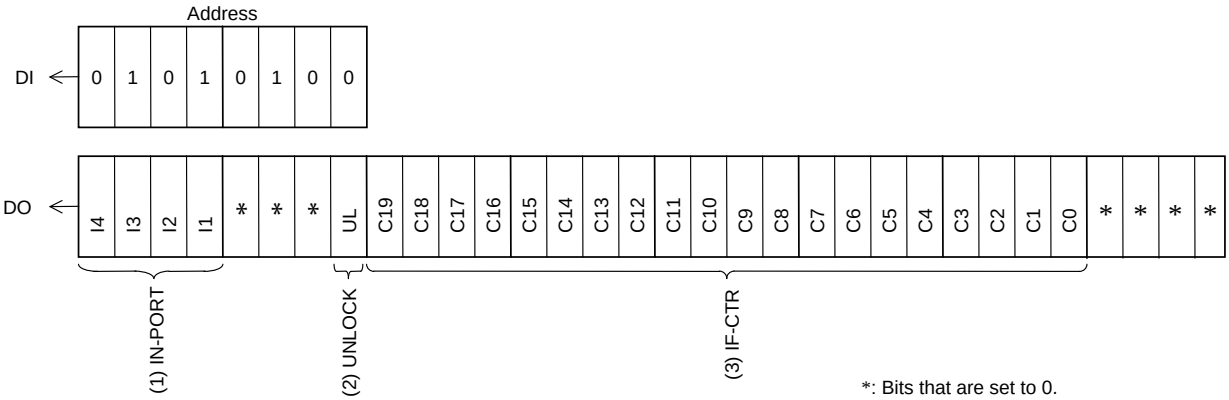
<table>
<tr><th>No.</th><th>Control block/data</th><th>Content</th><th>Related data</th></tr>
<tr><td>(13)</td><td>High-speed locking charge wait time control data
CWS0, CWS1</td><td>• Data to control the wait time in the high-speed locking. This data is valid when the FMIN (high-speed mode) is selected by setting DVS and SNS to 1.
<table><tr><th>CWS1</th><th>CWS0</th><th>Wait time [µs]</th></tr><tr><td>0</td><td>0</td><td>2.5</td></tr><tr><td>0</td><td>1</td><td>5</td></tr><tr><td>1</td><td>0</td><td>10</td></tr><tr><td>1</td><td>1</td><td>20</td></tr></table>*:The wait time is 20 µs at a power on reset.
Refer to Description of the High-Speed Locking Control System (P.19) for details.</td><td>DVS
SNS</td></tr>
<tr><td>(14)</td><td>High-speed locking completion flag output wait time control data
HSE0, HSE1</td><td>• Data to control the wait time after the high-speed locking control completes till the operation is switched to the normal PLL operation. This data is valid when the FMIN (high-speed mode) is selected by setting DVS and SNS to 1.
During the wait time, the unlock signal is forcibly output, the sub-charge pump allows to be operated. Thereby, reduces the locking time after switching to the normal PLL operation.
<table><tr><th>HSE1</th><th>HSE0</th><th>Wait time [µs]</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>200</td></tr><tr><td>1</td><td>0</td><td>400</td></tr><tr><td>1</td><td>1</td><td>800</td></tr></table>*:The wait time is 400 µs at a power on reset.
Refer to Description of the High-Speed Locking Control System (P.19) for details.</td><td>DVS
SNS
PDC0
PDC1</td></tr>
<tr><td>(15)</td><td>IC test data
TEST0
TEST1
TEST2
TEST3</td><td>• IC test control data
These bits must be set as follows during normal operation.
TEST0 = 0
TEST1 = 0
TEST2 = 0
TEST3 = 0
*: After the power-on reset, the test data is all set to zero.†</td><td></td></tr>
<tr><td>(16)</td><td>Reset
RST</td><td>• This data resets the LC72151V.
*: After the power is first applied, the power-on reset circuit initializes the IC. However, the data must be set to 1 to ensure the initialization.</td><td></td></tr>
<tr><td>(17)</td><td>DNC</td><td>• Set data to 0</td><td></td></tr>
<tr><td>(18)</td><td>Crystal oscillator circuit
XS
XB</td><td>• Crystal oscillator selection data
XS = 0: 10.25 MHz
= 1: 10.35 MHz
• Crystal oscillator buffer (XBUF)
XB = 0: Buffer output is turned off.
XB = 1: Buffer output is turned on.
*: XB = 0: Buffer output is turned off at a power-on reset.</td><td>R0 to R3</td></tr>
</table>

†Note: After power is first applied, the power-on reset circuit initializes the IC. However, the CCB data (RST) must be input to the IC to ensure the initialization.

Structure of the DO Output Data (serial output data)

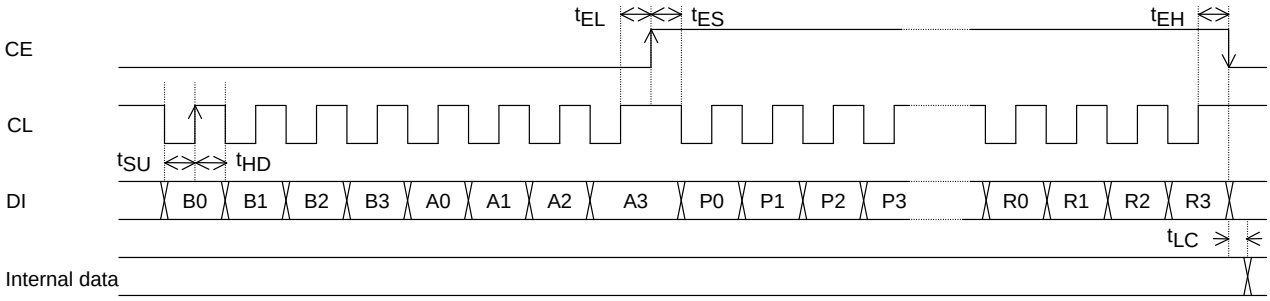
(3) OUT mode



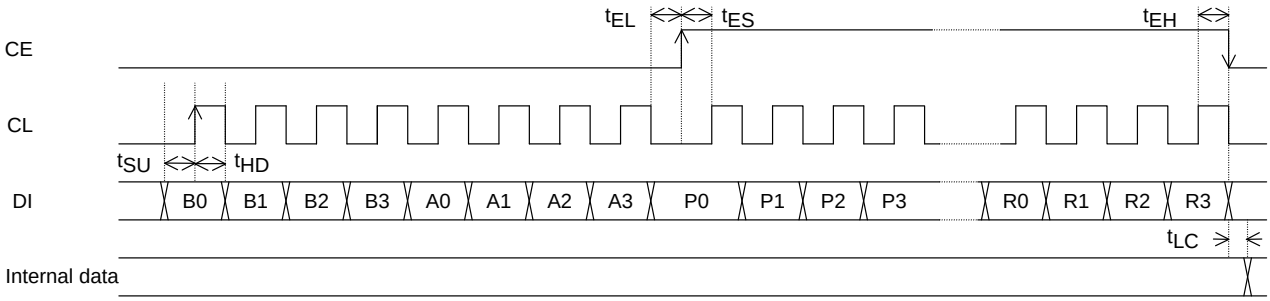
No.	Control block/data	Content	Related data
(1)	I/O port data I4 to I1	• The bits I1 to I4 are set to the latched states of the I/O pins I/O-1 and I/O-2 and the input pins HCTR/I-3 and LCTR/I-4. These states are latched at the point the IC enters data output mode. The pin states are latched regardless of the pin mode (input or output). I1, I2 ← I/O-1 and I/O-2 pin states I3, I4 ← HCTR/I-3 and LCTR/I-4 pin states Pin state = high: 1 low: 0	I/O-1 I/O-2 H/I-3 L/I-4
(2)	PLL unlock data UL	• Data created by latching the value for the unlock detection circuit UL ← 0: Unlocked 1: Locked or in detection halt mode	UL0 UL1
(3)	IF counter binary counter C19 to C0	• Data created by latching the value for the IF counter (20-bit binary counter) C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTE GT0 GT1

Serial data input (IN1/IN2) t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH}, > 0.45 µs t_{LC} < 0.45 µs

(1) CL: Normally high

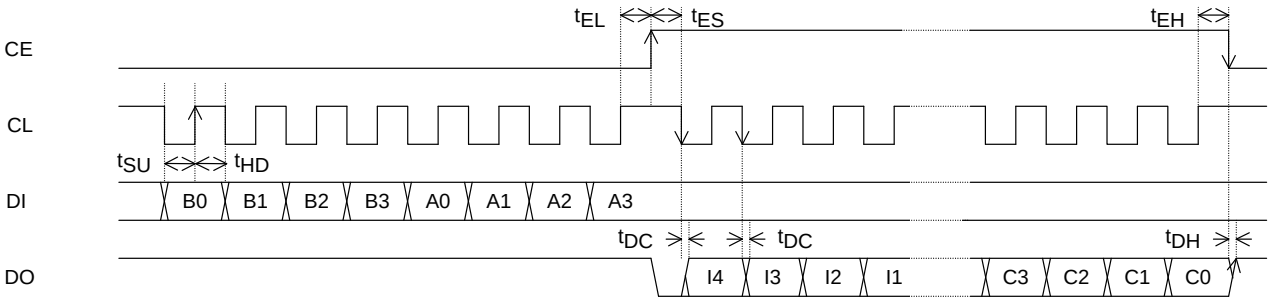


(2) CL: Normally low

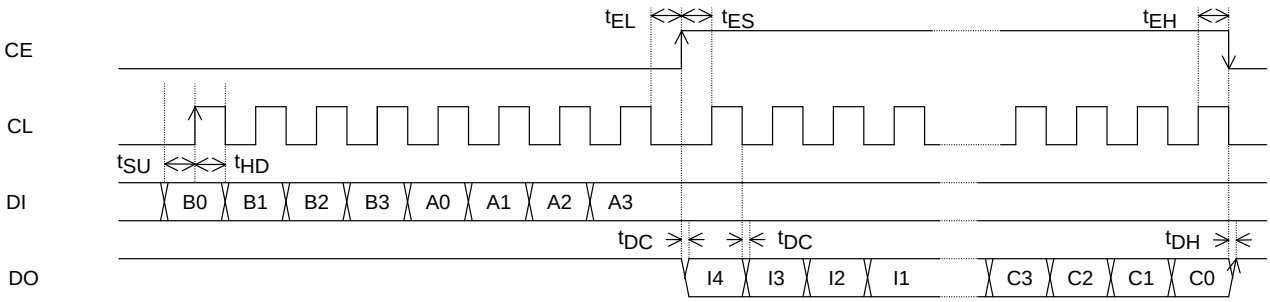


Serial data output (OUT) t_{SU}, t_{HD}, t_{EL}, t_{ES}, t_{EH} > 0.45 µs t_{DC}, t_{DH} < 0.2 µs

(1) CL: Normally high

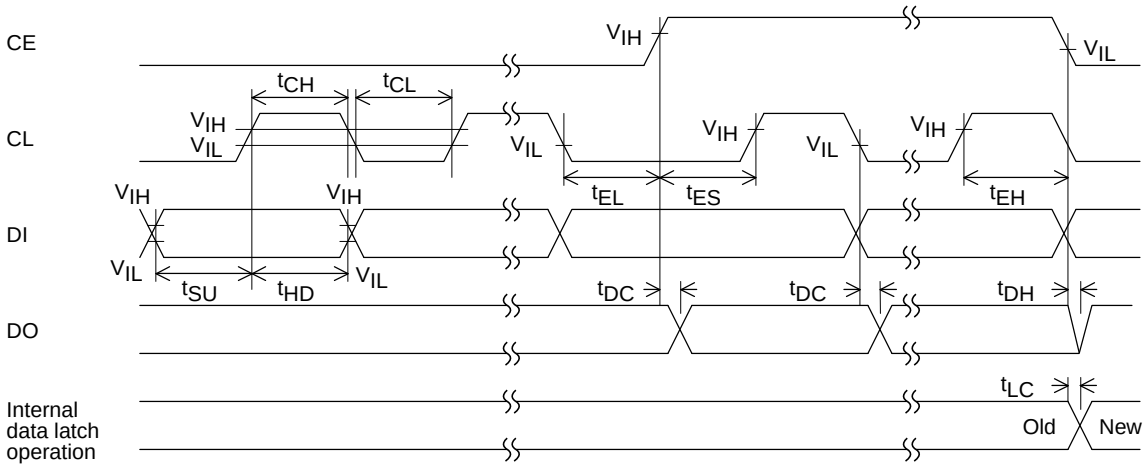


(2) CL: Normally low

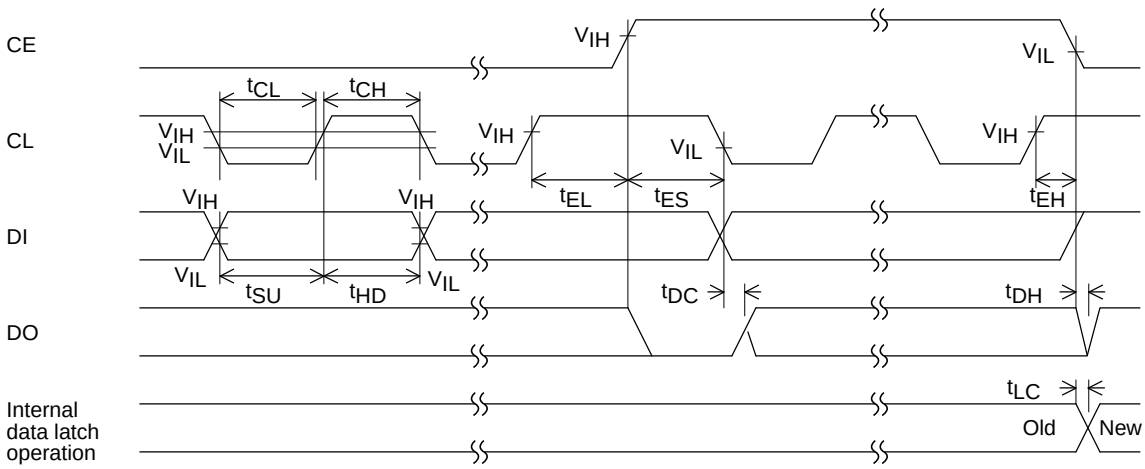


Note: The DO pin is an n-channel open drain output, and thus the data switching time will differ depending on the value of the pull-up resistor used and the printed circuit board capacitance.

Serial data timing



<When CL is stopped at the low level>



<When CL is stopped at the high level>

Allowable Operating Ranges at Ta = –40 to 85°C, V_{SS} = 0 V

Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Data setup time	t_{SU}	DI, CL		0.45			µs
Data hold time	t_{HD}	DI, CL		0.45			µs
Clock low-level period	t_{CL}	CL		0.45			µs
Clock high-level period	t_{CH}	CL		0.45			µs
CE wait time	t_{EL}	CE, CL		0.45			µs
CE setup time	t_{ES}	CE, CL		0.45			µs
CE hold time	t_{EH}	CE, CL		0.45			µs
Data latch change time	t_{LC}					0.45	µs
Data output time	t_{DC}	DO, CL	Depends on the value of the pull-up resistor used.			0.2	µs
	t_{DH}	DO, CE					

Note: See the timing chart for serial data transfers.

Description of the High-Speed Locking Control System

The LC72151V realizes the maximum inter-band edge high-speed locking time 500 μs by optimizing the filter constants and internal status setting when the FMIN (high-speed mode) by setting DVS and SNS to 1. The following describes the high-speed locking control system.

Procedure

The LC72151V operates as shown below when selecting FMIN (high-speed mode) and setting sub-charge pump operation during unlocked.

	PDF/PDM1/PDM2/PDS/TGI1/TGI2 pin states					
	PDF	PDM1	PDM2	PDS	TGI1	TGI2
Change value N	×	○	○	×	×	○
↓						
New high-speed locking control (When the value N variation is under 16, only operates the normal PLL.)	○	×	×	×	○	×
↓						
Operates normal PLL when the local oscillation frequency enters the high-speed locking frequency range. (The sub-charge pump operates for the time set by the high-speed locking completion flag output wait time.)	×	○	○	○	×	○
↓						
Stops the sub-charge pump and only the main-charge pump operates. (Normal locking state)	×	○	○	×	×	○

*: ○ : operating; × : stopped (high-impedance)

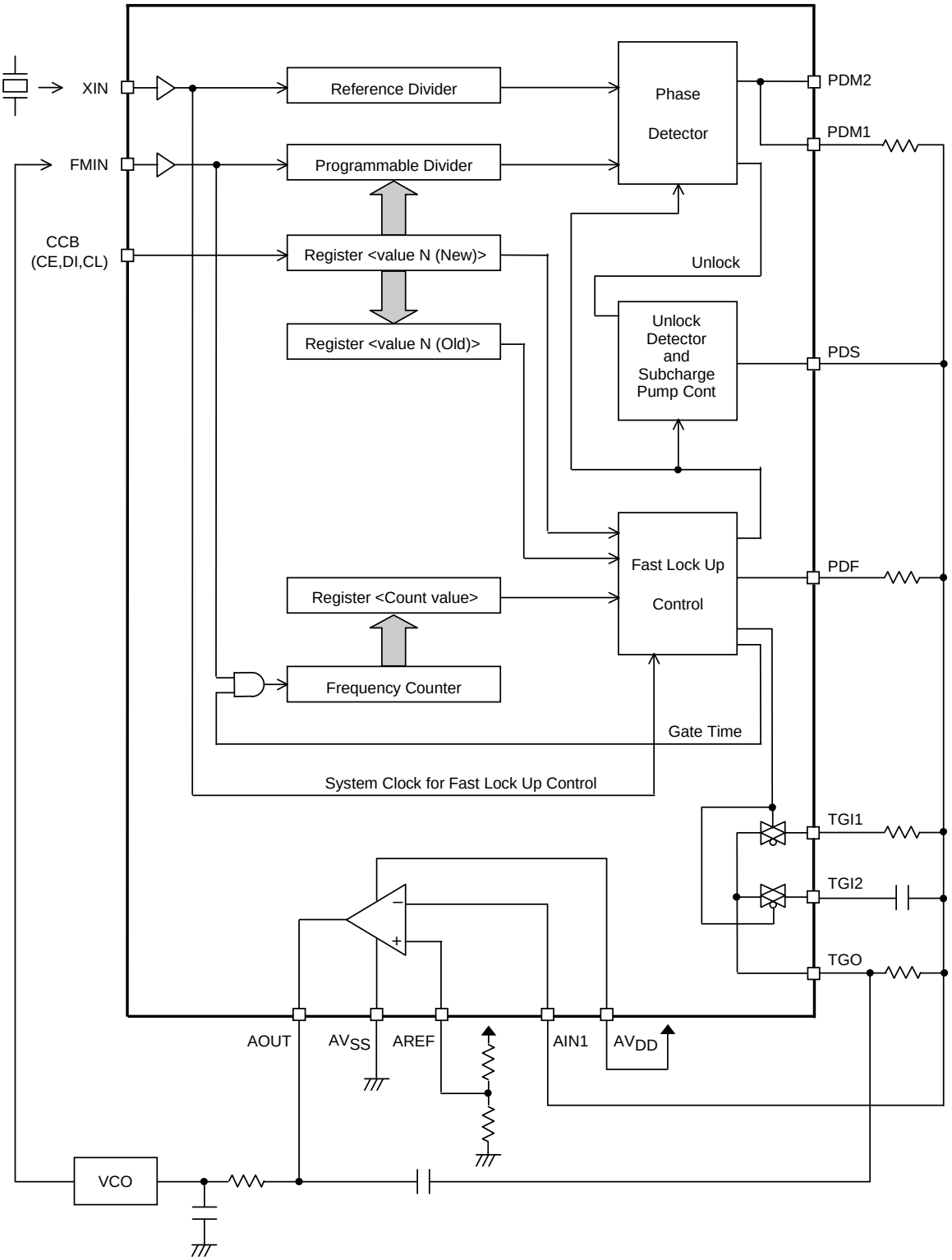
Control Data

Setting data (CCB) necessary for the new high-speed locking control is described below.
This data is valid when the FMIN (high-speed mode) is selected by setting DVS and SNS to 1.

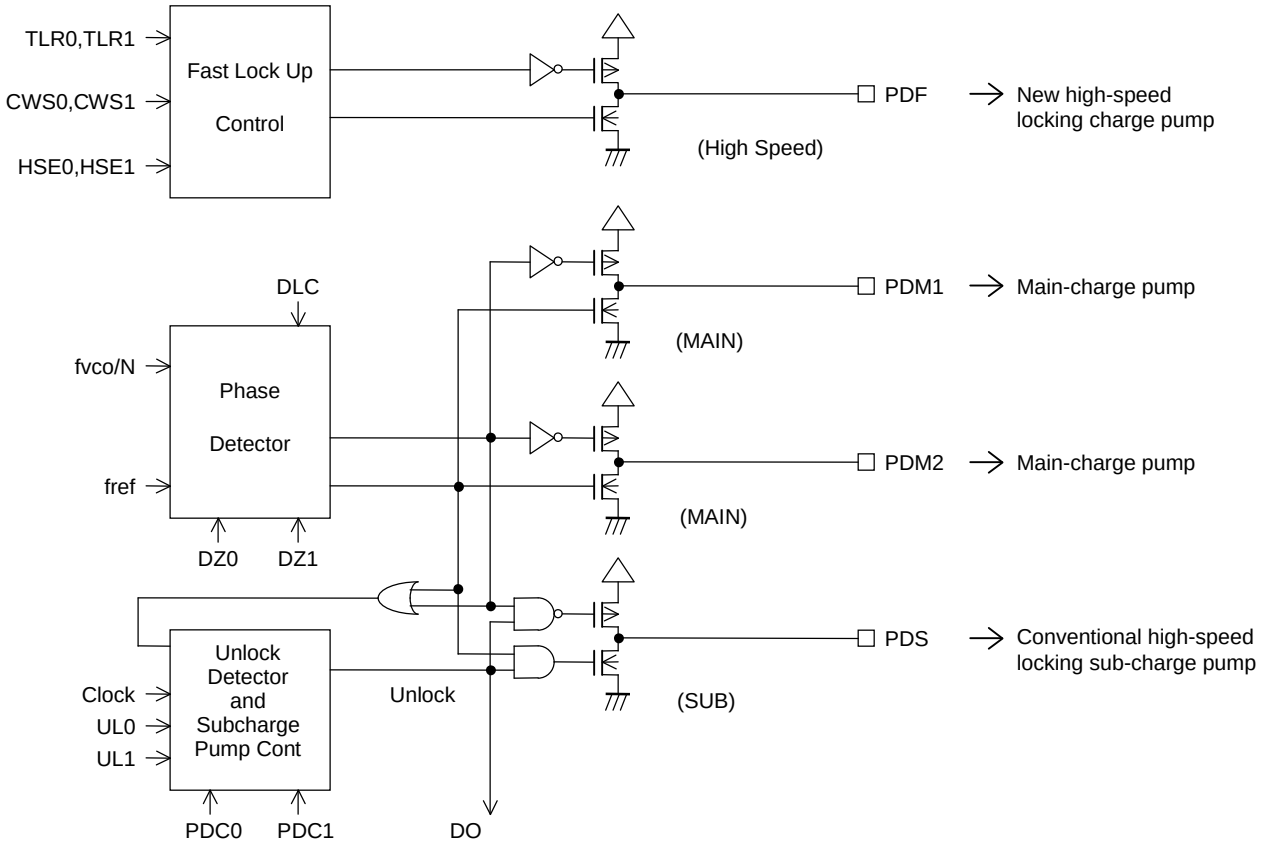
CCB data	Name (Selectable set value)	Description	Recommended value
TLR0/TLR1	High-speed locking convergence range (±50/100/150/200 kHz)	The new high-speed locking control controls the convergence of the target frequency into the set frequency range. This data can be used to set the frequency range for convergence judgement. *: As the convergence range narrower, the locking time tends to be shorter.	TLR0 = 0 TLR1 = 0 (±50 kHz)
CWS0/CWS1	High-speed locking charge wait time (0/2.5/5/10 μs)	During the new high-speed locking control, charge application from the PDF pin and local oscillation frequency measurement for the FMIN pin are repeatedly implemented. This data can be used to set the Vt voltage stable time after the charge is applied until the local oscillator frequency is measured. *: Voltage stable time Vt changes according to the peripheral circuit.	CWS0 = 1 CWS1 = 0 (5 μs)
HSE0/HSE1	High-speed locking completion flag output wait time (0/100/200/400 μs)	After the new high-speed locking control ends, since the phase remains in convergence state in the internal unlock detection circuit until the locking judgement is implemented, the sub-charge pump will not operate by the sub-charge pump operation setting during unlocked. This data can be used to set the time to force the sub-charge pump to operate for after the new high-speed locking control completes. *: After the new high-speed locking control completes, the locking time tends to be shortened by operating the sub-charge pump for an adequate time.	HSE0 = 0 HSE1 = 1 (400 μs)

*: The recommended values are for reference purpose only, not the guarantee values for the fastest locking time.

Block Diagram



Charge Pump Structure



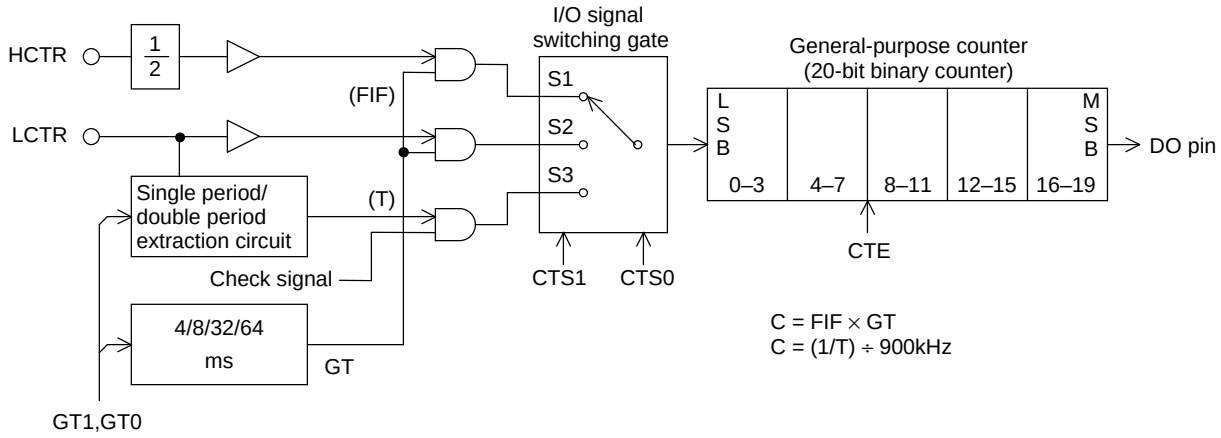
PDC1	PDC0	PDS(Sub-charge pump state)
0	*	High impedance
1	1	Charge pump operating (at all times)
1	0	Charge pump operating (when PLL unlocked)

DLC	PDM1, PDM2, PDS
0	Normal operation
1	Forced low

Note: If the unlock state is detected when the channel changes, the sub-charge pump (PDS) operates. Since the sub-charge pump operates concurrently with the main-charge pump, decrease the time constants for the low-pass filter to accelerate the locking.

However, note that when the FMIN (high-speed mode) is selected and when the channel changes (during high-speed locking control), both the main- and the sub-charge pumps do not operate and enter the high impedance state, and forcibly implement an unlock judgement. When locked at a high-speed locking control completion, the output is not extended but locking is instantaneously judged. By selecting sub-charge operation (during unlocked) with FMIN (high-speed mode) selected, the sub-charge pump is forcibly operated to shorten the locking time for the time set by the high-speed locking completion flag output wait time control data (HSE0, HSE1) after switching from high-speed locking control to normal PLL operation.

General-purpose counter structure



Parameter	LCTR period measurement mode check signal frequency		
X'tal OSC	10.25 MHz	10.35 MHz	
		fref = 30, 9, 3 kHz	fref = other than 30, 9, 3 kHz
Check signal	1025 kHz	1030 kHz	1150 kHz

	CTS1	CTS0	Input pin	Measurement mode	Frequency range	Input sensitivity
S1	1	*	HCTR	Frequency	0.4 to 25.0 MHz	40 mVrms *1
S2	0	1	LCTR	Frequency	10 to 500 kHz	40 mVrms *1
S3	0	0	LCTR	Period	1.0 to 20 × 10^3 Hz	(Pulse)

*1: CTC = 0: 40 mVrms
CTC = 1: 70 mVrms

	HCTR: Minimum input sensitivity regulation f [MHz]		
CTC	0.4 ≤ f < 8	8 ≤ f < 12	12 ≤ f ≤ 25
0 (Normal mode)	40 mVrms	40 mVrms (5 to 15 mVrms)	40 mVrms
1 (Degrade mode)	—	70 mVrms (40 to 60 mVrms)	—

	LCTR: Minimum input sensitivity regulation f [MHz]	
CTC	10 ≤ f< 400	400 ≤ f ≤ 500
0 (Normal mode)	40 mVrms	20 mVrms (1 to 10 mVrms)
1 (Degrade mode)	—	70 mVrms (15 to 30 mVrms)

—: No stipulation (Not guaranteed)
( ): Actual value (Reference value)

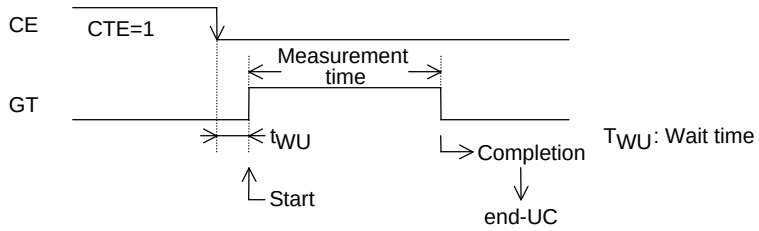
GT1	GT0	Frequency measurement mode		Period measurement mode
		Measurement time	Wait time	
0	0	4 ms	3 to 4 ms	1 period
0	1	8	7 to 8 ms	2 periods
1	0	32		
1	1	64		

CTC: Input sensitivity select data. Input sensitivity is degraded by setting CTC to 1.
However, the actual value for HCTR is in the range 40 to 60 mVrms at 10.7 MHz, for LCTR is in the range 15 to 30 mVrms at 450 kHz.

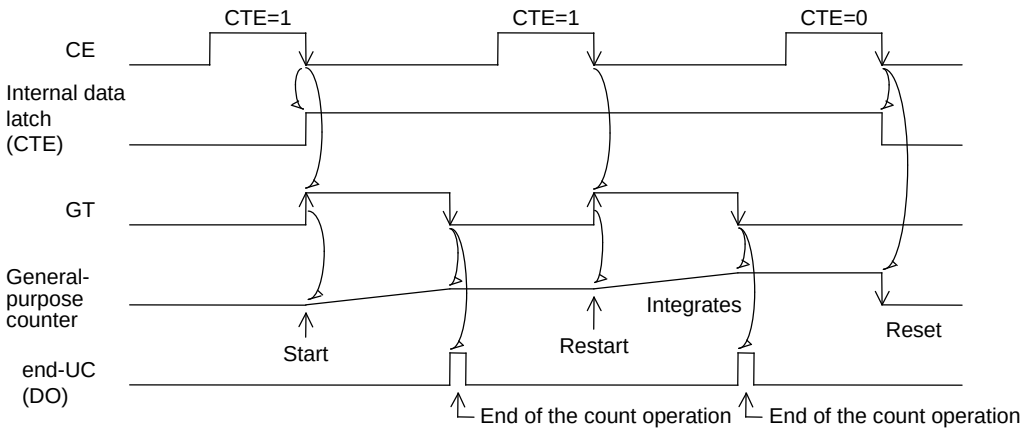
CTP: Input pull-down can be inhibited by setting CTP to 1.
Set CTP to 1 4 ms before setting CTE to 1. Set CTP to 0 when the counter is not used.
Wait time will be reduced to 1 to 2 ms by setting CTP to 1.

The LC72151V's general-purpose counter is a 20-bit binary counter.
The result of the count operation can be read out MSB first from the DO pin.
The measurement time when the general-purpose counter is used for frequency measurement is set to either 4, 8, 32, or 64 ms by the GT0 and GT1 bits. The frequency of the input to the HCTR pin can be measured by determining how many pulses were input to the general-purpose counter during this measurement time.

When the general-purpose counter is used to measure the frequency, the period of the signal input to LCTR pin can be measured by counting the number of check signals input to the general-purpose counter for the one or two periods of the signal input to the LCTR pin.
Reset the general-purpose counter in advance by setting CTE to 0 before starting the counter.
A general-purpose counter count operation is started by setting the CTE bit in the serial data to 1. The serial data takes effect internally to the LC72151V when the CE pin input level is changed from high to low. The input to the HCTR pin must be provided before the wait time has elapsed after CE was set low.
Next, the result of the general-purpose counter count after the measurement completes must be read out while CTE is still set to 1. This is because the general-purpose counter is reset when CTE is set to 1.
Never fail to reset the general-purpose counter before starting the count operation of the general-purpose counter. In addition, the signal input to LCTR pin is directly transmitted to the general-purpose counter.
Note that the signal input to the HCTR pin is first divided by 2 internally to the IC and then input to the general-purpose counter. Therefore, the result of the general-purpose counter count is a value that corresponds to 1/2 of the frequency actually input to the HCTR pin.



When used as an integrating counter



*CTE: 0 → • Resets the general-purpose counter
1 → • Starts the general-purpose counter
• Restarts the counter if set to 1 again.

In integrating count mode, the count value of the general-purpose counter is accumulated. Care must be taken to handle counter overflow correctly. The count value will be in the range 0_H to $FFFFF_H$.

Other items

(1) Notes on the phase detector dead band

DZ1	DZ0	Dead band mode	Charge pump	Dead band
0	0	DZA	ON/ON	– –0 s
0	1	DZB	ON/ON	–0 s
1	0	DZC	OFF/OFF	+0 s
1	1	DZD	OFF/OFF	++0 s

When the charge pump operates in ON/ON mode, the charge pump generates correction pulses even when the PLL is locked. Here, it is easy for the loop to become unstable, and special care is required in designs that use this mode.
The following problems may occur in ON/ON mode.

- Side bands may be generated due to reference frequency leakage.
- Side bands may be generated due low-frequency leakage due to the envelope of the correction pulses.

When a dead band is present (OFF/OFF mode), the loop will be stable, but it will be harder to acquire a good C/N ratio. On the other hand, with the mode that does not have a dead band (ON/ON mode), it will be easier to acquire a high C/N ratio, but harder to acquire loop stability.
Therefore, the DZA and DZB modes, in which there is no dead band, can be effective if either a high signal-to-noise ratio of 90 to 100 dB in FM reception or an increased pilot margin in AM stereo reception is required.
Inversely, if such a high FM signal-to-noise ratio is not required for FM reception, or an adequate pilot margin can be acquired for AM stereo reception, then the DZC and DZD modes, in which a dead band is present, may be more effective.

Dead zone (dead band) definition

The phase comparator compares fp with the reference frequency (fr) as shown in figure 1. This circuit outputs a voltage V (A) that is proportional to the phase difference ø as shown in figure 2. However, due to internal delays and other factors, the actual IC is unable to compare small phase differences, and thus a dead zone (B) appears in the output. To achieve a high signal-to-noise ratio in the end product, the dead zone should be as small as possible.

However, in popularly-priced models, there are cases where a somewhat wider dead zone may be easier to work with. This is because in some situations, such as when a powerful signal is applied to the RF input, in popularly-priced models there may be RF leakage from the mixer to the VCC. When the dead zone is narrow, outputs to correct this leakage are output, that output in turn modulates the VCO, and generates a beat signal with the RF.

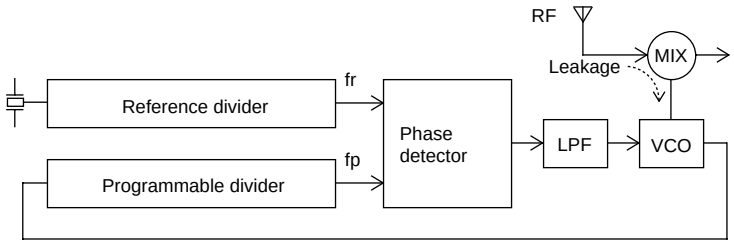


Figure 1

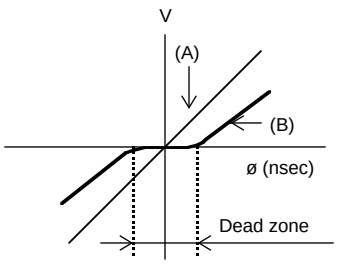


Figure 2

(2) Notes on the FMIN, AMIN, HCTR/I-3, and LCTR/I-4 pins
The coupling capacitor must be located as close as possible to these pins. A capacitance of approximately 100 pF is desirable.
In particular, if the HCTR/I-3 and LCTR/I-4 pin capacitor is over about 1000 pF, the time required to reach the bias level may become excessive, and incorrect counting may occur due to the relationship with the wait time.

(3) Notes on the IF counting using HCTR/I-3 and LCTR/I-4 pins
When counting the IF frequency, the application microcontroller must test the state of the IF IC SD (station detect) signal, and only if the SD signal is present, turn on the IF counter buffer output and perform an IF count operation. Methods in which auto-search operations are implemented only using the IF count may incorrectly stop at frequencies where no station is present due to leakage from the IF counter buffer.

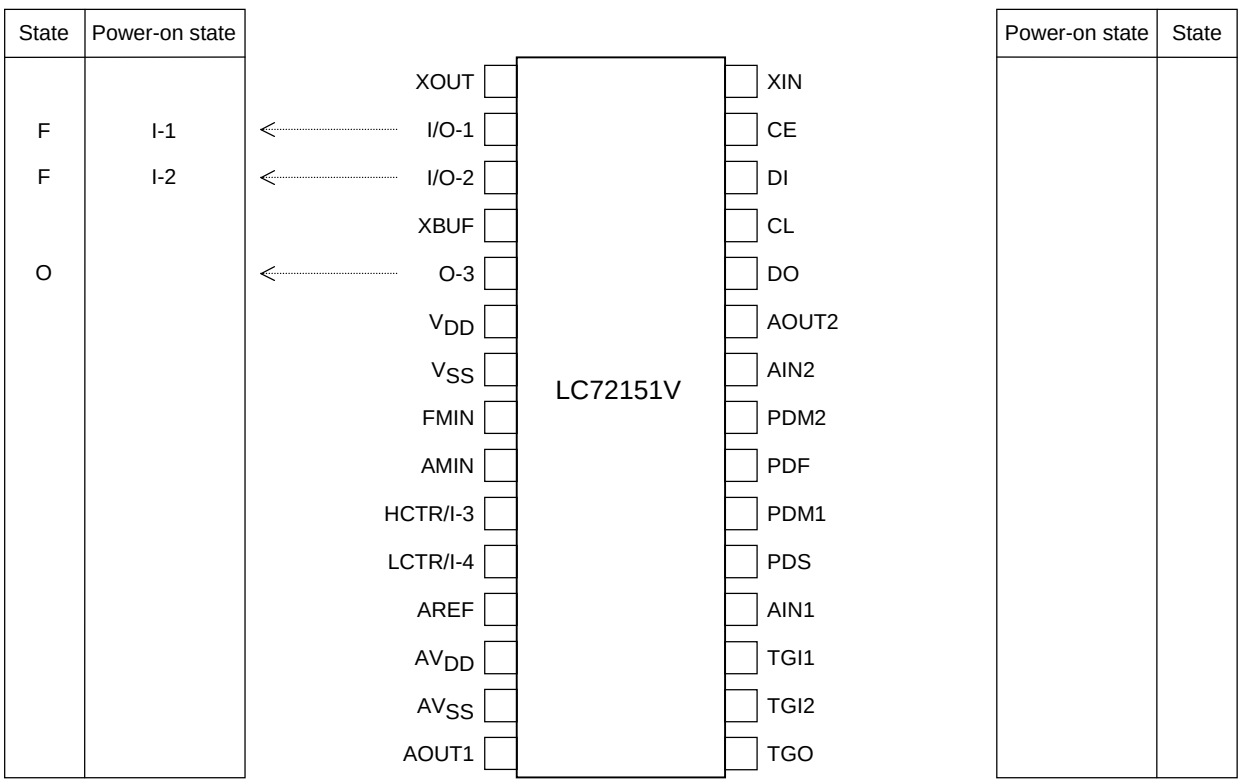
(4) Using the DO pin
At times other than data output mode, the DO pin can also be used to check for general-purpose counter count operation completion, to output the unlock state detection signal, and to check for changes in the input pins.
Note that the states of the input pins (I/O-1 and I/O-2) can be directly input to the system microcontroller through the DO pin.

(5) Power supply pins
Capacitors of at least 0.1 µF must be inserted between the V_{DD} and V_{SS} power supply pins and between AV_{DD} and AV_{SS} to reduce noise.
These capacitors must be located as close to the V_{DD} and V_{SS}, AV_{DD} and AV_{SS} pins as possible.
Additionally, power must be applied to AV_{DD} before applying to V_{DD}, and AV_{DD} must be higher than or equal to V_{DD}.

(6) Note on power application
After power is first applied, the power-on reset circuit initializes the IC. However, the CCB data RST must be set to 1 to ensure the initialization.

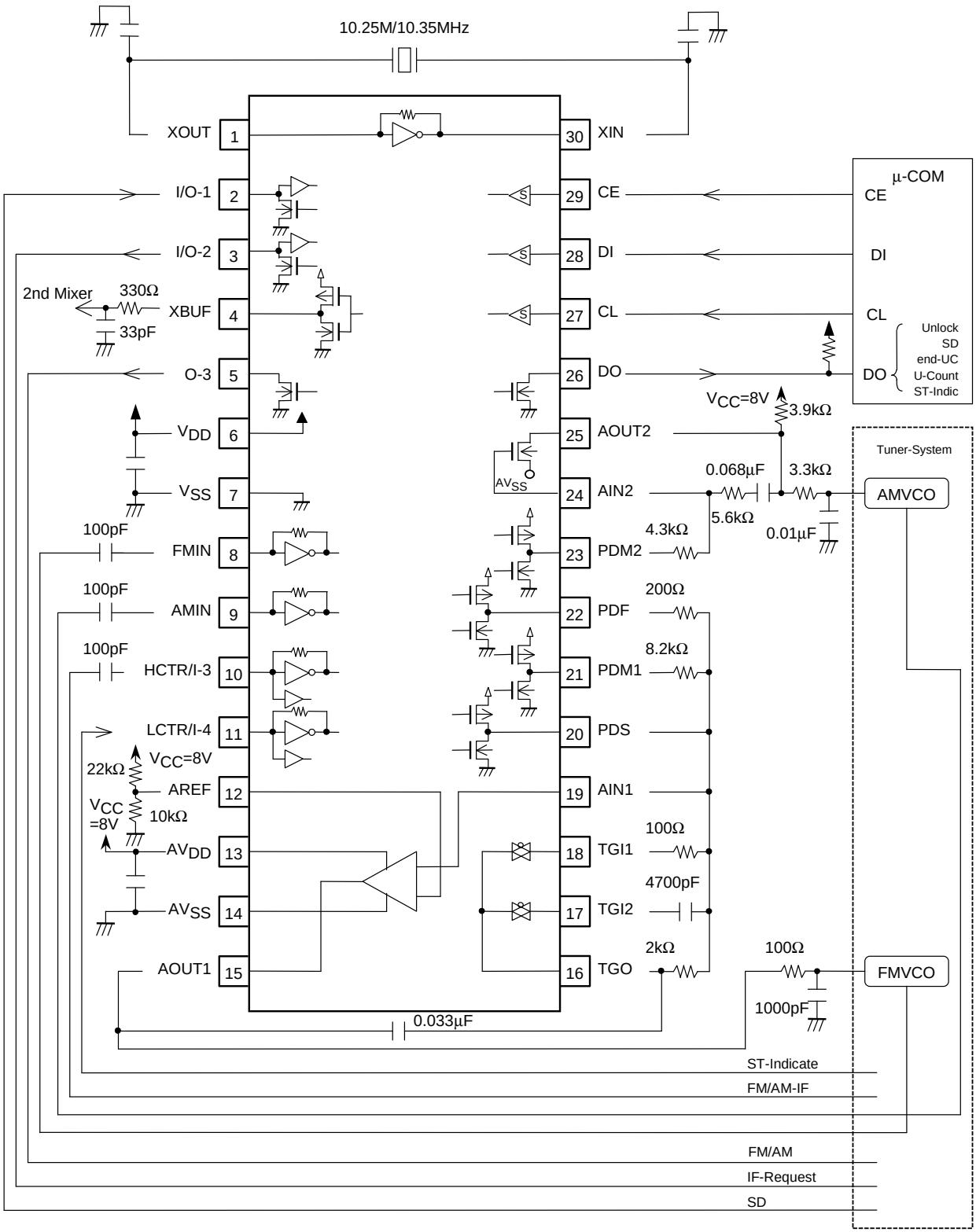
(7) Notes on VCO design
The VCO must be designed so that the VCO oscillation does not stop if the control voltage (Vtune) becomes 0 V. If it is possible for this oscillator to stop, use the charge pump control data (DLC) to forcible set Vtune to VCC temporarily to prevent the PLL circuit from deadlocking. (This function is called a deadlock clear circuit.)

Pin states during a power-on reset



O: Open L: Low F: Floating

Sample Application Circuit



*: The constants shown are for reference purpose only, but do not guarantee the operation.

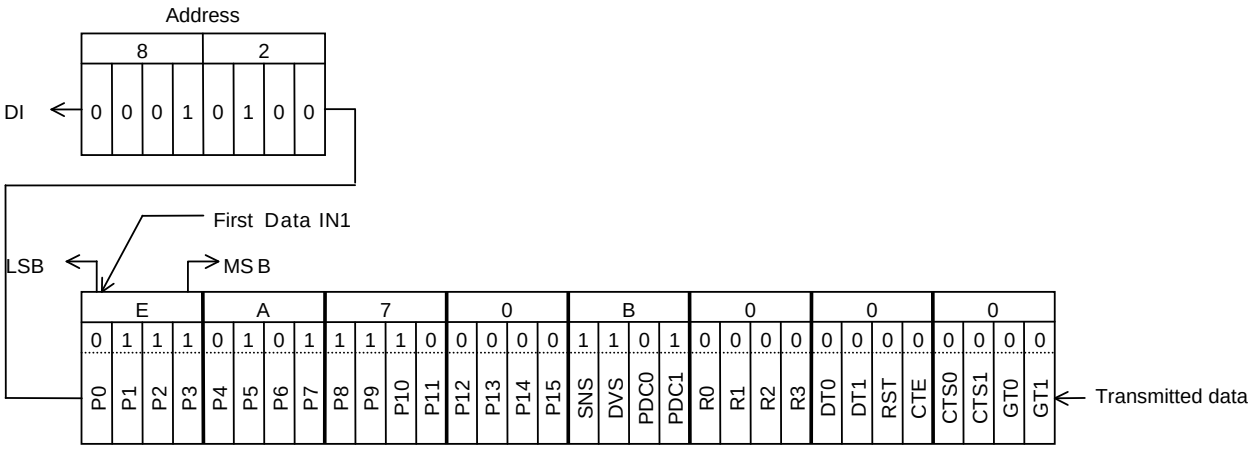
Notes: 1. Power must be applied to AV_{DD} before applying to V_{DD}, and AV_{DD} must be higher than or equal to V_{DD}.

2. AREF is an op-amp reference input voltage pin and must be applied a voltage 1/2 V_{DD}. The applied voltage requires to be applied from another power supply from V_{DD} to prevent affections due to logic system noise or other factors.

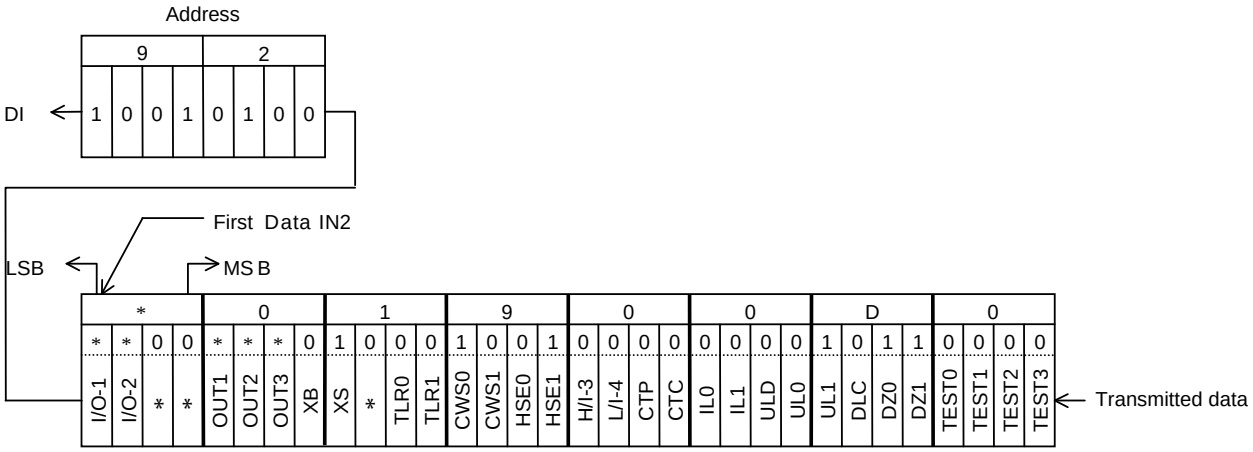
LC72151V State Setting Examples

1. In the case of FMRF 87.5 MHz reception (X'tal = 10.35 MHz/IF = +10.8 MHz)
   FM VCO = 98.3 MHz
   X'tal = 10.35 MHz, fref = 50 kHz : XS = 1, R0 = R1 = R2 = R3 = 0
   FMIN (high-speed mode) selected : DVS = 1, SNS = 1
   Dead-zone mode = DZD : DZ0 = DZ1 = 1
   Programmable divider divisor
   98.3 MHz ÷ 50 kHz = 1966 → 07AE (Hex)
   High-speed locking control conditions
   High-speed locking convergence range = ±50 kHz : TLR0 = TLR1 = 0
   High-speed locking charge wait time = 5 µs : CWS0 = 1, CWS1 = 0
   High-speed locking completion flag output wait time = 400 µs : HSE0 = 0, HSE1 = 1
   Unlock detection width = ±0.43 µs : UL0 = 0, UL1 = 1

[IN1]

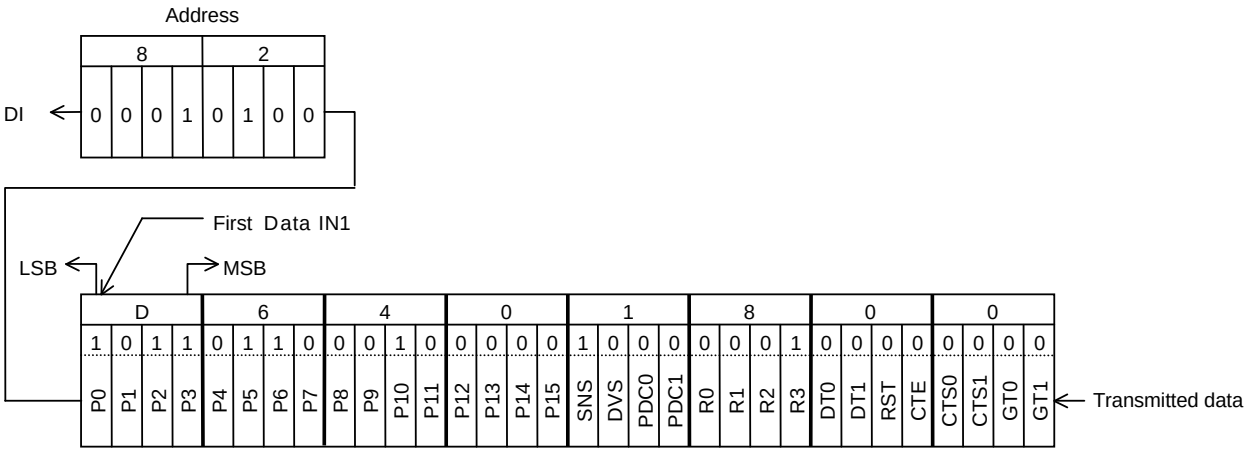


[IN2]

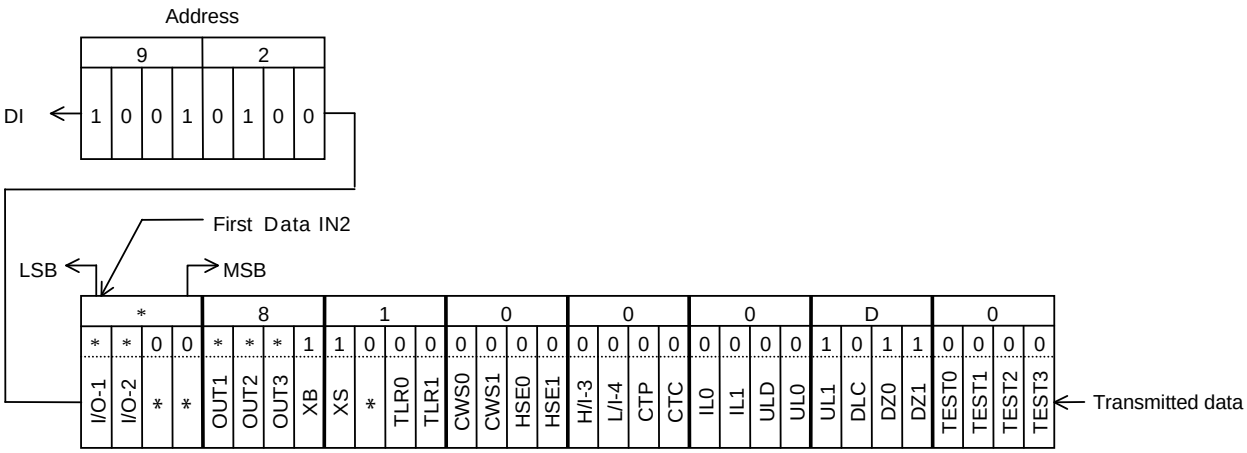


2. In the case of AMRF 530 kHz reception (X'tal = 10.35 MHz/IF = 10.8 MHz)
   AM VCO = 11.330 MHz
   X'tal = 10.35 MHz, fref = 10 kHz : XS = 1, R0 = R1 = R2 = 0, R3 = 1
   X'tal Buffer ON : XB = 1
   AMIN selected : DVS = 0, SNS = 1
   Dead-zone mode = DZD : DZ0 = DZ1 = 1
   Programmable divider divisor
   11.330 MHz ÷ 10 kHz = 1133 → 046D (Hex)

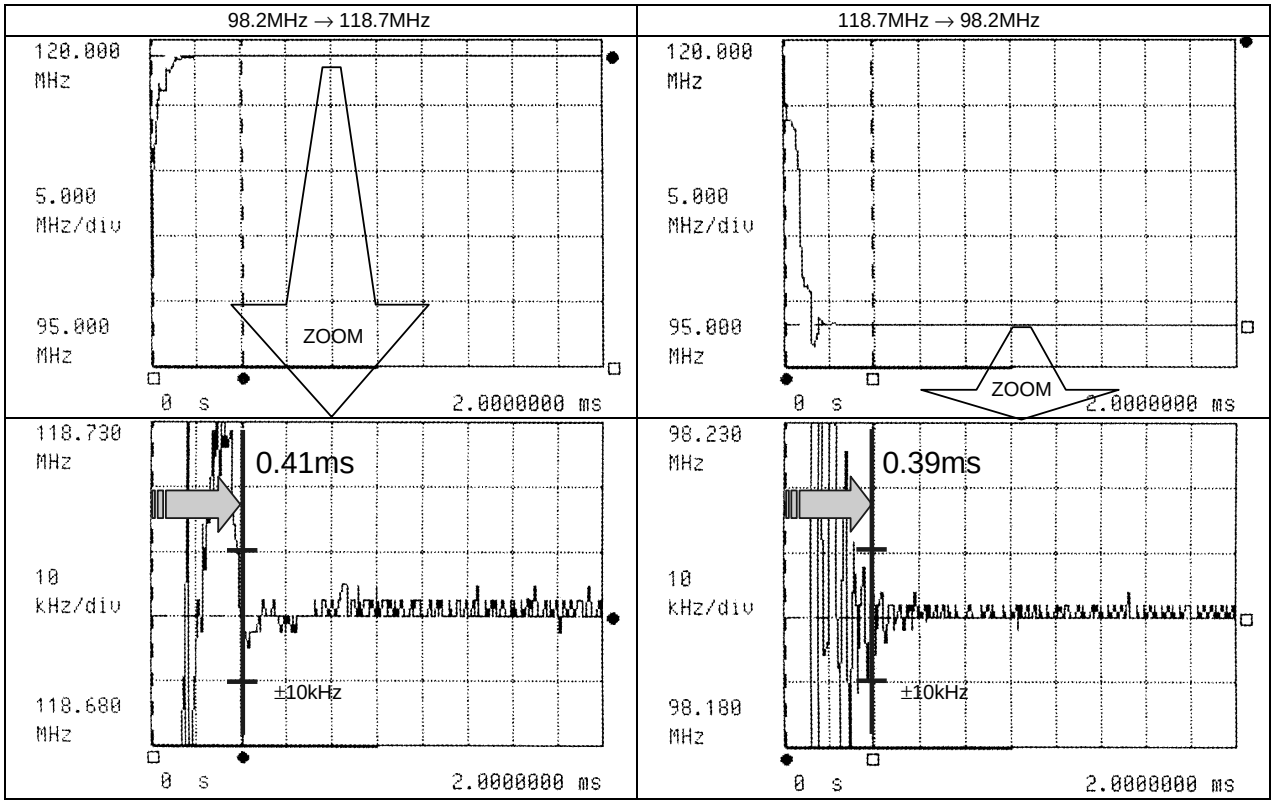
[IN1]



[IN2]



Locking time (Reference data)



*: Data here are measured using a SANYO evaluation board with the peripheral circuits and state setting shown in the Sample Application Circuit and the LC72151V State Setting Examples.