Ordering number :EN5640A

Monolithic linear IC

LA5621M, 5621V

Lithium-Ion Battery Charge Control IC

Overview

The LA5621M and LA5621V are external charge control ICs for lithium-ion batteries. These ICs are ideally suited for on/off control of external power MOSFETs in systems that incorporate a charging circuit in the set. They detect the charge and discharge status, output it to the set control microcontroller, which then outputs a signal to switch external power MOSFETS either on or off. Moreover, these ICs have a built-in function that detects discharge (countercurrent) from lithium-ion batteries within sets to external lithium-ion batteries in an AC adapter/charger, etc. and switches external power MOSFETs off.

Application

- Charge control of 1- or 2-cell lithium-ion batteries of video cameras, digital still cameras, cellular telephones, etc., used in combination with a microcontroller.

Functions

- Charge/discharge: In charge/discharge mode, switch external power MOSFETs on to charge the battery or discharge it to set load.
- Charge detection: Detect the charge status of lithium-ion batteries with comparator.
- Charge completion control: When charging of the lithium-ion battery is completed, the comparator is activated and the external power MOSFETs are switched off to stop charging.
- Countercurrent detection and control:
  In systems that support charging of both the set of the video camera, etc., and the AC adapter/charger, when spare batteries are charged on the AC adapter/charger side, if the battery voltage on the set side becomes high when the set is connected to the AC adapter/charger, current flows out to the battery on the AC adapter/charger side. These ICs feature a function that prevents this from happening.
- Charge prevention: A specified voltage is applied to the $\overline{\text{CHARGEINH}}$ pin to stop charging.

Features

- The combination of a microcontroller and external power MOSFETs enables easy charge/discharge control of lithium-ion batteries.
- Small power dissipation makes these ICs suitable for sets that require long time operation
- Use of compact package makes these ICs suitable for compact sets.
- Large power supply operation range supports both 1-cell and 2-cell lithium-ion batteries.

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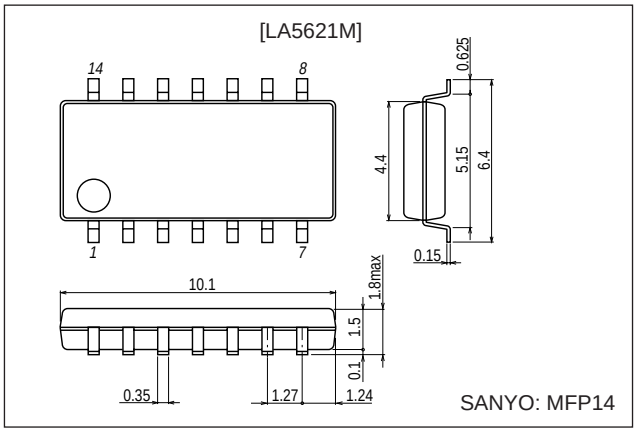
Package Dimensions

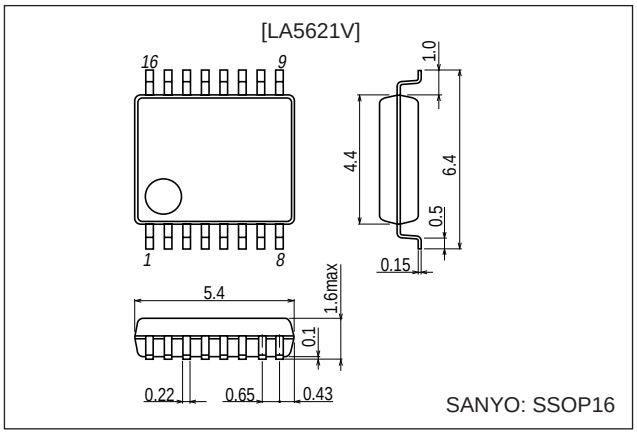
unit: mm

3034A-MFP14



unit: mm

3178-SSOP16



Specifications

Maximum Rating at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		11	V
Allowable power dissipation	Pd max	LA5621M	320	mW
		LA5621V	250	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +125	°C

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	$V_{CC}1$	$V_{CC}1 \le V_{CC}2$	1 to 11	V
Supply voltage 2	$V_{CC}2$	$V_{CC}1 \le V_{CC}2$*	2 to 5.5	V

Note: * When $V_{CC}1 < 2$ V, only the gate block (external power MOSFET drive) operates.

Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 5.5 V, $V_{CC}2$ = 3.15 V (unless otherwise specified)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain 1-1 (During set operation discharge)	$I_{CC}1$-1	$V_{CC}1$ in current, $V_{CHG} = V_{CC}2$, SW4, 6: on, SW5: off		90	120	µA
Current drain 2-1 (During set operation discharge)	$I_{CC}2$-1	$V_{CC}2$ in current, $V_{CHG} = V_{CC}2$, SW4, 6: on, SW5: off		20	26	µA
Current drain 1-2 (During charging outside set)	$I_{CC}1$-2	$V_{CC}2$ in current, $V_{CHG} = V_{CC}2$, SW4, 5: on		20	26	µA
Current drain 2-2 (During charging)	$I_{CC}2$-2	$V_{CC}2$ in current SW5: on, V_{CPU}: L, V_{GATE}:H		600	800	µA
[Output pin block]						
High-level CPU pin	$V_{CPU\text{-}H}$	$V_{IN}1^-$ = 15 mV, $V_{IN}1^+$ = 11 mV, $V_{CHG} = V_{CC}2$, SW4: off, SW5: on	$V_{CC}2 - 0.15$			V
Low-level CPU pin	$V_{CPU\text{-}L}$	$V_{IN}1^-$ = 15 mV, $V_{IN}1^+$ = 23 mV, $V_{CHG} = V_{CC}2$, SW4: off, SW5: on			0.2	V
CPU pin sink current	$V_{CPU\text{-}SINK}$	$V_{IN}1^-$ = 15 mV, $V_{IN}1^+$ = 23 mV, $V_{CHG} = V_{CC}2$, SW4: off, SW5: on		35		µA
High-level BIAS1 pin	$V_{BIAS}1$-H	SW1, 2, 5, 6: on	$V_{CC}2 - 0.15$			V
High-level BIAS2 pin	$V_{BIAS}2$-H	SW1, 2, 5, 6: on, $V_{IN}2^-$ = 15 mV, $V_{IN}2^+$ = 11 mV	$V_{CC}2 - 0.15$			V
Low-level BIAS2 pin leak current	$I_{BIAS}2$-LK	SW1, 2, 5, 6: on, $V_{IN}1^-$ = 15 mV, $V_{IN}1^+$ = 23 mV			10	µA

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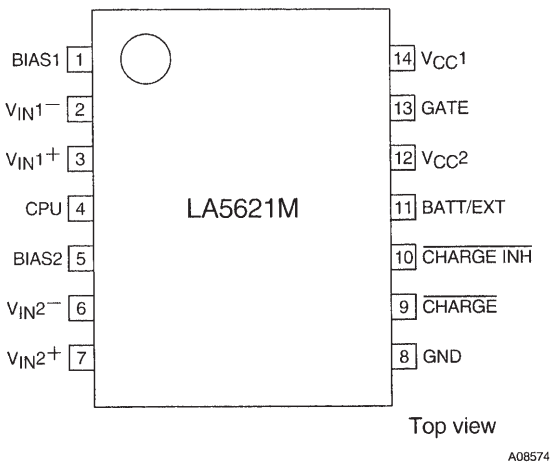
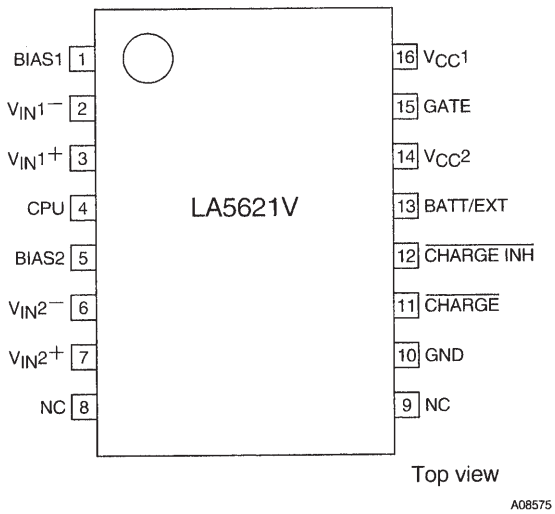
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[FET drive block]						
Drive high-level voltage	V_{GATE-H}	Same as current drain 1-1	5.3	5.4		V
Drive low-level voltage	V_{GATE-L}	SW6: on, Same as current drain 1-2		0.1	0.2	V
[Comparator block] SW1, 2, 5, 6: on						
Input offset voltage 1	$V_{IO}1$	Comparator 1, when CPU voltage is reversed	–3	+2	+7	mV
Input offset voltage 2	$V_{IO}2$	Comparator 2, when BIAS2 voltage is reversed	–3	–1	+1	mV
Input offset voltage 3	$V_{IO}3$	Total temperature, comparator 2	–5		+3	mV
Input offset current	I_{IO}	Comparators 1, 2		5	50	nA
Input bias current	I_{IB}	Comparators 1, 2	–250	–25		nA
In-phase input voltage range	V_{ICR}	Comparators 1, 2			$V_{CC}2 - 1.5$	V
Input current during negative voltage application	I_{LIM}	Comparators 1, 2 non-reversed input block only, SW3: on	–1.5			mA
[Input pin block] $V_{IN}1^- = 15$ mV, $V_{IN}1^+ = 23$ mV, $V_{IN}2^- = 15$ mV, $V_{IN}2^+ = 23$ mV						
$\overline{\text{CHARGE}}$ pin threshold voltage	V_{CHG-TH}	SW1, 2, 5, 6: When on, BIAS2 voltages are reversed	0.5		1.2	V
$\overline{\text{CHARGE}}$ pin input bias current 1	$I_{CHG-BI}1$	Current during threshold voltage			10	µA
$\overline{\text{CHARGE}}$ pin input bias current 2	$I_{CHG-BI}2$	$V_{\overline{\text{CHARGE}}} = V_{CC}2$	55	70	85	µA
$\overline{\text{CHARGE-INH}}$ pin open voltage	$V_{CH-IN-OP}$	SW1, 2, 5, 6: on		$V_{CC}2$		V
$\overline{\text{CHARGE-INH}}$ pin threshold voltage	$V_{CH-IN-TH}$	SW1, 2, 5, 6: When on, BIAS2 voltages are reversed	0.7		1.3	V
$\overline{\text{CHARGE-INH}}$ pin low-level input current	I_{CH-IN}	SW1, 2, 5, 6: on	–30			µA
BATT/EXT pin open voltage	$V_{BA/EX-OP}$	SW1, 2, 6: on		$V_{CC}2$		V
BATT/EXT pin threshold voltage	$V_{BA/EX-TH}$	SW1, 2, 6: When on, BIAS2 voltages are reversed	1.45		2.05	V
BATT/EXT pin low-level input current	$V_{BA/EX}$	SW1, 2, 5, 6: on	–30			µA

Handling Cautions

Observe precautions when handling these ICs because they are electrostatic sensitive devices.

Pin Assignment



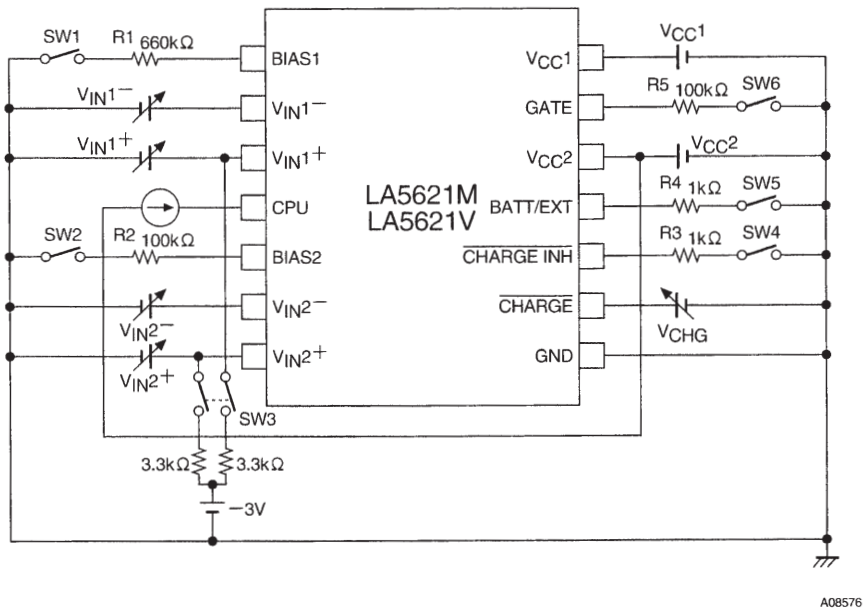


Pin Functions

Pin No.		Pin name	Function
LA5621M	LA5621V		
1	1	BIAS1	Resistor connection pin for setting non-reversed input potential of comparator 1
2	2	$V_{IN}1-$*	Reversed input of comparator 1 (for charge current detection)
3	3	$V_{IN}1+$*	Non-reversed input of comparator 1 (for charge current detection)
4	4	CPU	Microcontroller signal input pin
5	5	BIAS2	Resistor connection pin for setting non-reversed input potential of comparator 2
6	6	$V_{IN}2-$*	Reversed input of comparator 2 (for countercurrent detection when 2 batteries are used)
7	7	$V_{IN}2+$*	Non-reversed input of comparator 2 (for countercurrent detection when 2 batteries are used)
—	8	NC	No connection
—	9	NC	No connection
8	10	GND	Substrate of this IC (Lowest potential)
9	11	$\overline{\text{CHARGE}}$	Charging signal input pin, charge with low
10	12	$\overline{\text{CHARGE INH}}$	Charge prohibition signal input pin, charge prohibition with low (becomes low during discharge mode for lithium-ion battery that set operates on)
11	13	BATT/EXT	On/off control pin of this IC, except Gate block (becomes "Open" during discharge mode for lithium-ion battery that set operates on)
12	14	$V_{CC}2$	Power supply input
13	15	GATE	Gate connection pin of external power MOSFETs
14	16	$V_{CC}1$	Lithium-ion battery + side input pin

Note: * If negative voltage is applied due to countercurrent, etc., up to 1.5 mA can be allowed.

Specified Test Circuit



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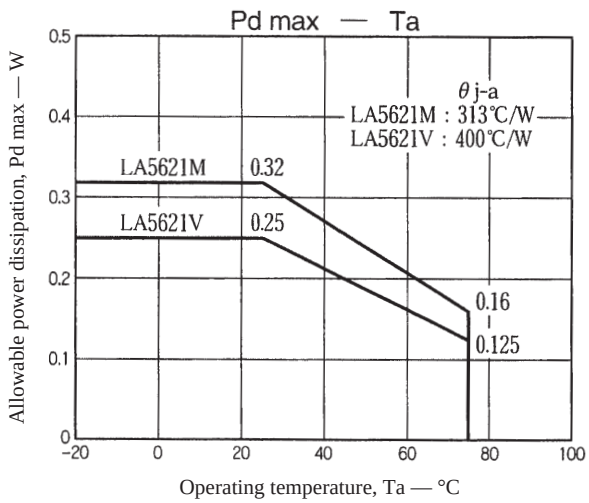
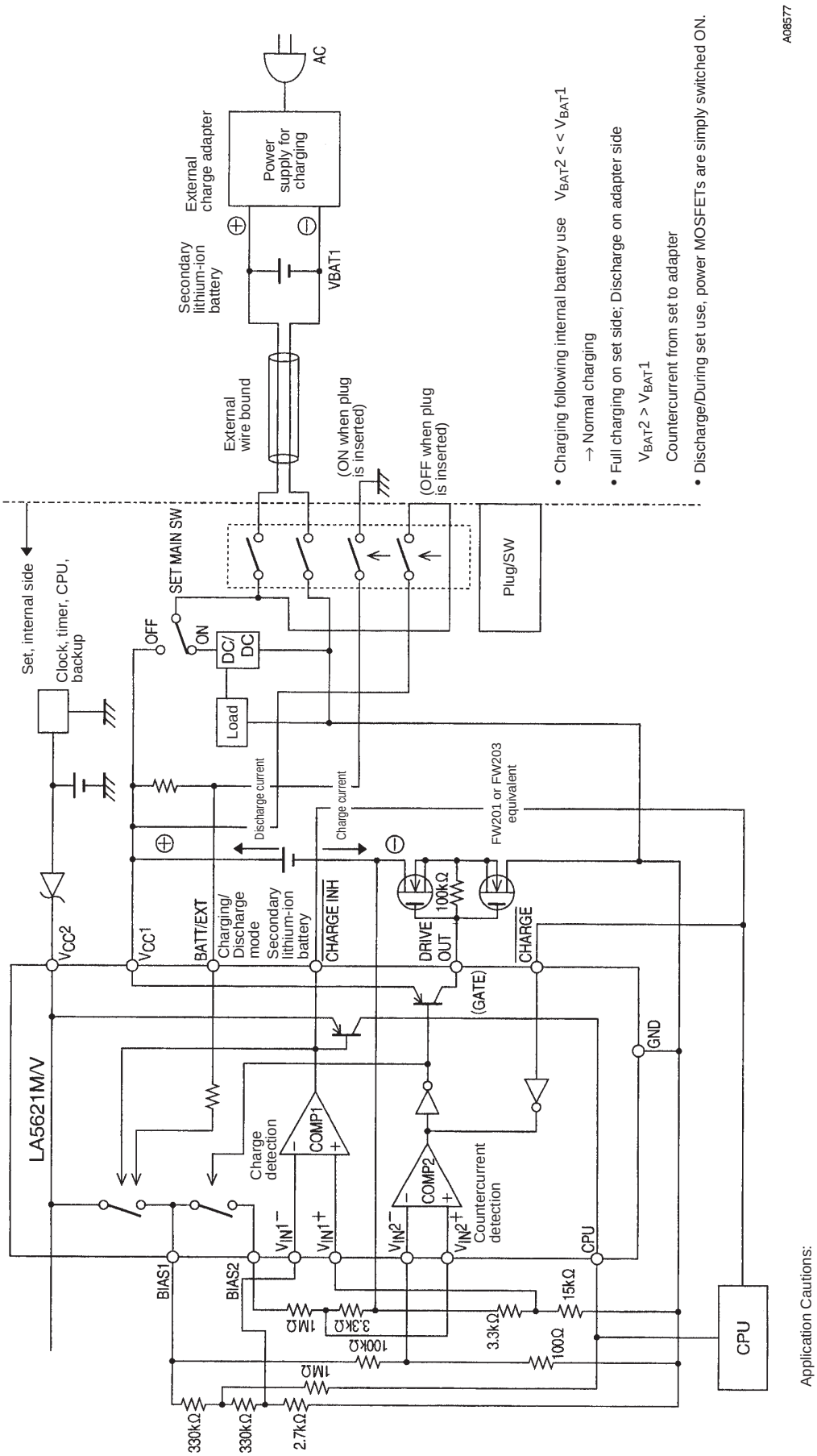


Equivalent Circuit Block and Sample Peripheral Circuit



Application Cautions:

The charging conditions of the secondary battery to be used must be set according to the battery specifications.
The peripheral circuit constants must be set taking into consideration the specifications of the power MOSFETs.
Microcontroller use conditions must be carefully studied.