Ordering number : ENN6519

Monolithic Linear IC

LA5695M

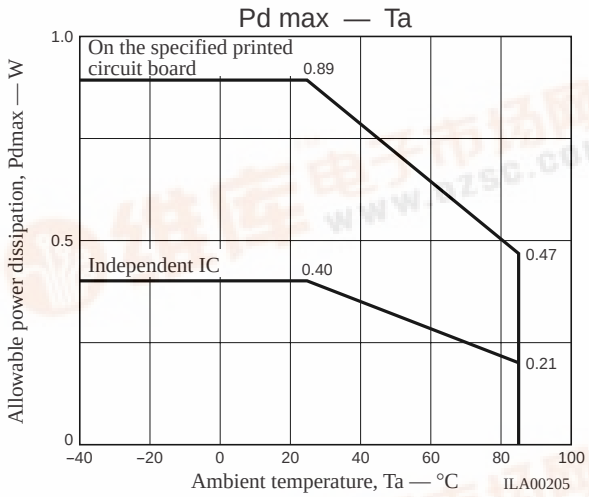
Dual Protection IC for Heating/Cooling and OA Equipment

Overview

The LA5695M is a protection IC for heating/cooling and OA equipment.

Functions

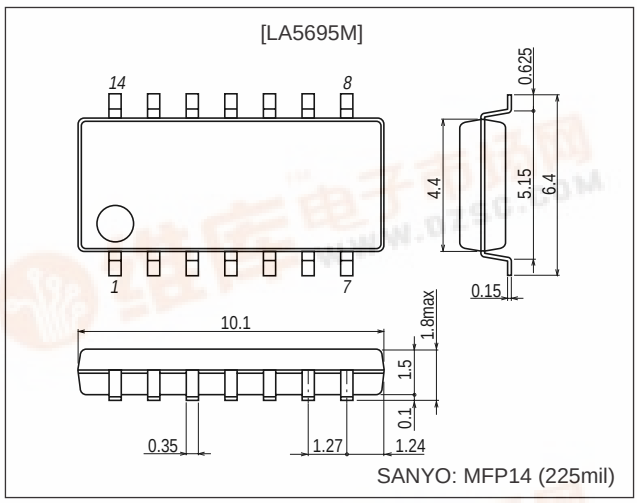
- Supply voltage abnormality detection circuit
- Driver output with built-in output delay circuit
- Can be controlled from 8 input pins.



Package Dimensions

unit: mm

3034A-MFP14



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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		18	V
Maximum output current	I_C max		5	mA
Maximum input voltage	V_{IN} max		18	V
Allowable power dissipation	Pd max	Independent IC, Design guarantee value*	0.4	W
Operating temperature	Topr	Design guarantee value*	–40 to +85	°C
Storage temperature	Tstg	Design guarantee value*	–55 to +150	°C

Note: * The design guarantee values are not measured.

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{CC}		5 ± 0.25	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		3.5	5.0	6.0	V
Output delay time	$T_{DC}1$	With C fixed.	14	15	16	s
Detection frequency setting range	fw C2		0.5		40	Hz
Detection frequency	f C2	With C fixed.		1		Hz
Circuit current	I_{CC}			6.0	10	mA
[VCC Rise/Fall Detection Block]						
Voltage rise detection level	V_{CC}THH		6		7	V
Voltage fall detection level	V_{CC} THL		2.5	3.0	3.5	V
Hysteresis	V_{CC} HYS	When detecting a rising voltage	0.05		1.0	V
	V_{CC} LYS	When detecting a falling voltage	50		200	mV
Minimum operating voltage	V_{CC} LV				2.0	V
[Input Circuits]						
Input pull-up resistor	RPUL IN	IN1, 2, 3, 4, 5, 7, 8	14.0	16.5	19.0	kΩ
High-level input voltage	V_{IN} H		0.7 × V_{CC}		V_{CC}	V
Low-level input voltage	V_{IN} L		–0.3		0.3 × V_{CC}	V
[Test Pin]						
High-level output voltage	V_{TP} H	Pin 11	4.0		V_{CC}	V
Low-level output voltage	V_{TP} L	Pin 11	GND		0.3	V
Output pull-down resistor	RPUL TP	Pin 11 = GND	18.3	21.5	24.8	kΩ
[Output Delay Circuit]						
High-level output voltage	V_{OUT} TH	R_O = 2.2 kΩ	4			V
Low-level output voltage	V_{OUT} L	Pin 14, Output = Low, Isink=2.5 mA			0.4	V
Output sink current	I_O sink	Pin 14, R_O = 2.2 kΩ	1.8			mA
Pin 14 leakage current	I_O leak		0		10	µA
Pin 8 inverted detection voltage	V_{TH8}H		2.3	2.5	2.7	V
Pin 8 hold clear voltage	V_{TH8}L		0.8		1.2	V
Pin 8 voltage (hold state)	V_{8LAT}		4.0		5.1	V
Pin 8 voltage (hold state after a clear operation)	$V_{8ULT}1$		2.5	2.7	2.9	V
Pin 8 voltage (cleared)	$V_{8ULT}2$	Pin 8 = 180 Ω	–0.05		0.1	V
Pin 8 output resistance	$R_{OUT}8$		0.8	1	1.4	kΩ
[Frequency Detection Block]						
Pin 5 high-level input current	I_{IN}5H	Pin 5 = V_{CC}		0	100	µA
Pin 5 high-level input voltage	V_{IN}5H	Pin 5 = open	4.9		5.1	V
Pin 5 low-level input current	I_{IN}5L		146	194	243	µA
Pin 10 high-level voltage	V10H	Pin 5 = GND	4.7		5.1	V
Pin 10 low-level voltage	V10L	Pin 5 = open	–0.1		0.1	V
Pin 10 inverted detection voltage	V_{TH}10		2.3	2.5	2.7	V
Pin 10 source current	I_{10SRC}	Pin 5 = GND	60		110	µA
Pin 10 sink current	I_{10SINK}	Pin 5 = open	140		240	µA

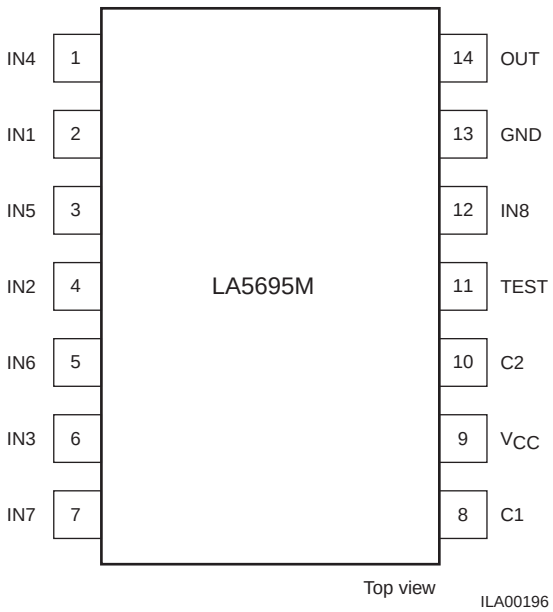
Note: The AC characteristics are target ratings.

Operating Functions Table

IN1	IN2	IN3	IN4	IN5	IN6	IN7	IN8	V_{CC}	OUT
H	H	*	*	*	*	*	*	*	L. .
H	*	H	*	*	*	*	*	*	L. .
*	*	*	H	H	*	*	*	*	L. .
*	*	*	H	*	⊓⊔⊓ !	H	*	*	L. .
*	*	*	H	*	*	*	H	*	L. .
*	*	*	*	*	*	*	*	$V_{CC} \geq 6$ V	L. .
								$V_{CC} \leq 3$ V	L. .
Combinations other than the above									H

Notes: * The level, high or low, of items marked with an asterisk (*) have no influence on the OUT pin.
Example: When both IN1 and IN2 are high, the OUT pin will be low, regardless of other inputs.
! Items marked with an exclamation mark (!) apply when the input pulse frequency (with a 50% duty) is under the set value.
. . Items marked with a double dot (. .) indicate the state after the delay time has elapsed once the input conditions have been met.
OUT indicates the pin 14 output.

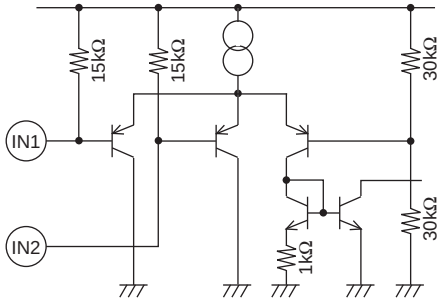
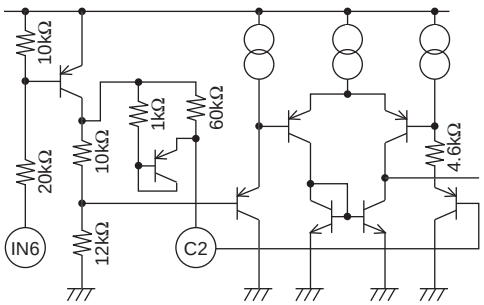
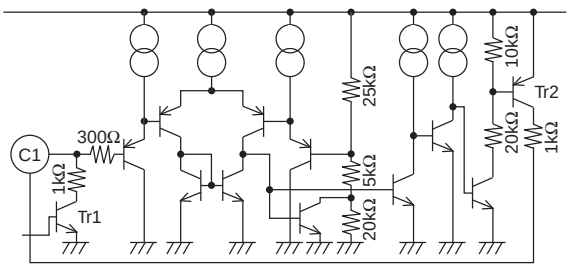
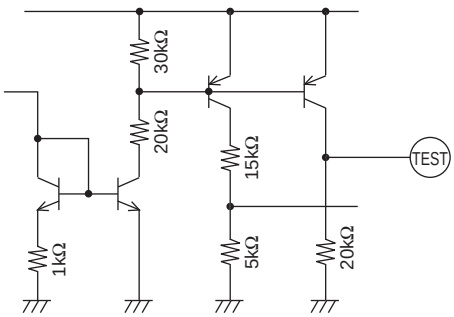
Pin Assignment



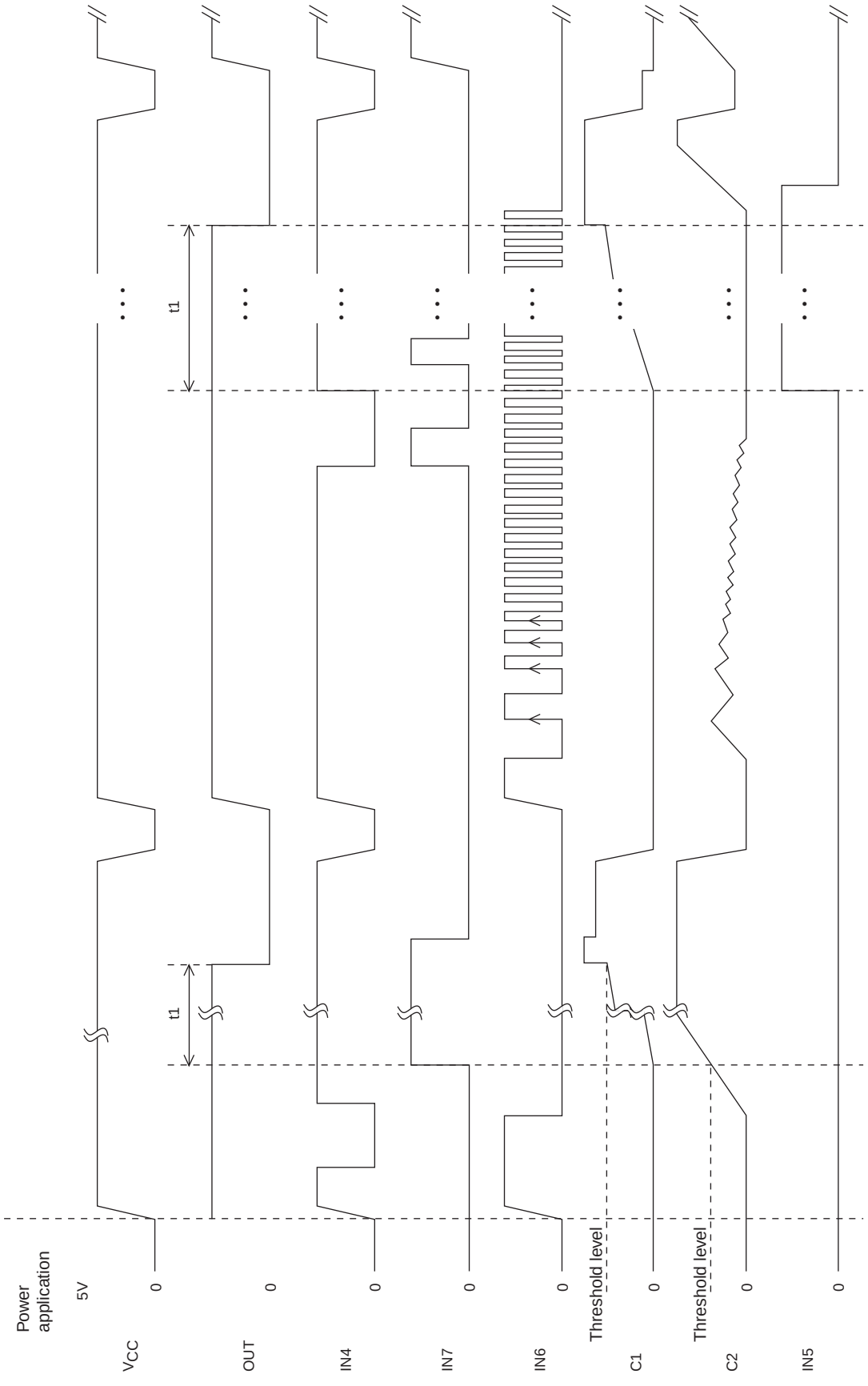
Top view

ILA00196

Pin Functions

Pin No.	Pin name	Description	Equivalent circuit
2 4	IN1 IN2	Input AND and OR block. The pull-up resistance is 15 kΩ.	 ILA00197
2 6	IN1 IN3	These are the same as IN1/IN2.	
1 3	IN4 IN5	These are the same as IN1/IN2.	
1 7	IN4 IN7	These are the same as IN1/IN2.	
1 12	IN4 IN8	These are the same as IN1/IN2.	
5 10	IN6 C2	IN6: pulse waveform input. The trigger waveform is output from the C2 capacitor (0.1 µF).	 ILA00198
8	C1	C1 is pulled up by a 220 kΩ resistor and pulled down by 100 µF capacitor. The comparator switches 15 seconds later at about 1 Hz. Tr1 = 3 S, Tr2 = 13 S	 ILA00199
9	V_{CC}	Any condition other than 3.1 V < V_{CC} < 6.7 V is seen as an abnormal state.	
14	OUT	Output pin	
13	GND	Minimum potential for this IC.	
11	TEST	OR circuit output block. The output is pulled down by a 20 kΩ resistor.	 ILA00200

Timing Chart



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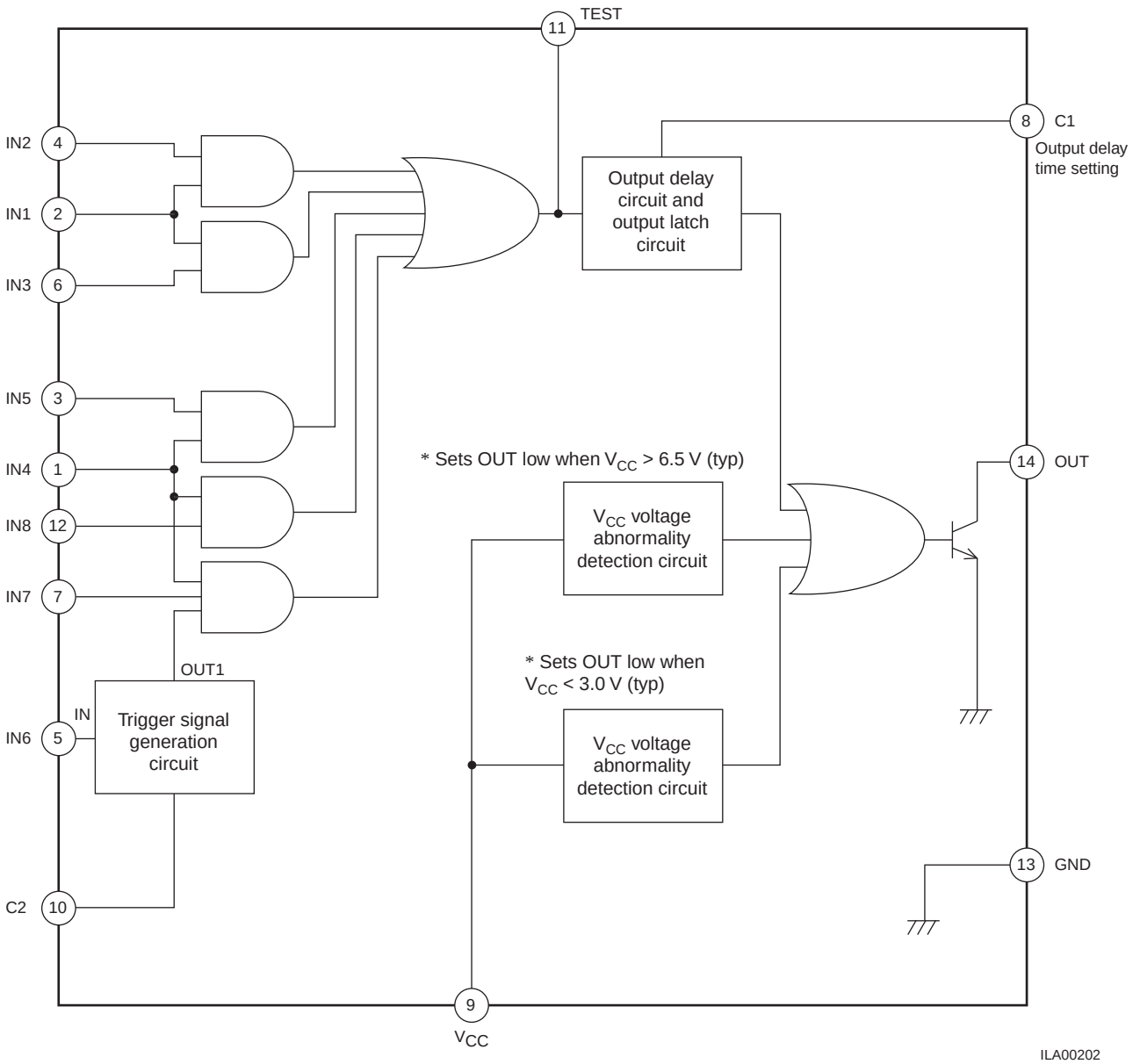
Equivalent Circuit Block Diagram

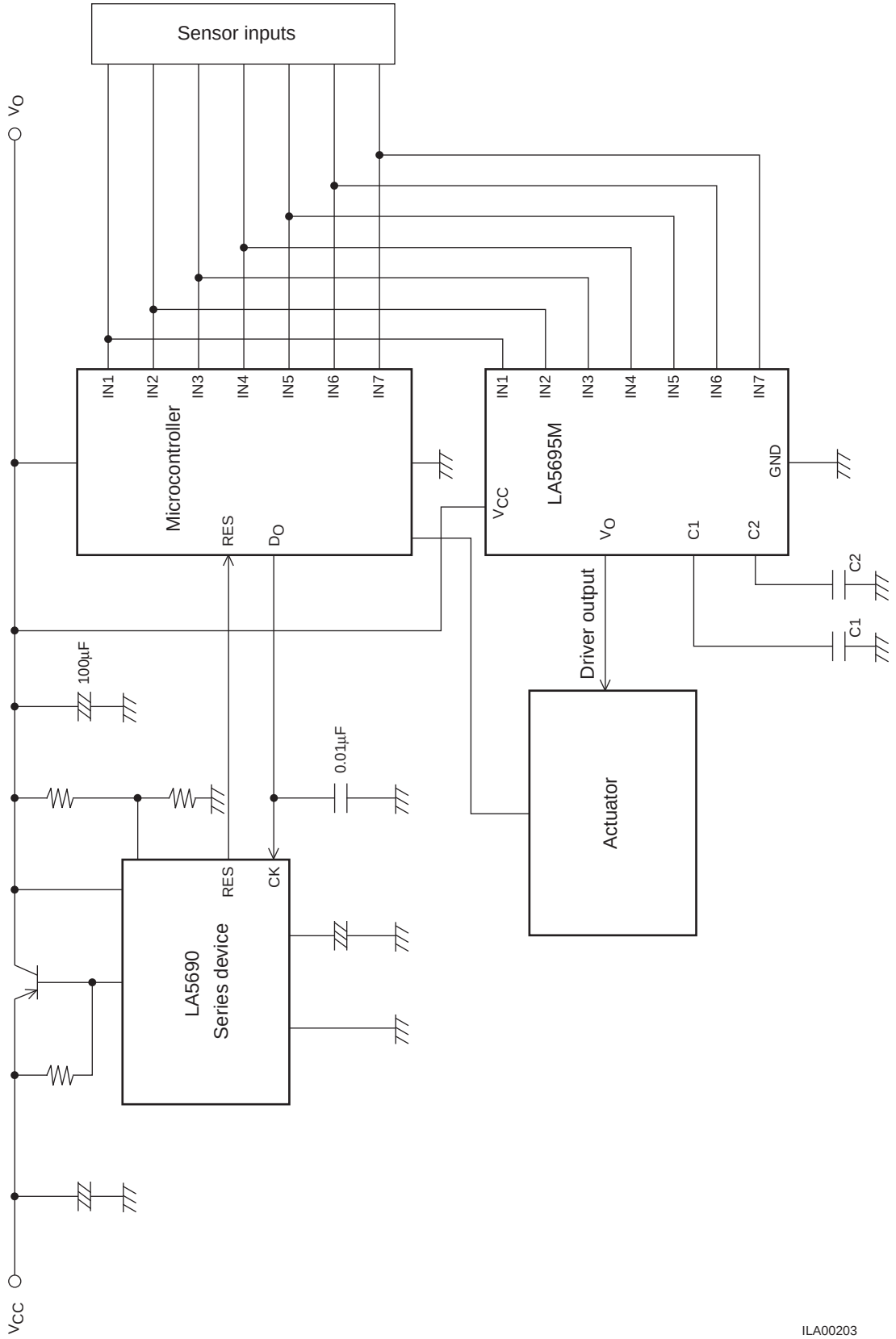


[Trigger signal generation circuit]
When the input pulse (50% duty) is held low or high, OUT1 is set high. At other times, this circuit generates the trigger signal.

[Output delay circuit and output latch circuit]
The OUT pin is set low when the delay time set by the external capacitor (connected to the output delay time setting pin) elapses after the input goes high. Furthermore, once the output goes low, it is held in that state until the power supply is turned off.

[V_{CC} voltage abnormality detection circuit]
These circuits monitor the V_{CC} voltage and set OUT low if the voltage exceeds the set range.

Sample Application Circuit



Test Circuit Diagram