

**LB1817W****FDD Spindle Motor Driver**

Overview

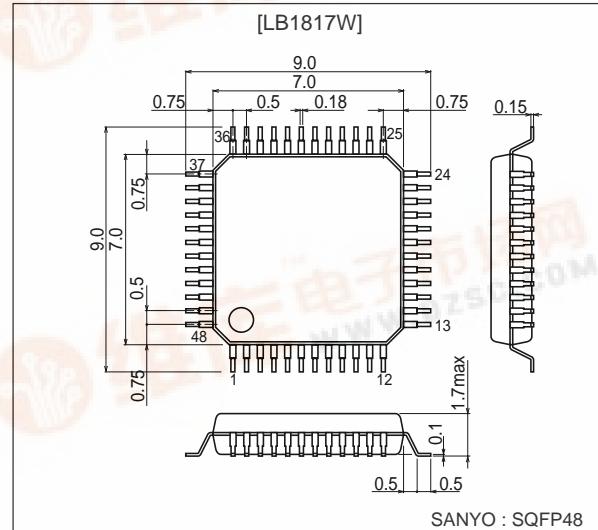
The LB1817W is a spindle motor driver for low-profile floppy disk drives.

Functions and Features

- Three-phase full-wave linear drive (with external PNP transistor)
- Low saturation voltage
- Built-in digital speed control
- Start/stop circuit (Low active)
- Switchable rotation speed
- Current limiter circuit
- Built-in index processing circuit
- Index timing adjustable by VR
- AGC circuit
- Thermal protection circuit

Package Dimensions

unit: mm

3163A-SQFP48

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Maximum output current	I_{CC} max1	$t \leq 0.5\text{s}$	1.5	A
Maximum constant output current	I_O max2		1.0	A
Allowable power dissipation	P_d max1	IC only	0.45	W
Operating temperature	T_{opr}		-20 to +80	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +150	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC}		4.2 to 6.5	V

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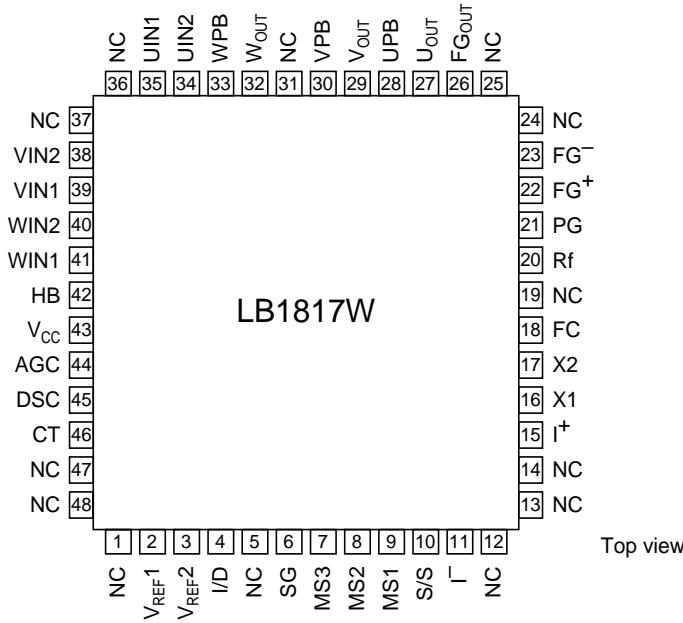
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CC0}	S/S = 5V (Standby)		70	100	μA
	I_{CC}	S/S = 0V (Normal)		25	35	mA
MS1 bias current	I_{MS1}	$V_{MS1} = 5\text{V}$		180	270	μA
MS1 Low input voltage	V_{MS1L}		0.0		0.8	V
MS1 High input voltage	V_{MS1H}			2		V_{CC}
MS2 bias current	I_{MS2}	$V_{MS2} = 5\text{V}$		90	135	μA
MS2 Low input voltage	V_{MS2L}		0.0		0.8	V
MS2 High input voltage	V_{MS2H}			2		V_{CC}
MS3 bias current	I_{MS3}	$V_{MS3} = 5\text{V}$		90	135	μA
MS3 Low input voltage	V_{MS3L}		0.0		0.8	V
MS3 High input voltage	V_{MS3H}			2		V_{CC}
S/S bias current	$I_{S/S}$				20	μA
S/S Low voltage	$V_{S/SL}$		0.0		0.8	V
S/S High voltage	$V_{S/SH}$			2		V_{CC}
Hall amplifier input bias current	I_{HB}				15	μA
Common mode input voltage range	V_h		2.0		$V_{CC}-0.7$	V
Differential input voltage range	V_{dif}			50	200	$\text{mV}_{\text{p-p}}$
Input offset voltage	V_{ho}	*			± 10	mV
Hall bias output voltage	V_H	$I_H = 5\text{ mA}$	0.5	0.8	1.1	V
Leakage current	V_{HL}	S/S = 5V			± 10	μA
Output saturation voltage	$V(\text{sat})$	$I_O = 0.8\text{A}$		0.45	0.64	V
Output leakage current	I_{OL}				1	mA
Current limiter	I_{lim}	$R_F = 3\text{ k}\Omega$, $R_{OUT} = 100\Omega$	6.3	7.5	8.7	mA
Control amplifier voltage gain	G_C		-7.5	-5.5	-3.5	dB
Voltage gain phase differential	ΔG_C				± 1	dB
V/I conversion source current	I^+		19	28	37	μA
V/I conversion sink current	I^-		-19	-28	-37	μA
V/I conversion current ratio	I^+/I^-		0.8	1.0	1.2	
DSC buffer input current	I_{DSC}				1	μA
FG amplifier input voltage	V_{FG}	$f_{FG} = 300\text{ Hz}$	2		20	$\text{mV}_{\text{p-p}}$
FG amplifier voltage gain	G_{FG}	Open loop*		60		dB
FG amplifier input offset	V_{FGO}	*			± 10	mV
FG amplifier internal reference voltage	V_{FGB}		2.2	2.5	2.8	V
FG Schmitt hysteresis width	ΔV_{sh1}	High \rightarrow Low*		25		mV
	ΔV_{sh2}	Low \rightarrow High*		25		mV
Speed discriminator count	N			1390/2		
Discriminator operating frequency	F_D	*			1.1	MHz
Oscillator frequency	F_{OSC}	*			1.1	MHz
Oscillator frequency tolerance	ΔF_{OSC}				± 0.2	$\%$
Index output Low voltage	V_{IDL}	$I_O = 2\text{ mA}$			0.4	V
Index output leakage current	I_{IDL}				± 10	μA
Index amplifier common mode input voltage range	V_I		0.2		$V_{CC}-0.7$	V
Index amplifier differential input voltage range	V_{DIF}	Hysteresis width $< 25\text{ mA}$	25		100	mV
Index amplifier hysteresis set current	I_{HYS}		2.9	4.2	5.5	μA
Timing adjustment at High level	V_{TH}	MS1 = L	1.15	1.26	1.35	V
Timing adjustment at Low level	V_{TL}	MS1 = L	0.40	0.52	0.60	V
Timing adjustment ratio	T_{HL}	V_{TH} (MS1 = L) / V_{TH} (MS1 = H)		1.148		
Reference voltage	V_{REF1}		2.20	2.50	2.80	V
	V_{REF2}		1.85	2.15	2.45	V
Thermal protection operating temperature	T_{SD}	*	150	180		$^\circ\text{C}$
Hysteresis width	ΔT_{SD}	*		10		$^\circ\text{C}$

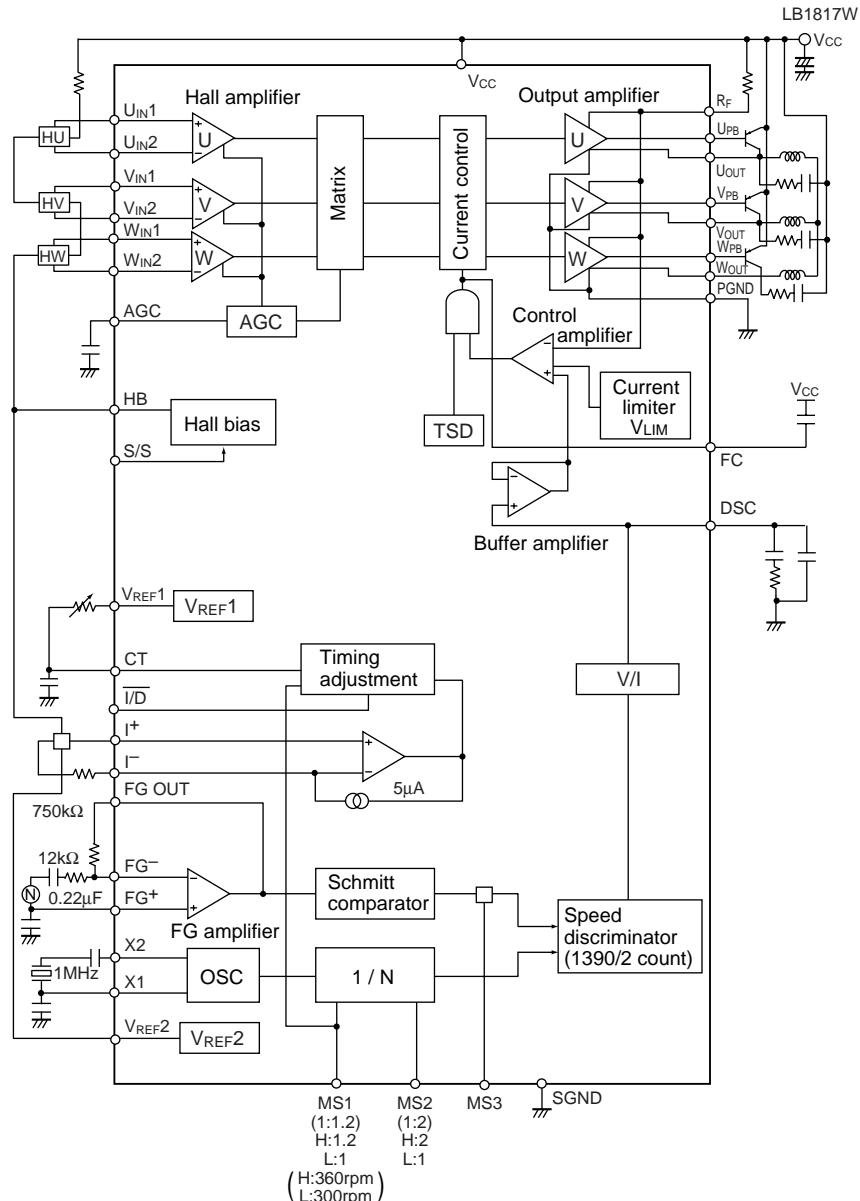
Note: Items shown to be “*” are not measured.

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Pin Assignment



Block Diagram



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Pin Descriptions

Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
1, 5 12, 13 14, 19 24, 25 31, 36 37, 47 48	NC			<ul style="list-style-type: none"> Pins not used
2	V _{REF1}	2.5V typ		<ul style="list-style-type: none"> V_{REF1} pin. Used as power supply for external CR serving for index timing adjustment.
3	V _{REF2}	2.15V typ		<ul style="list-style-type: none"> V_{REF2} pin. Used as bias pin for external index sensor.
4	I/D			<ul style="list-style-type: none"> Index pulse output pin.
6	SG			<ul style="list-style-type: none"> Signal ground pin. Connect to ground together with pin 21.
7	MS3	H: 2.0V min L: 0.8V max		<ul style="list-style-type: none"> FG switching pin. High: FG set to through Low: FG set to 1-stage division
8	MS2	H: 2.0V min L: 0.8V max		<ul style="list-style-type: none"> CLK switching pin. High: Clock set to through Low: Clock set to 1-stage division

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
9	MS1	H: 2.0V min L: 0.8V max		<ul style="list-style-type: none"> Rotation speed switching pin. High: 360 rpm Low: 300 rpm For details, see rotation speed switching table.
10	S/S	H: 2.0V min L: 0.8V max		<ul style="list-style-type: none"> Start/stop switching pin. Low: active
11 15	I ⁻ I ⁺			<ul style="list-style-type: none"> External index – input pin. External index + input pin. When I⁻ pin is High, constant current I1 flows. When pin is Low, constant current I1 is cut off. Resistor externally connected to I⁻ pin determines hysteresis width.
16	X1			<ul style="list-style-type: none"> Reference clock generator pin.
17	X2			
18	FC			<ul style="list-style-type: none"> Frequency characteristics compensation pin. To prevent current control loop oscillation, insert a capacitor between this pin and V_{CC}.

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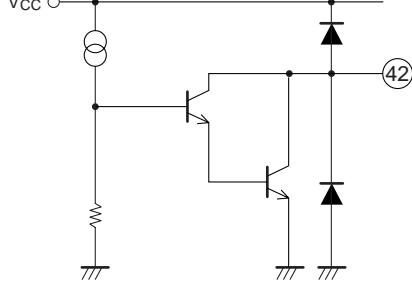
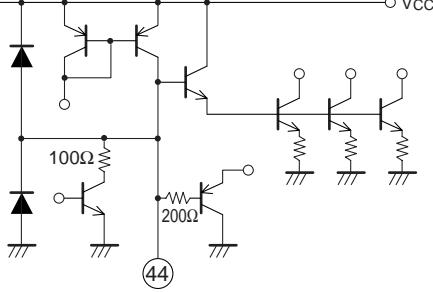
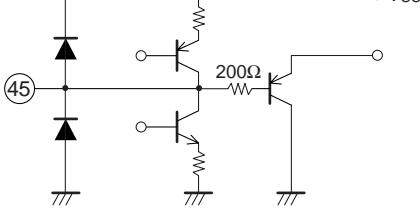
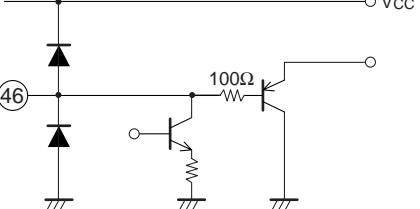
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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
20	RF			<ul style="list-style-type: none"> Output current detection pin. To detect output current as a voltage, insert a resistor R_f between this pin and V_{CC}. The voltage is used for the current limiter. The detection level is about 1/50 of the output current.
21	PG			<ul style="list-style-type: none"> Output transistor ground pin. Connect to ground together with pin 6.
22 23	FG+ FG-	2.5V typ		<ul style="list-style-type: none"> FG amplifier + pin FG amplifier – pin
26	FGout			<ul style="list-style-type: none"> FG amplifier output pin.
27 28 29 30 32 33	UOUT UPB VOUT VPB WOUT WPB			<ul style="list-style-type: none"> U phase output pin. U phase external PNP transistor base connection. V phase output pin. V phase external PNP transistor base connection. W phase output pin. W phase external PNP transistor base connection.
34 35 38 39 40 41	U _{IN} 2 U _{IN} 1 V _{IN} 2 V _{IN} 1 W _{IN} 2 W _{IN} 1			<ul style="list-style-type: none"> U phase Hall input pin. Logic High means $U_{IN1} > U_{IN2}$. V phase Hall input pin. Logic High means $V_{IN1} > V_{IN2}$. W phase Hall input pin. Logic High means $W_{IN1} > W_{IN2}$.

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
42	HB			<ul style="list-style-type: none"> • Hall bias negative-side pin. In stop mode, the pin is open and Hall bias is cut off.
43	V _{CC}			<ul style="list-style-type: none"> • Power supply pin. The voltage supplied to this pin must be stabilized to prevent ripple noise or other noises from inputting to this pin.
44	AGC			<ul style="list-style-type: none"> • AGC pin. Controls the Hall amplifier gain according to Hall input amplitude. An external capacitor is used.
45	DSC			<ul style="list-style-type: none"> • Speed discriminator pin.
46	CT			<ul style="list-style-type: none"> • Timing adjustment pin. External CR for time constant circuit is connected here.

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Truth Table

	Source → Sink	Hall input		
		U	V	W
1	V phase → W phase	H	H	L
2	V phase → U phase	L	H	L
3	W phase → U phase	L	H	H
4	W phase → V phase	L	L	H
5	U phase → V phase	H	L	H
6	U phase → W phase	H	L	L

Hall input pin High means $U_{IN1} > U_{IN2}$

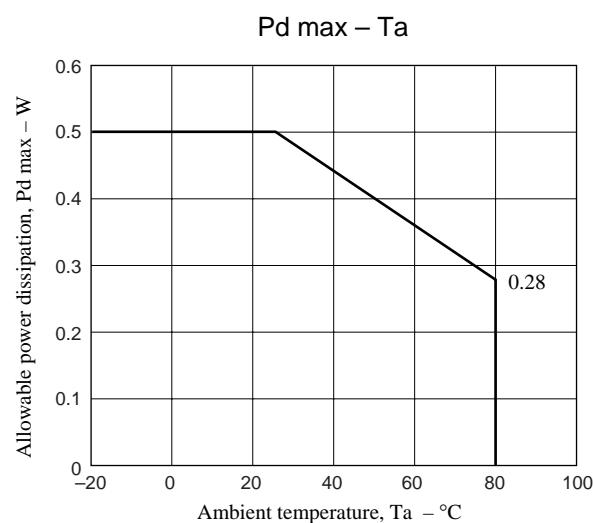
$V_{IN1} > V_{IN2}$

$W_{IN1} > W_{IN2}$

Rotation Speed Select Table

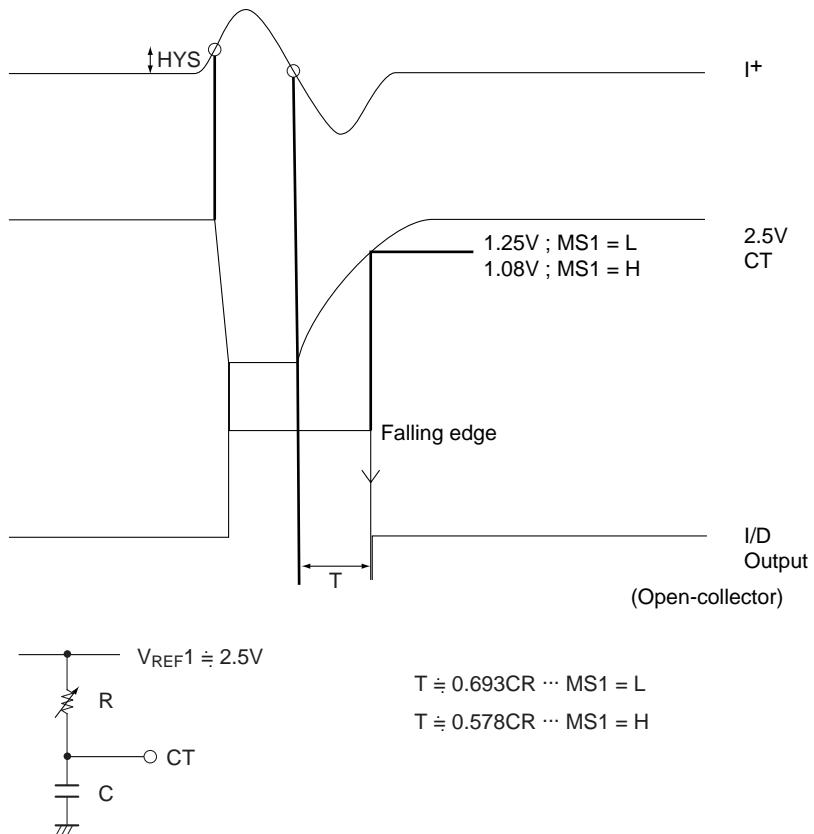
$f_{OSC} = 1 \text{ MHz}$

MS1	H	L	H	L	H	L	H	L
MS2		H		L		H		L
MS3		H		L		L		H
$f_{FG} [\text{Hz}]$	720	600	720	600	1440	1200	360	300



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Index and Timing Chart



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