Ordering number : ENN5805

Monolithic Digital IC

LB1817W

FDD Spindle Motor Driver

Overview

The LB1817W is a spindle motor driver for low-profile floppy disk drives.

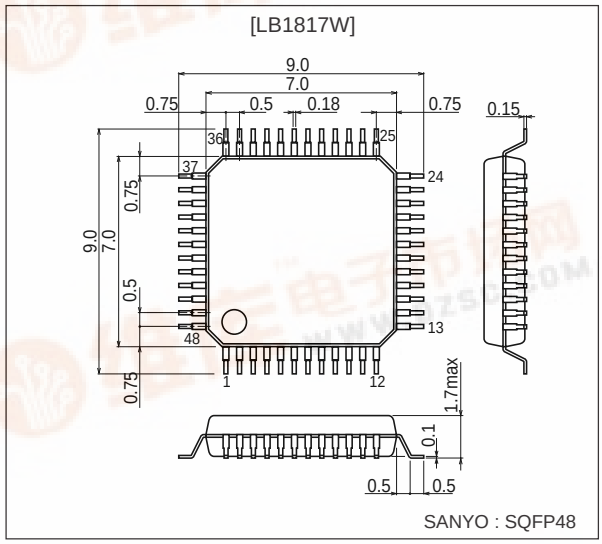
Functions and Features

- Three-phase full-wave linear drive (with external PNP transistor)
- Low saturation voltage
- Built-in digital speed control
- Start/stop circuit (Low active)
- Switchable rotation speed
- Current limiter circuit
- Built-in index processing circuit
- Index timing adjustable by VR
- AGC circuit
- Thermal protection circuit

Package Dimensions

unit: mm

3163A-SQFP48



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Maximum output current	I_{CC} max1	t ≤ 0.5s	1.5	A
Maximum constant output current	I_O max2		1.0	A
Allowable power dissipation	Pd max1	IC only	0.45	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–40 to +150	°C

Allowable Operating Ranges at Ta = 25°C

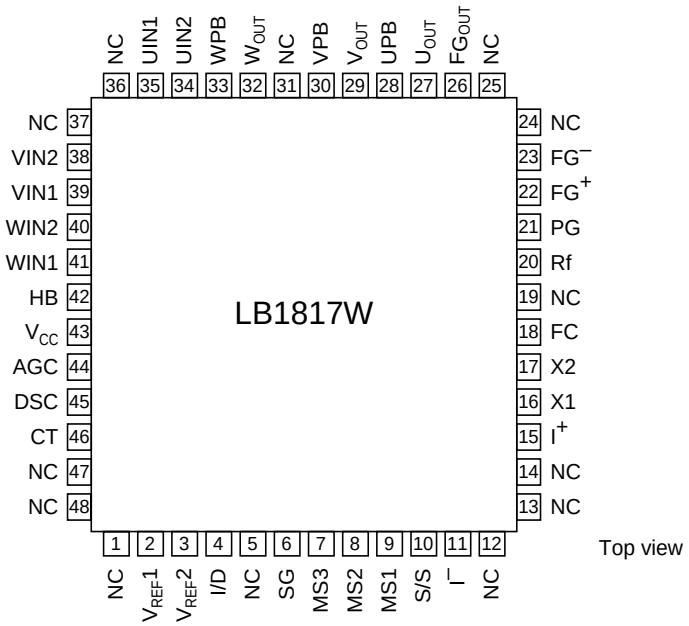
Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{CC}		4.2 to 6.5	V

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{CCO}	S/S = 5V (Standby)		70	100	µA
	I_{CC}	S/S = 0V (Normal)		25	35	mA
MS1 bias current	$I_{MS}1$	$V_{MS}1$ = 5V		180	270	µA
MS1 Low input voltage	$V_{MS}1L$		0.0		0.8	V
MS1 High input voltage	$V_{MS}1H$		2		V_{CC}	V
MS2 bias current	$I_{MS}2$	$V_{MS}2$ = 5V		90	135	µA
MS2 Low input voltage	$V_{MS}2L$		0.0		0.8	V
MS2 High input voltage	$V_{MS}2H$		2		V_{CC}	V
MS3 bias current	$I_{MS}3$	$V_{MS}3$ = 5V		90	135	µA
MS3 Low input voltage	$V_{MS}3L$		0.0		0.8	V
MS3 High input voltage	$V_{MS}3H$		2		V_{CC}	V
S/S bias current	$I_{S/S}$				20	µA
S/S Low voltage	$V_{S/SL}$		0.0		0.8	V
S/S High voltage	$V_{S/SH}$		2		V_{CC}	V
Hall amplifier input bias current	I_{HB}				15	µA
Common mode input voltage range	Vh		2.0		V_{CC}–0.7	V
Differential input voltage range	Vdif		50		200	mVp-p
Input offset voltage	Vho	*			±10	mV
Hall bias output voltage	V_H	I_H = 5 mA	0.5	0.8	1.1	V
Leakage current	V_{HL}	S/S = 5V			±10	µA
Output saturation voltage	V(sat)	I_O = 0.8A		0.45	0.64	V
Output leakage current	I_{OL}				1	mA
Current limiter	I_{lim}	R_F = 3 kΩ, R_{OUT} = 100Ω	6.3	7.5	8.7	mA
Control amplifier voltage gain	G_C		–7.5	–5.5	–3.5	dB
Voltage gain phase differential	ΔG_C				±1	dB
V/I conversion source current	I^+		19	28	37	µA
V/I conversion sink current	I^-		–19	–28	–37	µA
V/I conversion current ratio	I^+/I^-		0.8	1.0	1.2	
DSC buffer input current	I_{DSC}				1	µA
FG amplifier input voltage	V_{FG}	f_{FG} = 300 Hz	2		20	mVp-p
FG amplifier voltage gain	G_{FG}	Open loop*		60		dB
FG amplifier input offset	V_{FGO}	*			±10	mV
FG amplifier internal reference voltage	V_{FGB}		2.2	2.5	2.8	V
FG Schmitt hysteresis width	ΔVsh1	High –> Low*		25		mV
	ΔVsh2	Low –> High*		25		mV
Speed discriminator count	N			1390/2		
Discriminator operating frequency	F_D	*			1.1	MHz
Oscillator frequency	F_{OSC}	*			1.1	MHz
Oscillator frequency tolerance	ΔF_{OSC}				±0.2	%
Index output Low voltage	V_{IDL}	I_O = 2 mA			0.4	V
Index output leakage current	I_{IDL}				±10	µA
Index amplifier common mode input voltage range	V_I		0.2		V_{CC}–0.7	V
Index amplifier differential input voltage range	V_{DIF}	Hysteresis width < 25 mA	25		100	mV
Index amplifier hysteresis set current	I_{HYS}		2.9	4.2	5.5	µA
Timing adjustment at High level	V_{TH}	MS1 = L	1.15	1.26	1.35	V
Timing adjustment at Low level	V_{TL}	MS1 = L	0.40	0.52	0.60	V
Timing adjustment ratio	T_{HL}	V_{TH} (MS1 = L) / V_{TH} (MS1 = H)		1.148		
Reference voltage	$V_{REF}1$		2.20	2.50	2.80	V
	$V_{REF}2$		1.85	2.15	2.45	V
Thermal protection operating temperature	TSD	*	150	180		°C
Hysteresis width	ΔTSD	*		10		°C

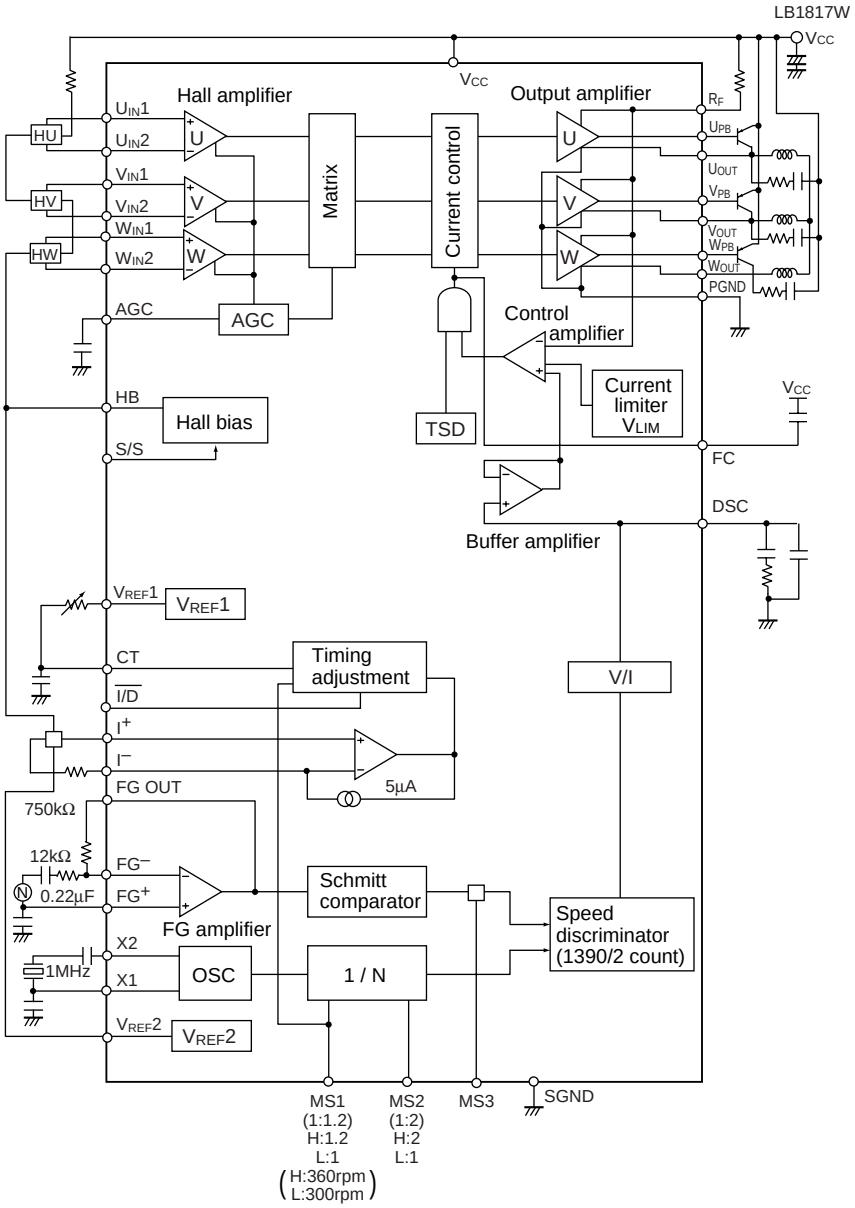
Note: Items shown to be "*" are not measured.

Pin Assignment

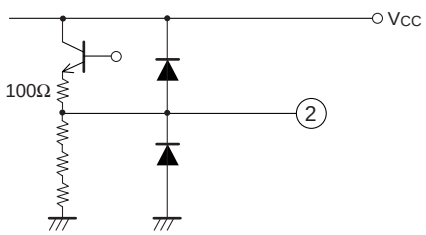
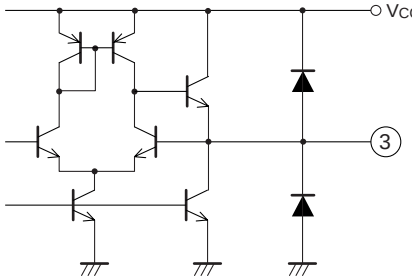
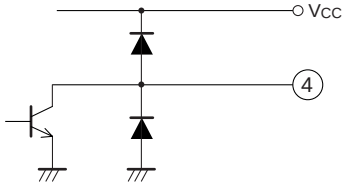
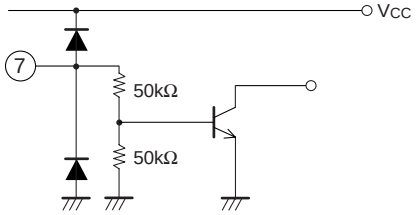
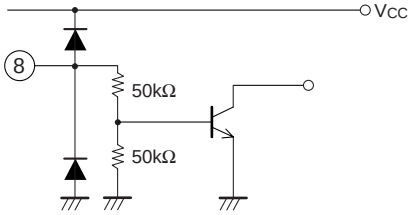


Top view

Block Diagram



Pin Descriptions

Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
1, 5 12, 13 14, 19 24, 25 31, 36 37, 47 48	NC			• Pins not used
2	$V_{REF}1$	2.5V typ		• $V_{REF}1$ pin. Used as power supply for external CR serving for index timing adjustment.
3	$V_{REF}2$	2.15V typ		• $V_{REF}2$ pin. Used as bias pin for external index sensor.
4	I/D			• Index pulse output pin.
6	SG			• Signal ground pin. Connect to ground together with pin 21.
7	MS3	H: 2.0V min L: 0.8V max		• FG switching pin. High: FG set to through Low: FG set to 1-stage division
8	MS2	H: 2.0V min L: 0.8V max		• CLK switching pin. High: Clock set to through Low: Clock set to 1-stage division

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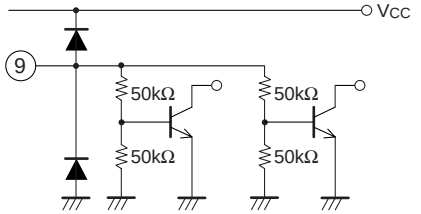
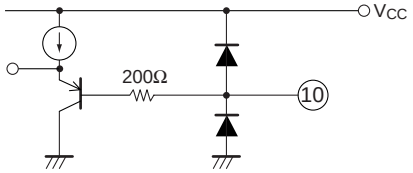
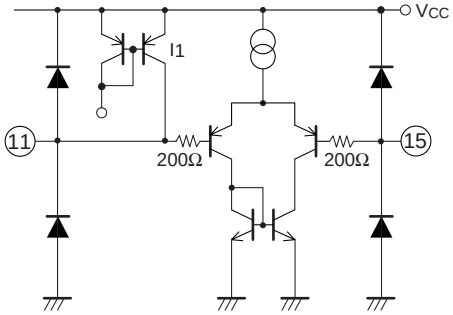
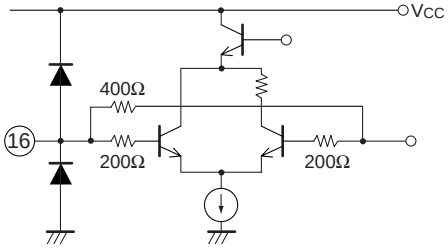
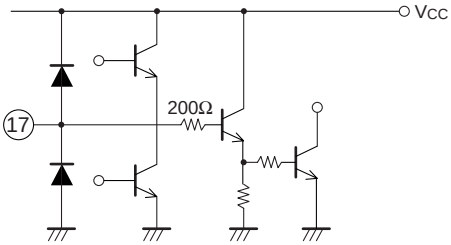
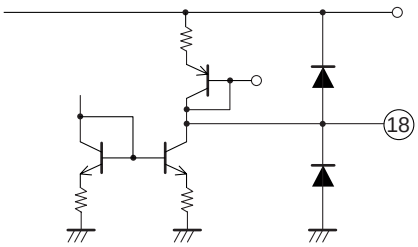
Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
9	MS1	H: 2.0V min L: 0.8V max		• Rotation speed switching pin. High: 360 rpm Low: 300 rpm For details, see rotation speed switching table.
10	S/S	H: 2.0V min L: 0.8V max		• Start/stop switching pin. Low: active
11 15	I⁻ I⁺			• External index – input pin. • External index + input pin. When I⁻ pin is High, constant current I1 flows. When pin is Low, constant current I1 is cut off. Resistor externally connected to I⁻ pin determines hysteresis width.
16	X1			• Reference clock generator pin.
17	X2			
18	FC			• Frequency characteristics compensation pin. To prevent current control loop oscillation, insert a capacitor between this pin and V_{CC}.

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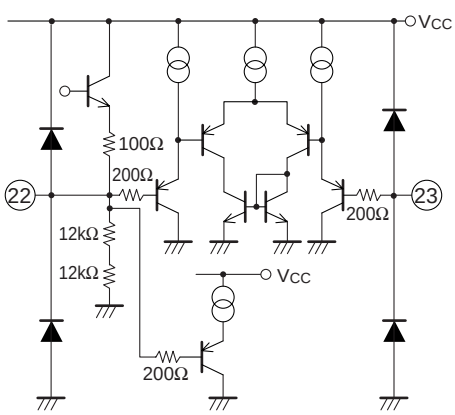
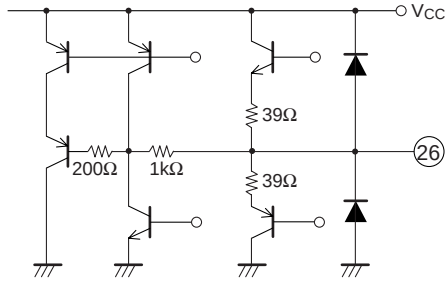
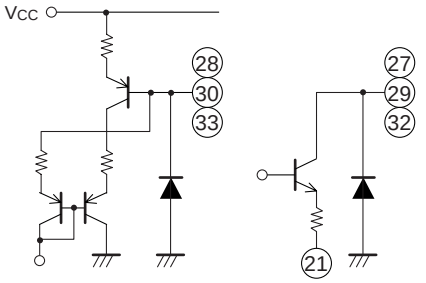
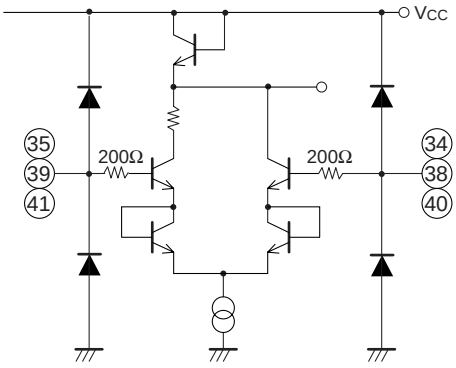
Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
20	RF			• Output current detection pin. To detect output current as a voltage, insert a resistor R_f between this pin and V_{CC}. The voltage is used for the current limiter. The detection level is about 1/50 of the output current.
21	PG			• Output transistor ground pin. Connect to ground together with pin 6.
22 23	FG^+ FG^-	2.5V typ		• FG amplifier + pin • FG amplifier – pin
26	FGout			• FG amplifier output pin.
27 28 29 30 32 33	U_{OUT} U_{PB} V_{OUT} V_{PB} W_{OUT} W_{PB}			• U phase output pin. • U phase external PNP transistor base connection. • V phase output pin. • V phase external PNP transistor base connection. • W phase output pin. • W phase external PNP transistor base connection.
34 35 38 39 40 41	$U_{IN}2$ $U_{IN}1$ $V_{IN}2$ $V_{IN}1$ $W_{IN}2$ $W_{IN}1$			• U phase Hall input pin. Logic High means $U_{IN}1 > U_{IN}2$. • V phase Hall input pin. Logic High means $V_{IN}1 > V_{IN}2$. • W phase Hall input pin. Logic High means $W_{IN}1 > W_{IN}2$.

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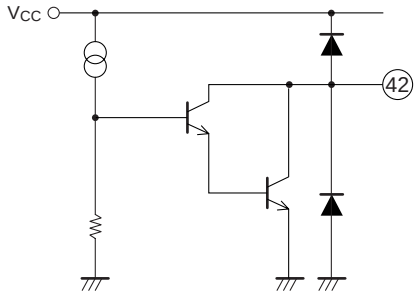
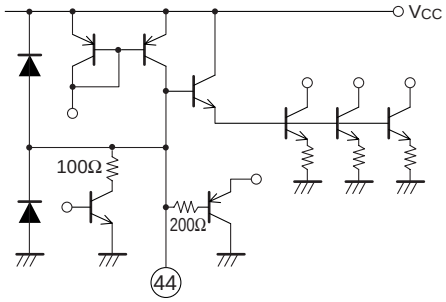
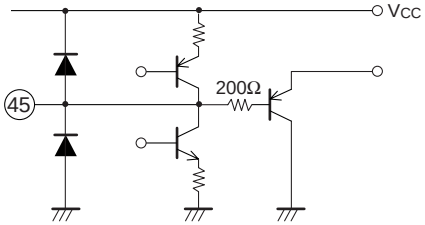
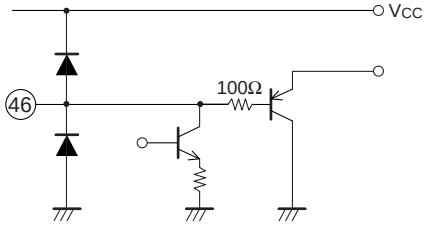
Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
42	HB			• Hall bias negative-side pin. In stop mode, the pin is open and Hall bias is cut off.
43	V_{CC}			• Power supply pin. The voltage supplied to this pin must be stabilized to prevent ripple noise or other noises from inputting to this pin.
44	AGC			• AGC pin. Controls the Hall amplifier gain according to Hall input amplitude. An external capacitor is used.
45	DSC			• Speed discriminator pin.
46	CT			• Timing adjustment pin. External CR for time constant circuit is connected here.

Truth Table

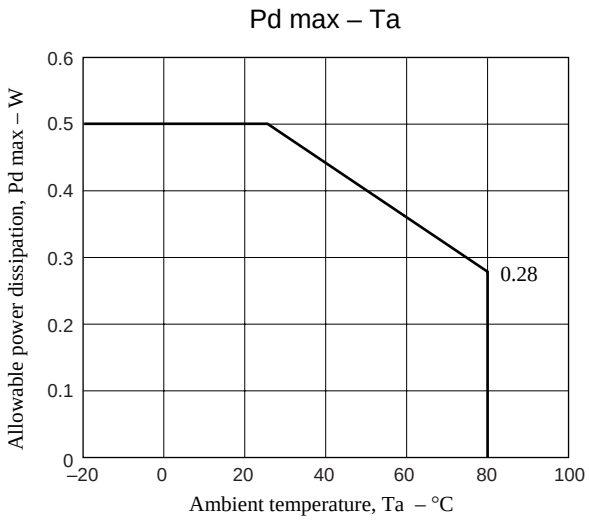
	Source –> Sink	Hall input		
		U	V	W
1	V phase –> W phase	H	H	L
2	V phase –> U phase	L	H	L
3	W phase –> U phase	L	H	H
4	W phase –> V phase	L	L	H
5	U phase –> V phase	H	L	H
6	U phase –> W phase	H	L	L

Hall input pin High means $U_{IN}1 > U_{IN}2$
$V_{IN}1 > V_{IN}2$
$W_{IN}1 > W_{IN}2$

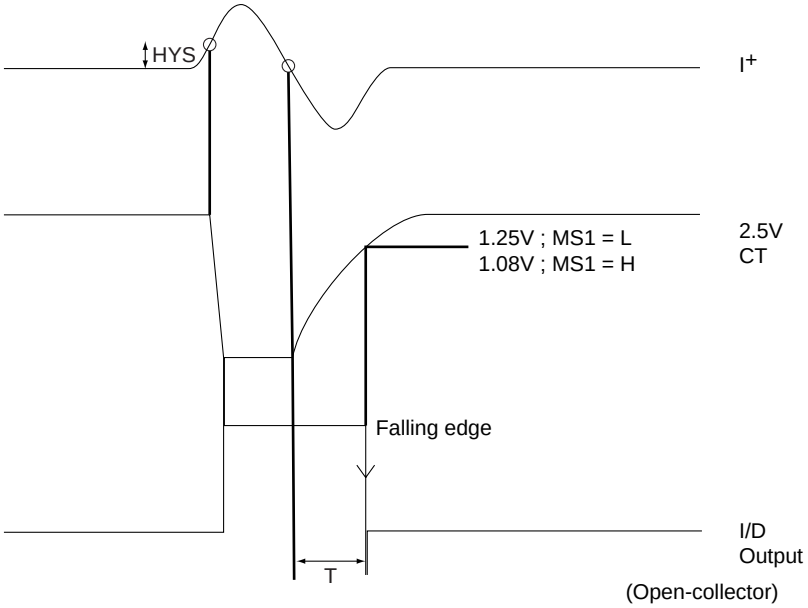
Rotation Speed Select Table

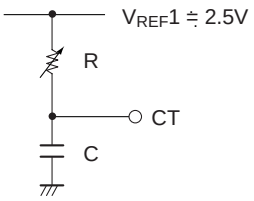
f_{OSC} = 1 MHz

MS1	H	L	H	L	H	L	H	L
MS2	H		L		H		L	
MS3	H		L		L		H	
f_{FG} [Hz]	720	600	720	600	1440	1200	360	300



Index and Timing Chart





T ≒ 0.693CR ··· MS1 = L

T ≒ 0.578CR ··· MS1 = H