Ordering number: ENN6198A

Monolithic Digital IC



## LB1928

# Three-Phase Brushless Motor Driver for Office Automation Equipment

### Overview

The LB1928 is a 3-phase brushless motor driver well suited for drum and paper feed motors in laser printers, plain-paper copiers and other office automation equipment. Direct PWM drive allows control with low power losses. Peripheral circuitry including speed control circuit and FG amplifier is integrated, thus allows drive circuit to be constructed with a single chip.

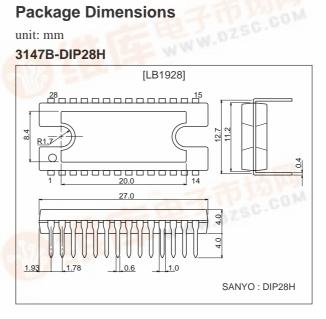
### **Functions and Features**

- Three-phase bipolar drive (30V, 3.1A)
- Direct PWM drive technique
- · Built-in diode for absorbing output lower-side kickback
- · Speed discriminator and PLL speed control
- Speed lock detection output
- Built-in forward/reverse switching circuit
- Built-in protection circuitry includes current limiter, overheat protection, motor restraint protection, etc.

## **Package Dimensions**

unit: mm

#### 3147B-DIP28H



## **Specifications**

### Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	Vcc max	-1 Rd Sall(0) ==	30	V
Maximum output current	I <sub>O</sub> max	T ≤ 500 ms	3.1	Α
Allowable power dissipation 1	Pd max 1	IC only	3	W
Allowable power dissipation 2	Pd max 2	With an arbitrary large heat sink	20	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

## Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage range 1	Vcc		9.5 to 28	V
Regulator voltage output current	I <sub>REG</sub>	100071-21	0 to -20	mA
LD output current	I <sub>LD</sub>	151 9/1/0	0 to 15	mA

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## LB1928

## Electrical Characteristics at $Ta = 25^{\circ}C$ , Vcc = VM = 24V

				Ratings		
Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply current 1	Icc1			23	30	mA
Power supply current 2	ly current 2 Icc2 In STOP mode				5	mA
[Output block]						
Output saturation voltage 1	Vosat1	lo = 1.0A, Vo(SINK) + Vo(SOURCE)		2.0	2.5	V
Output saturation voltage 2	Vosat2	Io = 2.0A, Vo(SINK) + Vo(SOURCE)		2.6	3.2	V
Output leak current	Ioleak				100	μΑ
Lower-side diode forward voltage 1	V <sub>D</sub> 1	$I_{D} = -1.0A$		1.2	1.5	· V
Lower-side diode forward voltage 2	V <sub>D</sub> 2	$I_{D} = -2.0A$		1.5	2.0	V
[5V regulator voltage output]						
Output voltage	V <sub>REG</sub>	lo = -5 mA	4.65	5.00	5.35	V
Voltage fluctuation	ΔV <sub>REG</sub> 1	Vcc = 9.5 to 28V		30	100	mV
Load fluctuation	ΔV <sub>REG</sub> 2	Io = -5 to -20 mA		20	100	mV
[Hall amplifier]	INLO					
Input bias current	I <sub>HB</sub>		-2	-0.5		μΑ
					V <sub>REG</sub>	-
Common mode input voltage range	V <sub>ICM</sub>		1.5		-1.5	V
Hall input sensitivity			80			mVp-p
Hysteresis width	$\Delta V_{IN}$		15	24	42	mV
Input voltage L -> H	V <sub>SLH</sub>			12		mV
Input voltage H-> L	V <sub>SHL</sub>			-12		mV
[PWM oscillator]	,					
Output High level voltage	V <sub>OH(PWM)</sub>		2.5	2.8	3.1	V
Output Low level voltage	V <sub>OL(PWM)</sub>		1.2	1.5	1.8	V
Oscillator frequency	f <sub>(PWM)</sub>	C = 3900 pF		18		kHz
Amplitude	V <sub>(PWM)</sub>		1.05	1.30	1.55	Vp-p
[CSD circuit]	(1 *****)		<u> </u>			
Operating voltage	V <sub>OH(CSD)</sub>		3.6	3.9	4.2	V
External capacitance charge current	I <sub>CHG</sub>		-17	-12	-9	μΑ
Operating time	t <sub>(CSD)</sub>	C = 10 μF Design target value		3.3		s
[Current limiter operation]	(СОД)	, , ,				
Limiter	$V_{RF}$	V <sub>CC</sub> -VM	0.45	0.5	0.55	V
[Thermal shutdown operation]	IXI					
Thermal shutdown operating temperature	TSD	Design target value (junction temperature)	150	180		°C
Hysteresis width	ΔTSD	Design target value (junction temperature)		50		°C
[FG amplifier]						
Input offset voltage	V <sub>IO(FG)</sub>		-10		+10	mA
Input bias current	I <sub>B(FG)</sub>		-1		+1	μΑ
			V <sub>REG</sub>	V <sub>REG</sub>		
Output High level voltage	V <sub>OH(FG)</sub>	$I_{FGO} = -0.2 \text{ mA}$	-1.2	-0.8		V
Output Low level voltage	V <sub>OL(FG)</sub>	I <sub>FGO</sub> = 0.2 mA		0.8	1.2	V
FG input sensitivity		Gain 100 times	3			mV
Next-stage Schmitt comparator width		Design target value	100	180	250	mV
Operating frequency range					2	kHz
Open-loop gain		f(FG) = 2 kHz	45	51		dB
[Speed discriminator]						
Output High level voltage	V	$I_{DO} = -0.1 \text{ mA}$	V <sub>REG</sub>	V <sub>REG</sub> -0.7		V
, ,	V <sub>OH(D)</sub>		-1.0			
Output Low level voltage	V <sub>OL(D)</sub>	I <sub>DO</sub> = 0.1 mA		0.8	1.1	V
Count number				512		
[PLL output]			1 1/			
Output High level voltage	V <sub>OH(P)</sub>	$I_{PO} = -0.1 \text{ mA}$	V <sub>REG</sub> -1.8	V <sub>REG</sub> −1.5	V <sub>REG</sub> –1.2	V
Output Low level voltage	V <sub>OL(P)</sub>	I <sub>PO</sub> = 0.1 mA	1.2	1.5	1.8	V
[Lock detection]	L OL(P)	110				-
1r						
Output Low level voltage	VOLUEN	$I_{LD} = 10 \text{ mA}$		0.15	0.51	V
Output Low level voltage Lock range	V <sub>OL(LD)</sub>	I <sub>LD</sub> = 10 mA		0.15 6.25	0.5	V 

## LB1928

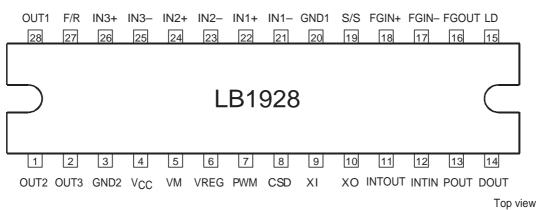
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Damamatan	Coursels al	Conditions	Ratings			l limit
Parameter	Symbol	Symbol		typ	max	Unit
[Integrator]			•			
Input bias current	I <sub>B(INT)</sub>		-0.4		+0.4	μΑ
Output High level voltage	V <sub>OH(INT)</sub>	I <sub>INTO</sub> = -0.2 mA	V <sub>REG</sub> –1.2	V <sub>REG</sub> -0.8		V
Output Low level voltage	V <sub>OL(INT)</sub>	I <sub>INTO</sub> = 0.2 mA		0.8	1.2	V
Open-loop gain		f(INT) = 1 kHz	45	51		dB
Gain bandwidth product		Design target value		450		kHz
Reference voltage		Design target value	-5%	V <sub>REG</sub> /2	5%	V
[Crystal oscillator]						
Operating frequency range	fOSC		3		10	MHz
Low level pin voltage	V <sub>OSCL</sub>	$I_{OSC} = -0.5 \text{ mA}$		1.65		V
High level pin current	I <sub>OSCH</sub>	$V_{OSC} = V_{OSCL} + 0.3V$		0.4		mA
[Start/stop pin]						
High level input voltage range	V <sub>IH(S/S)</sub>		3.5		$V_{REG}$	V
Low level input voltage range	V <sub>IL(S/S)</sub>		0		1.5	V
Input open voltage	V <sub>IO(S/S)</sub>		V <sub>REG</sub> -0.5		V <sub>REG</sub>	V
Hysteresis width	ΔV <sub>IN</sub>		0.35	0.50	0.65	V
High level input current	I <sub>IH(S/S)</sub>	$V_{(S/S)} = V_{REG}$	-10	0	10	μΑ
Low level input current	I <sub>IL(S/S)</sub>	$V_{(S/S)} = 0V$	-280	-210		μΑ
[Forward/reverse pin]			•			
High level input voltage range	V <sub>IH(F/R)</sub>		3.5		V <sub>REG</sub>	V
Low level input voltage range	V <sub>IL(F/R)</sub>		0		1.5	V
Input open voltage	V <sub>IO(F/R)</sub>		V <sub>REG</sub> -0.5		V <sub>REG</sub>	V
Hysteresis width	ΔV <sub>IN</sub>		0.35	0.50	0.65	V
High level input current	I <sub>IH(F/R)</sub>	$V_{(F/R)} = V_{REG}$	-10	0	+10	μΑ
Low level input current	I <sub>IL(F/R)</sub>	$V_{(F/R)} = 0V$	-280	-210		μΑ

#### **Truth Table**

	Source	F/R = "L"			F/R = "H"		
	Sink	IN1	IN2	IN3	IN1	IN2	IN3
1	OUT2 -> OUT1	Н	L	Н	L	Н	L
2	OUT3 -> OUT1	Н	L	L	L	Н	Н
3	OUT3 -> OUT2	Н	Н	L	L	L	Н
4	OUT1 -> OUT2	L	Н	L	Н	L	Н
5	OUT1 -> OUT3	L	Н	Н	Н	L	L
6	OUT2 -> OUT3	L	L	Н	Н	Н	L

## **Pin Assignment**



Pd max – Ta

With an arbitrary large heat sink

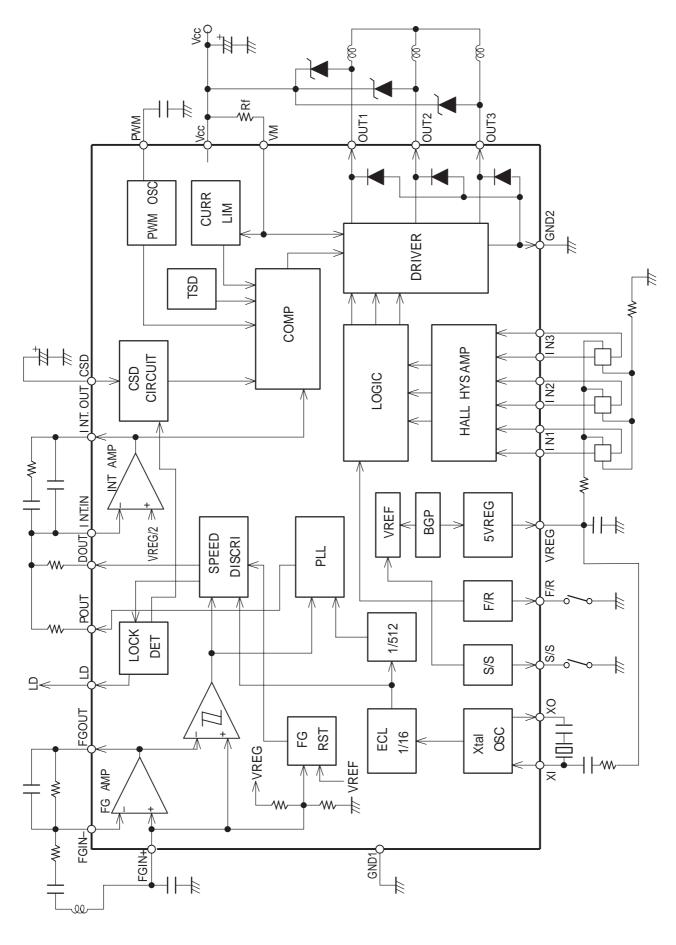
Without heat sink

Without heat sink

Ambient temperature, Ta – °C

Relationship between crystal oscillator frequency fosc and FG frequency fFG is as follows.  $fFG (servo) = fosc/ (ECL \ divide-by-16 \times count \ number)$  = fosc/8192

## **Equivalent Circuit Block Diagram**



## **Pin Description**

Pin Descr	iption		
Pin number	Pin name	Equivalent circuit	Pin function
28	OUT1	V	Motor drive output pins.
1	OUT2	V <sub>CC</sub> , 300Ω , VM	Connect a Schottky diode between these
2	OUT3	30002 VM 5	outputs and V <sub>CC</sub> .
3	GND2		Output ground pin.
5	VM		Output block power supply and output
		\(\psi\)	current detection pin.
		<i>#</i> 1 2 28	Connect a resistor (Rf) between this pin and
			$V_{CC}$ to detect the output current as a voltage.
			The output current is limited according to the
		<b> </b>	-
		(3) A12983	equation I <sub>OUT</sub> = VRF/Rf.
4	V		Power supply pin (except for output block)
6	V <sub>CC</sub> VREG	V	
6	VKEG	Vcc	Regulated power supply output pin (5V
			output)
		<b>├ ★</b>	Connect a capacitor (approx. 0.1 µF) between
		<b>*</b>	this pin and ground to stabilize the output.
		6	
		<b>↓ ♦</b>	
		777 A12984	
7	PWM		DWM fra muse and action or rice
/	PVVIVI	VREG	PWM frequency setting pin.
		$ $ $\psi$ $\psi$ $\psi$ $ $	Connect a capacitor between this pin and
			ground.
			C = 3900 pF results in a frequency of about 18 kHz.
		200Ω (7)	IO KIIZ.
		777 777 777 A12985	
8	CSD	VREG	Lock protection circuit operation time
	OOD		setting pin.
			Connecting a capacitor of about 10 µF
			between this pin and ground results in a
		300Ω	protection circuit operation time of about 3.3
		1κΩ \$ 8	i
			seconds.
		11 11 11 11 11 A12986	
9	ΧI		Quartz oscillator pins.
	XO	VREG.	-
10	ΛU		Connect to quartz oscillator to generate the reference clock.
			When an external clock (of several MHz) is
			used, the clock signal should be input via a
		<b>Y</b> -W-10	resistor of about 5.1 k $\Omega$ connected in series
		<b>V</b> (9)	with the XI pin. In this case, the XO pin must
			be left open.
		11 11 11 A12987	

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Pin number	Pin name	Equivalent circuit	Pin function
11	INT	VREG	Integrator output pin (speed control pin)
	OUT	PWM comparator	
12	INT IN	VREG 300Ω 12 A12989	Integrator input pin.
13	POUT	VREG 300Ω 13	PLL output pin.
14	DOUT	VREG 300Ω 14 A12991	Speed discriminator output pin. Acceleration: High, Deceleration: Low
15	LD	VREG (15)  A12992	Speed lock detection pin.  When motor rotation is within lock range (±6.25%): Low  Withstand voltage: 30V max.

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Pin number	Pin name	Equivalent circuit	Pin function					
16	FG OUT	VREG  16  FG schmitt comparator  A12993	FG amplifier output pin.					
17	FGIN-	VREG	FG amplifier input pin.					
18	FGIN+	FG reset circuit $\frac{300\Omega}{18}$ $\frac{300\Omega}{17}$ $\frac{17}{17}$ $\frac{300\Omega}{17}$ $\frac{17}{17}$	By connecting a capacitor (approx. $0.1~\mu F$ ) between FGIN+ and ground, the logic circuitry is reset.					
19	S/S	VREG  S N N N N N N N N N N N N N N N N N N	Start/stop control pin. Start (Low): 0V to 1.5V Stop (High): 3.5V to VREG High when open. Hysteresis width: approx. 0.5V.					
20	GND1		Ground pin (except for output block).					
22 21 24 23 26 25	IN1+ IN1- IN2+ IN2- IN3+ IN3-	VREG  21 (23) (25) 300Ω  W (22) (24) (26)  A12996	Hall input pins. High when IN+ > IN-, Low when IN+ < IN Hall signal should have an amplitude of at least 100 mVp-p (differential operation). When Hall signal noise is a problem, connect a capacitor between IN+ and IN					
27	F/R	VREG 2kΩ 27 A12997	Forward/reverse control pin. Forward (Low): 0V to 1.5V Reverse (High): 3.5V to VREG High when open. Hysteresis width: approx. 0.5V.					

#### **Description of the LB1928**

### 1. Speed control circuit

The IC performs speed control through combined use of a speed discrimination circuit and PLL circuit. The speed control circuit counts FG cycles and outputs a deviation signal every 2 FG cycles. The PLL circuit outputs a phase deviation signal every FG cycle.

The FG servo frequency is determined by the following equation. The motor rotation speed is set by the number of FG pulses and the crystal oscillator frequency.

fFG (servo) = fOSC/8192

fOSC: Crystal oscillator frequency

#### 2. Output drive circuit

In order to reduce power loss at the output, the LB1928 uses the PWM drive technique. While ON, the output transistors are always saturated, and motor drive power is adjusted by varying the output ON duty ratio. Because output PWM switching is performed by the lower-side output transistor, a Schottky diode must be connected between OUT and  $V_{CC}$ . (If the reverse recovery time of the diode is too long, a feedthrough current will flow at the instant when the lower-side transistor goes ON.) An internal diode is provided between OUT and GND. If large output current causes a problem (waveform distortion during lower-side kickback, etc.), an external rectifying diode or Schottky diode should be connected.

The output diode is integrated only on the lower side.

## 3. Current limiting circuit

The current limiting circuit limits the peak current to the value I = VRF/Rf (VRF = 0.5 V typ., Rf: current detector resistance). Current limiting is achieved by reducing the ON duty ratio of the output, which reduces the current.

## 4. Power save circuit

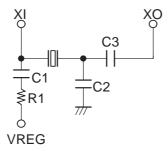
In order to reduce current drain in the STOP condition, the IC goes into power save mode. In this condition, bias current to most circuits is cut off, but the 5V regulator output remains active.

## 5. Reference clock

The reference clock for speed control can be input using one of the following two methods.

#### [1] Using a crystal oscillator

When a crystal is used for oscillation, connect the crystal, capacitors, and a resistor as shown in the figure below.



C1, R1: For stable oscillation

C3: For crystal coupling

C2: For overtone oscillation prevention

#### (Reference values)

Oscillator frequency (MHz)	C1 (μF)	C2 (pF)	C3 (pF)	R1 (Ω)
3 to 5	0.1	10	47	330k
5 to 8	0.1	None	47	330k
8 to 10	0.1	None	22	330k

The circuit configuration and values are for reference only. The crystal oscillator's characteristics as well as the possibility of floating capacitance and noise due to layout factors must be taken into consideration when designing an actual application.

[Precautions for wiring layout design]

Since the crystal oscillator circuit operates at high frequencies, it is susceptible to the influence of floating capacitance from the circuit board. Wiring should be kept as short as possible and traces should be kept narrow.

When designing the external circuitry, pay special attention to the wiring layout between the oscillator and C3 (C2), to minimize the influence of floating capacitance.

## [2] External clock input (equivalent to crystal oscillator, several MHz)

When using an external signal source instead of a crystal oscillator, the clock signal should be input from the XO pin through a resistor of about 5.1 k $\Omega$  connected to the pin in series. The XO pin should be left open. Signal input level

Low: 0 to 0.8V High: 2.5 to 5.0V

#### 6. Speed lock range

The speed clock range is  $\pm 6.25\%$  of the rated speed. When the motor rotation is within the lock range, the LD pin becomes Low (open collector output). When the motor rotation goes out of the lock range, the ON duty ratio of the motor drive output is varied according to the amount of deviation to bring the rotation back into the lock range.

### 7. PWM frequency

The PWM frequency is determined by the capacitance connected to the PWM pin.

 $f PWM = 1/(14400 \times C)$ 

The PWM frequency should be between 15 and 25 kHz.

## 8. Hall input signal

The Hall input requires a signal with an amplitude of at least the hysteresis width (42 mV max.). Taking possible noise influences into consideration, an amplitude of at least 100 mV is desirable.

#### 9. Forward/reverse switching

Forward/reverse switching of motor rotation is carried out with the F/R pin. If this is performed while the motor is running, the following points must be observed:

- Feedthrough current during switching is handled by proper circuit design. However, the V<sub>CC</sub> voltage rise
  during switching (caused by momentary return of motor current to power supply) must not exceed the rated
  voltage (30V). If problems occur, the capacitance between V<sub>CC</sub> and GND must be increased.
- If the motor current after switching exceeds the current limiter value, the lower-side transistors go OFF but the upper-side transistors go into the short brake state, which causes a current flow. The magnitude of the current is determined by the motor counterelectromotive voltage and the coil resistance. This current may not exceed the rated current (3.1A). (Forward/reverse switching at high speed therefore is not safe.)

#### 10. Motor restraint protection circuit

To protect the IC and the motor itself when rotation is inhibited, a restraint protection circuit is provided. If the LD output is High (unlocked) for a certain interval in the start condition, the lower-side transistors are turned off. The length of the interval is determined by the capacitance at the CSD pin. A capacitance of  $10 \,\mu\text{F}$  results in a set interval of about 3.3 seconds. (Tolerance approx.  $\pm 30\%$ )

Set interval (s) 
$$\doteq 0.33 \times C (\mu F)$$

If the capacitor arrangement is subject to leak current, possible adverse effects such as setting time tolerances must be taken into consideration.

When the restraint protection circuit has been activated, the condition can only be canceled by setting the system to the stop condition or by turning the power off and on again (in the stop condition). When wishing not to use the restraint protection circuit, connect the CSD pin to ground.

If the stop time when releasing the restraint protection is short, the capacitor charge will not be fully dissipated. This in turn will cause a shorter restraint protection activation time after the motor has been restarted. The stop time should therefore be designed to be sufficiently long, using the equation shown below (also when restarting in the motor start transient state).

Stop time (ms) 
$$\geq 15 \times C (\mu F)$$

#### 11. Power supply regulation

Because this IC has a high output current, power supply line fluctuations can occur easily. Therefore a capacitor of sufficient capacitance must be connected between the  $V_{CC}$  pin and ground to assure stable operation. If a diode is used in the power line for reverse-connection protection, the likelihood of power line fluctuations increases further, which will require more capacitance.

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