Ordering number: ENN5232A

Monolithic Digital IC

LB1951V

Three-phase Brushless Motor Driver for Portable VCR Capstan Use

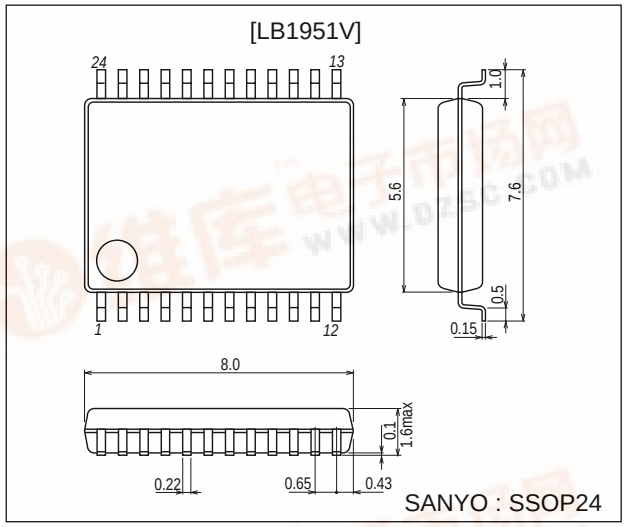
Functions

- 3-phase full-wave current linear drive system (120 ° voltage linear drive system).
- Torque ripple correction circuit built in (overlap correction).
- Speed control system using motor supply voltage control.
- FG comparator built in.
- Thermal shutdown circuit built in.

Package Dimensions

unit : mm

3175A-SSOP24



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}1 max		10	V
	V_{CC}2 max		11	V
	Vs max	≦V_{CC}2	11	V
Applied output voltage	V_O max		V_S +2	V
Maximum output current	I_O max		1.0	A
Allowable power dissipation	Pd max	Independent IC	440	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

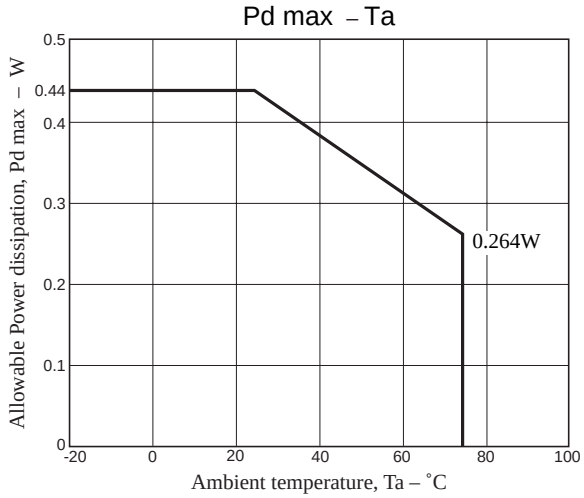
Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}1$		2.7 to 6.0	V
	$V_{CC}2$		3.5 to 9.0	V
	V_S		to V_{CC} 2	V
Hall input amplitude	V_{HALL}	Between Hall inputs	±20 to ±80	mV0-p

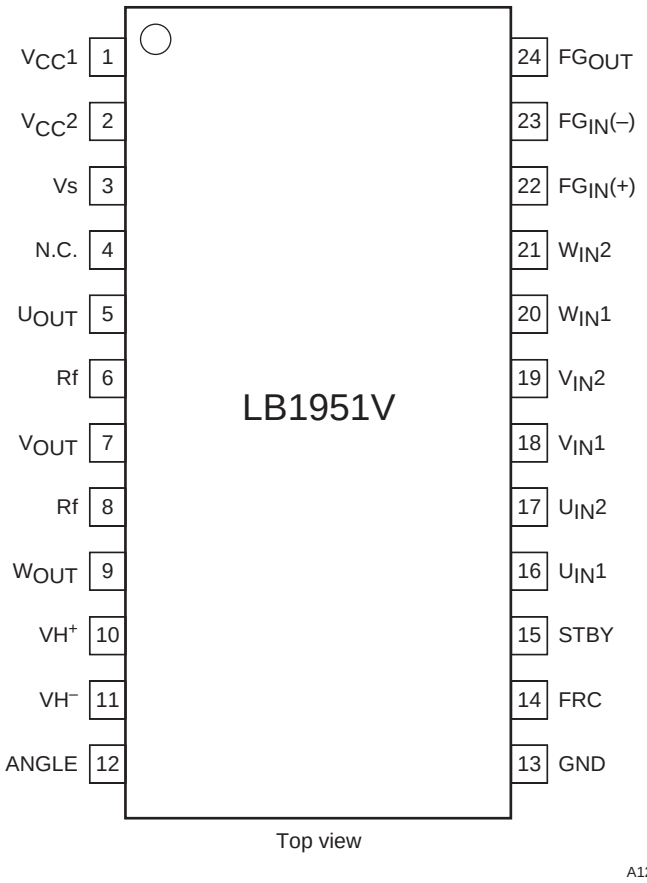
Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 3 V, $V_{CC}2$ = 4.75 V, V_S = 1.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Supply Current]						
Supply current 1	$I_{CC}1$	Iout = 100 mA		3.0	5.0	mA
Supply current 2	$I_{CC}2$	Iout = 100 mA		7.0	10.0	mA
Static current 1	$I_{CCQ}1$	V_{STBY} = 0 V		1.5	3.0	mA
Static current 2	$I_{CCQ}2$	V_{STBY} = 0 V			100	µA
V_S static current	I_{SQ}	V_{STBY} = 0 V		40	100	µA
[VX1]						
Upper side residual voltage	$V_{XH}1$	Iout = 0.2 A	0.15	0.22	0.29	V
Lower side residual voltage	$V_{XL}1$	Iout = 0.2 A	0.16	0.21	0.26	V
[VX2]						
Upper side residual voltage	$V_{XH}2$	Iout = 0.5 A		0.25	0.40	V
Lower side residual voltage	$V_{XL}2$	Iout = 0.5 A		0.25	0.40	V
Output side saturation voltage	Vosat	Iout = 0.8 A, Sink + Source			1.40	V
Overlap	O.L	R_L =39 Ω × 3, R angle = 20 kΩ Note 1	70	77	84	%
[Hall Amplifier]						
Hall amplifier input offset voltage	V_{HOFF}	Note 2	–5		+5	mV
Hall amplifier common-mode input range	V_{HCM}	R angle = 20 kΩ	0.95		2.4	V
Hall amplifier I/O voltage gain	V_{GVH}	R angle = 20 kΩ	24.5	27.5	30.5	dB
[Standby Pin]						
Stand-by pin high-level voltage	V_{STH}		2.5			V
Standby pin low-level voltage	V_{STL}				0.4	V
Standby pin input current	I_{STIN}	V_{STBY} = 3 V		25	40	µA
Standby leakage current	I_{STLK}	V_{STBY} = 0 V			–30	µA
[FRC Pin]						
FRC pin high-level voltage	V_{FRCH}		2.5			V
FRC pin low-level voltage	V_{FRCL}				0.4	V
FRC pin input current	I_{FRCIN}	V_{FRC} = 3 V		20	30	µA
FRC pin leakage current	I_{FRCLK}	V_{FRC} = 0 V			–30	µA
[VH]						
Hall supply voltage	V_{HALL}	I_H = 5 mA, V_H (+)–V_H (–)	0.85	0.95	1.05	V
V_H (–) pin voltage	V_H(–)	I_H = 5 mA	0.81	0.88	0.95	V
[FG Comparator]						
Input offset voltage	V_{FGOFF}		–3		+3	mV
Input bias current	I_{bFG}	V_{FGIN}^+ =V_{FGIN}^- = 1.5 V			500	nA
Input bias current offset	ΔI_{bFG}	V_{FGIN}^+ =V_{FGIN}^- = 1.5 V	–100		+100	nA
Common-mode input range	V_{FGCM}		1.2		2.5	V
Output high-level voltage	V_{FGOH}	At internal pull-up	2.8			V
Output low-level voltage	V_{FGOL}	At internal pull-up			0.2	V
Voltage gain	V_{GFG}	(Design target) Note 2		100		dB
Output current (Sink)	I_{FGOs}	With output pin "L"			5	mA
[TSD]						
TSD operating temperature	T-TSD	(Design target value) Note 2		180		°C
TSD temperature hysteresis width	ΔTSD	(Design target value) Note 2		20		°C

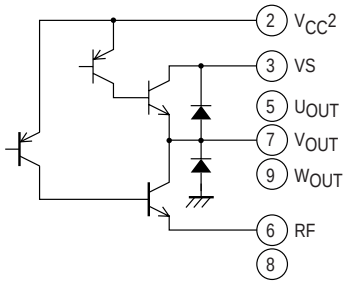
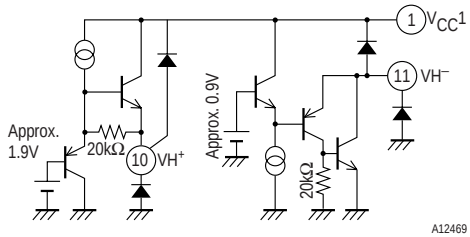
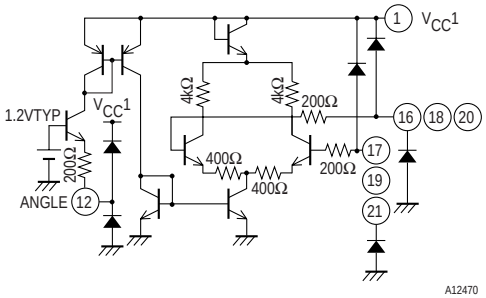
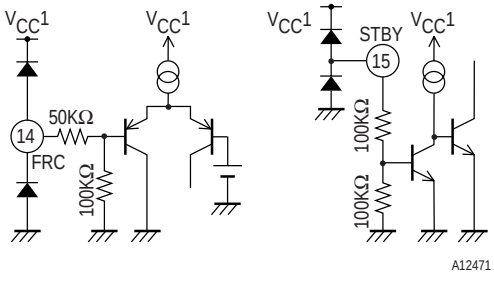
Note 1: Overlapping specifications are assumed to be test specifications.
Note 2: For parameters which have an entry of (Design target value) in the ''Conditions'' column, no measurements are made.



Pin Assignment



Pin Functions

Pin No.	Pin name	I/O equivalent circuit	Function
1	$V_{CC}1$		Power supply pin for supplying power to all circuits except amplitude control block in output block in IC.
2	$V_{CC}2$		Power supply pin for supplying power to all circuits of the amplitude control block and the output control block in IC.
3	V_S		Power supply pin for motor drive. Apply a voltage of $V_{CC}2$ or lower to this pin.
5 7 9	U_{OUT} V_{OUT} W_{OUT}		U-phase output pin V-phase output pin (Spark killer diode built in) W-phase output pin
6, 8	Rf		Pins for grounding output power transistor.
10 11	VH^+ VH^-		Pins for supplying the Hall element bias voltage. Voltage of 0.95 V (typ.) is generated between VH^+ and VH^- . (when I_H = 5 mA)
12	ANGLE		Pins for controlling the Hall input-output gain. The gain is controlled by a resistor between this pin and GND.
16 17 18 19 20 21	$U_{IN}1$ $U_{IN}2$ $V_{IN}1$ $V_{IN}2$ $W_{IN}1$ $W_{IN}2$		U-phase Hall element input pin; Logic “H” represents $IN^+ > IN^-$. V-phase Hall element input pin; Logic “H” represents $IN^+ > IN^-$. W-phase Hall element input pin; Logic “H” represents $IN^+ > IN^-$.
13	GND		Pin for grounding other than output transistors. Minimum potential of output transistors is equal to the level at Rf pin.
14	FRC		Forward/reverse select pin. The voltage on this pin is used for forward/reverse select. (with Hysteresis)
15	STBY		Pin for selecting the bias supply for all circuits except the FG comparator. “L” level on this pin cuts the bias supply.

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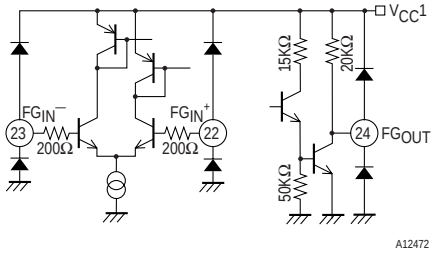
Pin No.	Pin name	I/O equivalent circuit	Function
22	FG_{IN}^{+}		Noninverting input pin for the FG comparator. No bias is applied internally.
23	FG_{IN}^{-}		Inverting input pin for the FG comparator. No bias is applied internally.
24	FG_{OUT}		FG comparator output pin. A resistive load of 20 kΩ is provided internally.

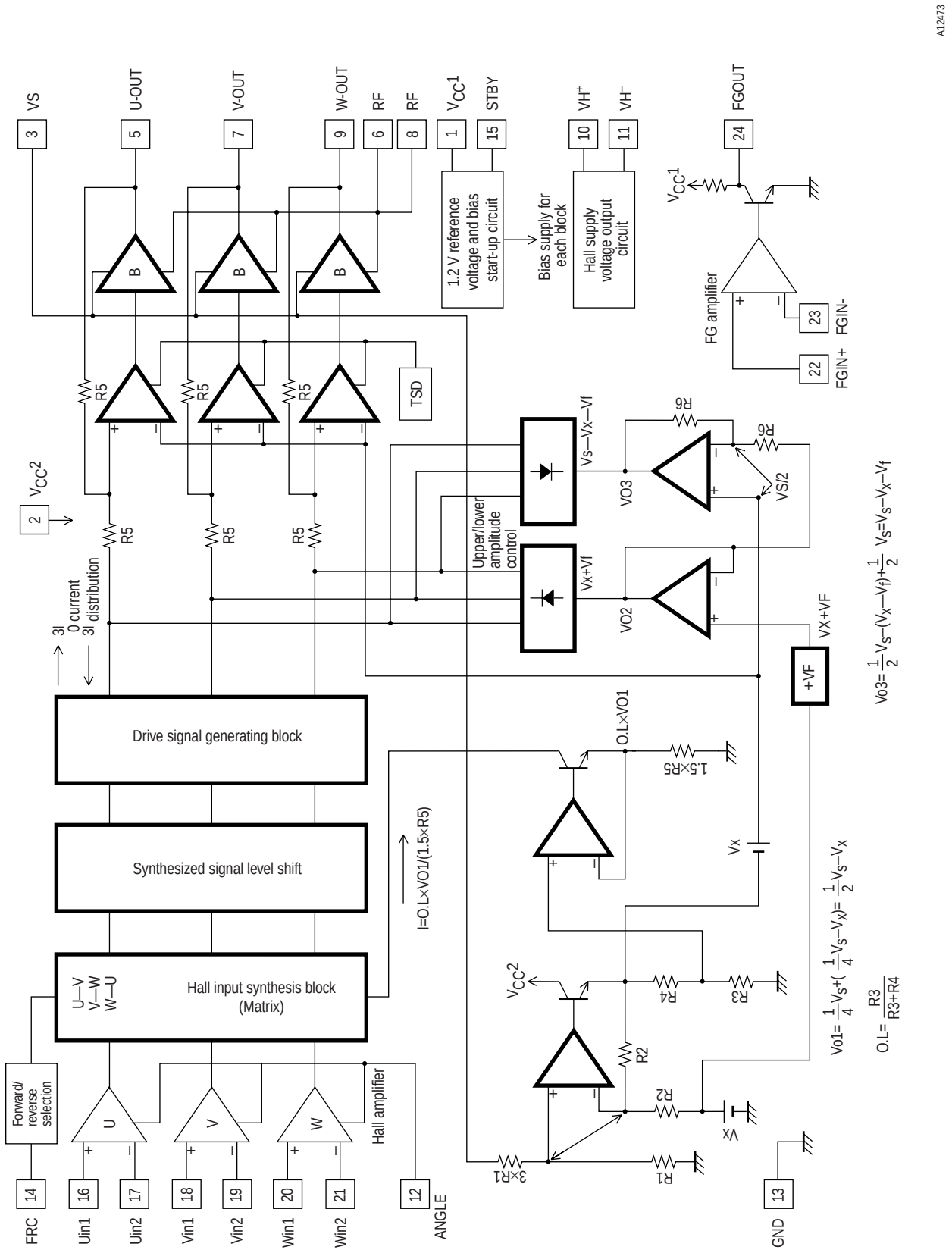
Truth Table

	Source → Sink	Hall input			FRC
		U	V	W	
1	V → W	H	H	L	H
	W → V				L
2	U → W	H	L	L	H
	W → U				L
3	U → V	H	L	H	H
	V → U				L
4	W → V	L	L	H	H
	V → W				L
5	W → U	L	H	H	H
	U → W				L
6	V → U	L	H	L	H
	U → V				L

Note: ‘‘H’’ in the FRC column represents a voltage of 2.5 V or more; ‘‘L’’ represents a voltage of 0.4 V or less. (At $V_{CC}1$ =3 V)

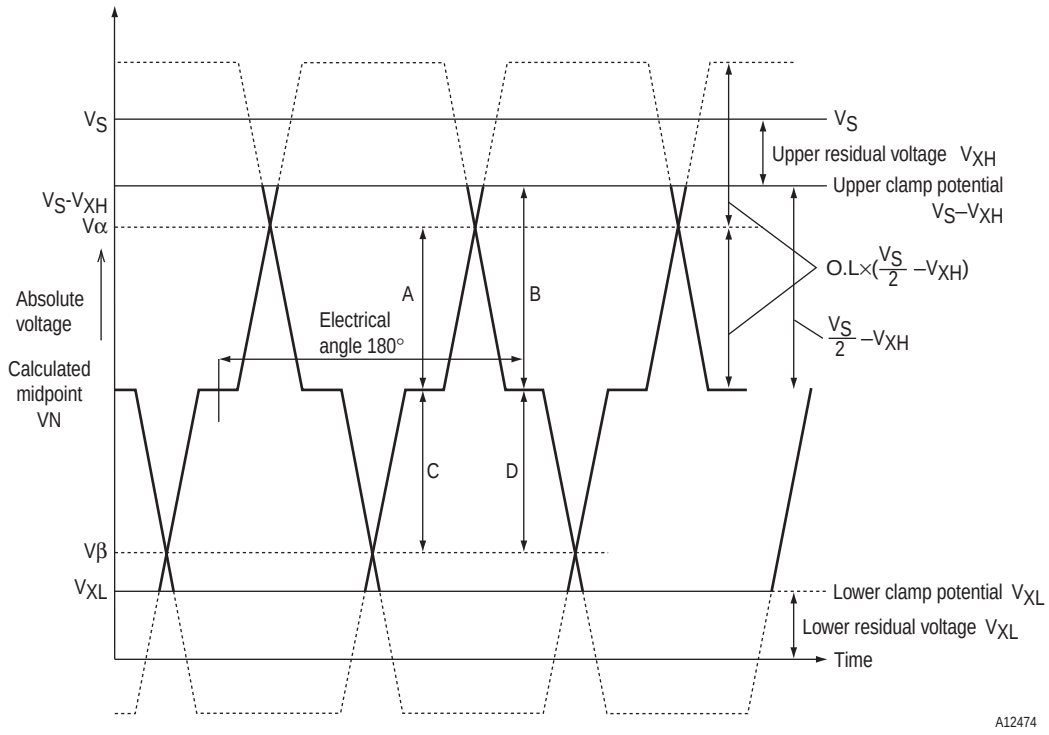
Note: ‘‘H’’ in the Hall input columns represents a state in which ‘‘+’’ has a potential which is higher by 0.02 V or more than that of the ‘‘–’’ phase inputs. Conversely, ‘‘L’’ represents a state in which ‘‘+’’ has a potential which is lower by 0.02 V or more than that of the ‘‘–’’ phase input.

Block Diagram



* For the blocks drawn with thick lines, power is supplied from $V_{CC}2$.

Overlap Creation and Calculation



i) Overlap creation

Because the voltage generated in the amplitude control block is: $2 \times \text{O.L.} \times (1/2\ V_S - V_X)$ for each side, (using the midpoint as the reference point), the point at which the two waveforms cross each other is O.L. $(1/2\ V_S - V_X)$ from the midpoint.

Because that waveform is clamped at $(1/2\ V_S - V_X)$ with the midpoint as the reference point, the overlap equals A/B $\times$ 100, which equals O.L. $\times$ 100 (%).

ii) Overlap calculation

(1) Upper overlap amount

$$\text{Calculated midpoint VN} = \frac{(V_S - V_{XH} - V_{XL})}{2} + V_{XL} = \frac{(V_S - V_{XH} + V_{XL})}{2}$$

Because $A = V\alpha - VN$ and $B = V_S - V_{XH} - VN$, the upper overlap amount is calculated as follows:

$$\text{Overlap amount} = \frac{A}{B} = \frac{V\alpha - \{(V_S - V_{XH} + V_{XL})/2\}}{V_S - V_{XH} - \{(V_S - V_{XH} + V_{XL})/2\}} \times 100$$

$$= \frac{2V\alpha - (V_S - V_{XH}) - V_{XL}}{(V_S - V_{XH}) - V_{XL}} \times 100\ (\%)$$

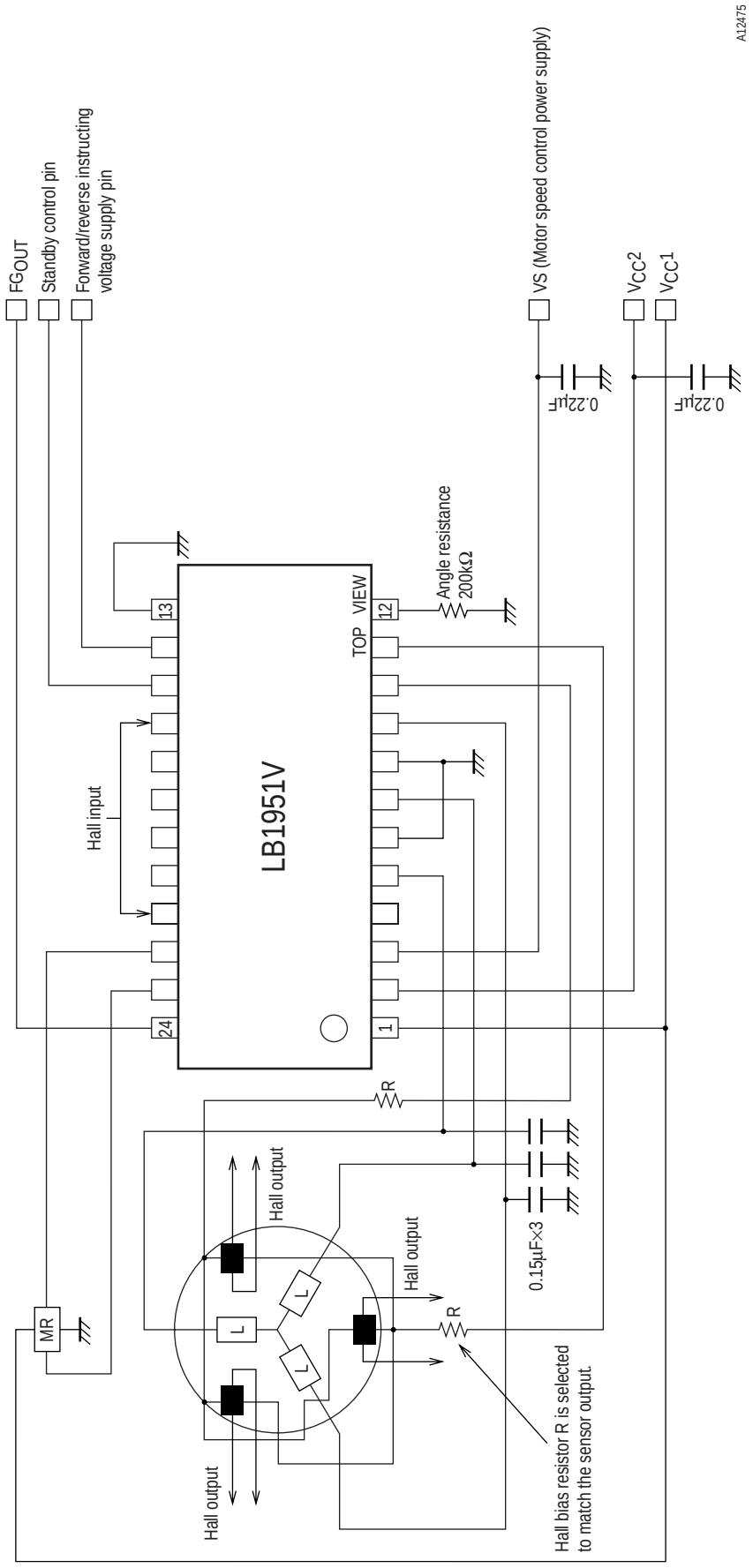
(2) Lower overlap amount

Because $C = VN - V\beta$ and $D = VN - V_{XL}$, the lower overlap amount is calculated as follows:

$$\text{Overlap amount} = \frac{C}{D} = \frac{\{(V_S - V_{XH} + V_{XL})/2\} - V\beta}{\{(V_S - V_{XH} + V_{XL})/2\} - V_{XL}} \times 100$$

$$= \frac{(V_S - V_{XH}) + V_{XL} - 2V\beta}{(V_S - V_{XH}) - V_{XL}} \times 100\ (\%)$$

Sample Application Circuit



Note: It should be noted that the constants specified are for example only, with no guarantee for characteristics implied.