

Monolithic Digital IC

**LB1951V**

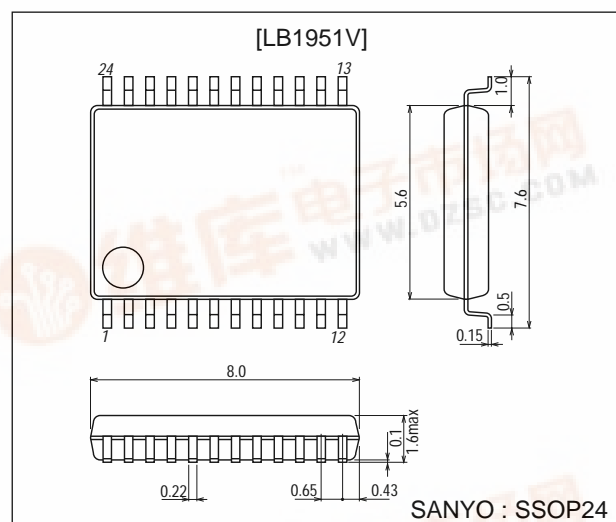
Three-phase Brushless Motor Driver for Portable VCR Capstan Use

Functions

- 3-phase full-wave current linear drive system (120 ° voltage linear drive system).
- Torque ripple correction circuit built in (overlap correction).
- Speed control system using motor supply voltage control.
- FG comparator built in.
- Thermal shutdown circuit built in.

Package Dimensions

unit : mm

3175A-SSOP24

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC1} max		10	V
	V _{CC2} max		11	V
	V _S max	≦V _{CC2}	11	V
Applied output voltage	V _O max		V _S +2	V
Maximum output current	I _O max		1.0	A
Allowable power dissipation	P _d max	Independent IC	440	mW
Operating temperature	T _{opr}		-20 to +75	°C
Storage temperature	T _{stg}		-55 to +150	°C

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Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC1}		2.7 to 6.0	V
	V _{CC2}		3.5 to 9.0	V
	V _S		to V _{CC2}	V
Hall input amplitude	V _{HALL}	Between Hall inputs	±20 to ±80	mV _{0-p}

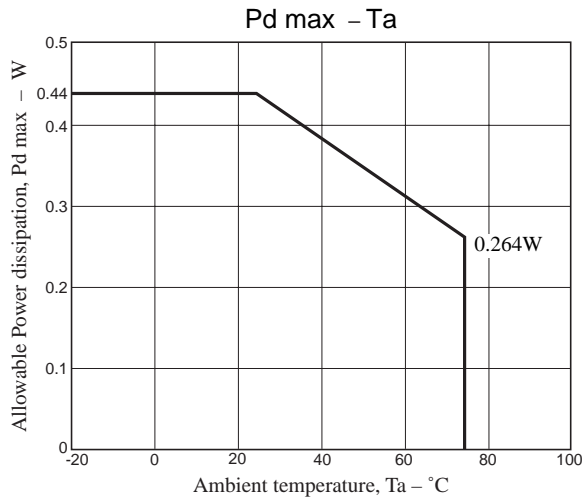
Electrical Characteristics at Ta = 25°C, V_{CC1} = 3 V, V_{CC2} = 4.75 V, V_S = 1.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Supply Current]						
Supply current 1	I _{CC1}	I _{out} = 100 mA		3.0	5.0	mA
Supply current 2	I _{CC2}	I _{out} = 100 mA		7.0	10.0	mA
Static current 1	I _{CCQ1}	V _{STBY} = 0 V		1.5	3.0	mA
Static current 2	I _{CCQ2}	V _{STBY} = 0 V			100	μA
V _S static current	I _{SQ}	V _{STBY} = 0 V		40	100	μA
[VX1]						
Upper side residual voltage	V _{XH1}	I _{out} = 0.2 A	0.15	0.22	0.29	V
Lower side residual voltage	V _{XL1}	I _{out} = 0.2 A	0.16	0.21	0.26	V
[VX2]						
Upper side residual voltage	V _{XH2}	I _{out} = 0.5 A		0.25	0.40	V
Lower side residual voltage	V _{XL2}	I _{out} = 0.5 A		0.25	0.40	V
Output side saturation voltage	V _{osat}	I _{out} = 0.8 A, Sink + Source			1.40	V
Overlap	O.L	R _L = 39 Ω × 3, R angle = 20 kΩ Note 1	70	77	84	%
[Hall Amplifier]						
Hall amplifier input offset voltage	V _{HOFF}	Note 2	-5		+5	mV
Hall amplifier common-mode input range	V _{HCM}	R angle = 20 kΩ	0.95		2.4	V
Hall amplifier I/O voltage gain	V _{GVH}	R angle = 20 kΩ	24.5	27.5	30.5	dB
[Standby Pin]						
Stand-by pin high-level voltage	V _{STH}		2.5			V
Standby pin low-level voltage	V _{STL}				0.4	V
Standby pin input current	I _{STIN}	V _{STBY} = 3 V		25	40	μA
Standby leakage current	I _{STLK}	V _{STBY} = 0 V			-30	μA
[FRC Pin]						
FRC pin high-level voltage	V _{FRCH}		2.5			V
FRC pin low-level voltage	V _{FRCL}				0.4	V
FRC pin input current	I _{FRGIN}	V _{FRC} = 3 V		20	30	μA
FRC pin leakage current	I _{FRCLK}	V _{FRC} = 0 V			-30	μA
[VH]						
Hall supply voltage	V _{HALL}	I _H = 5 mA, V _H (+)-V _H (-)	0.85	0.95	1.05	V
V _H (-) pin voltage	V _{H(-)}	I _H = 5 mA	0.81	0.88	0.95	V
[FG Comparator]						
Input offset voltage	V _{FGOFF}		-3		+3	mV
Input bias current	I _{bFG}	V _{FGIN+} = V _{FGIN-} = 1.5 V			500	nA
Input bias current offset	ΔI _{bFG}	V _{FGIN+} = V _{FGIN-} = 1.5 V	-100		+100	nA
Common-mode input range	V _{FGCM}		1.2		2.5	V
Output high-level voltage	V _{FGOH}	At internal pull-up	2.8			V
Output low-level voltage	V _{FGOL}	At internal pull-up			0.2	V
Voltage gain	V _{GFG}	(Design target) Note 2		100		dB
Output current (Sink)	I _{FGOs}	With output pin "L"			5	mA
[TSD]						
TSD operating temperature	T-TSD	(Design target value) Note 2		180		°C
TSD temperature hysteresis width	ΔTSD	(Design target value) Note 2		20		°C

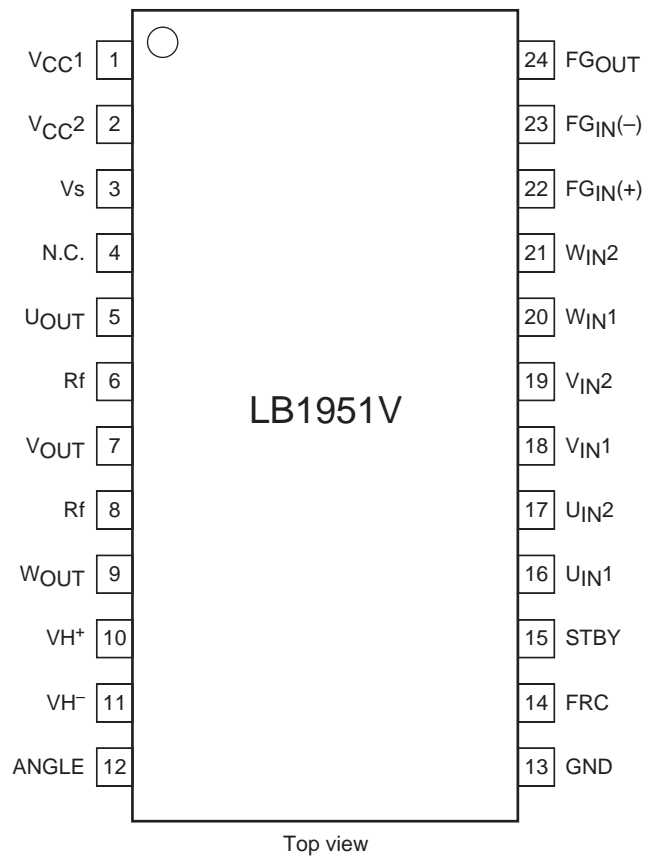
Note 1: Overlapping specifications are assumed to be test specifications.

Note 2: For parameters which have an entry of (Design target value) in the "Conditions" column, no measurements are made.

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Pin Assignment



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Pin Functions

Pin No.	Pin name	I/O equivalent circuit	Function
1	V _{CC1}		Power supply pin for supplying power to all circuits except amplitude control block in output block in IC.
2	V _{CC2}		Power supply pin for supplying power to all circuits of the amplitude control block and the output control block in IC.
3	V _S		Power supply pin for motor drive. Apply a voltage of V _{CC2} or lower to this pin.
5 7 9	U _{OUT} V _{OUT} W _{OUT}		U-phase output pin V-phase output pin (Spark killer diode built in) W-phase output pin
6, 8	Rf		Pins for grounding output power transistor.
10 11	V _H ⁺ V _H ⁻		Pins for supplying the Hall element bias voltage. Voltage of 0.95 V (typ.) is generated between V _H ⁺ and V _H ⁻ . (when I _H = 5 mA)
12	ANGLE		Pins for controlling the Hall input-output gain. The gain is controlled by a resistor between this pin and GND.
16 17 18 19 20 21	U _{IN1} U _{IN2} V _{IN1} V _{IN2} W _{IN1} W _{IN2}		U-phase Hall element input pin; Logic "H" represents IN ⁺ > IN ⁻ . V-phase Hall element input pin; Logic "H" represents IN ⁺ > IN ⁻ . W-phase Hall element input pin; Logic "H" represents IN ⁺ > IN ⁻ .
13	GND		Pin for grounding other than output transistors. Minimum potential of output transistors is equal to the level at Rf pin.
14	FRC		Forward/reverse select pin. The voltage on this pin is used for forward/reverse select. (with Hysteresis)
15	STBY		Pin for selecting the bias supply for all circuits except the FG comparator. "L" level on this pin cuts the bias supply.

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Pin No.	Pin name	I/O equivalent circuit	Function
22	FG _{IN+}		Noninverting input pin for the FG comparator. No bias is applied internally.
23	FG _{IN-}		Inverting input pin for the FG comparator. No bias is applied internally.
24	FG _{OUT}		FG comparator output pin. A resistive load of 20 kΩ is provided internally.

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Truth Table

	Source → Sink	Hall input			FRC
		U	V	W	
1	V → W	H	H	L	H
	W → V	H	H	L	L
2	U → W	H	L	L	H
	W → U	H	L	L	L
3	U → V	H	L	H	H
	V → U	H	L	H	L
4	W → V	L	L	H	H
	V → W	L	L	H	L
5	W → U	L	H	H	H
	U → W	L	H	H	L
6	V → U	L	H	L	H
	U → V	L	H	L	L

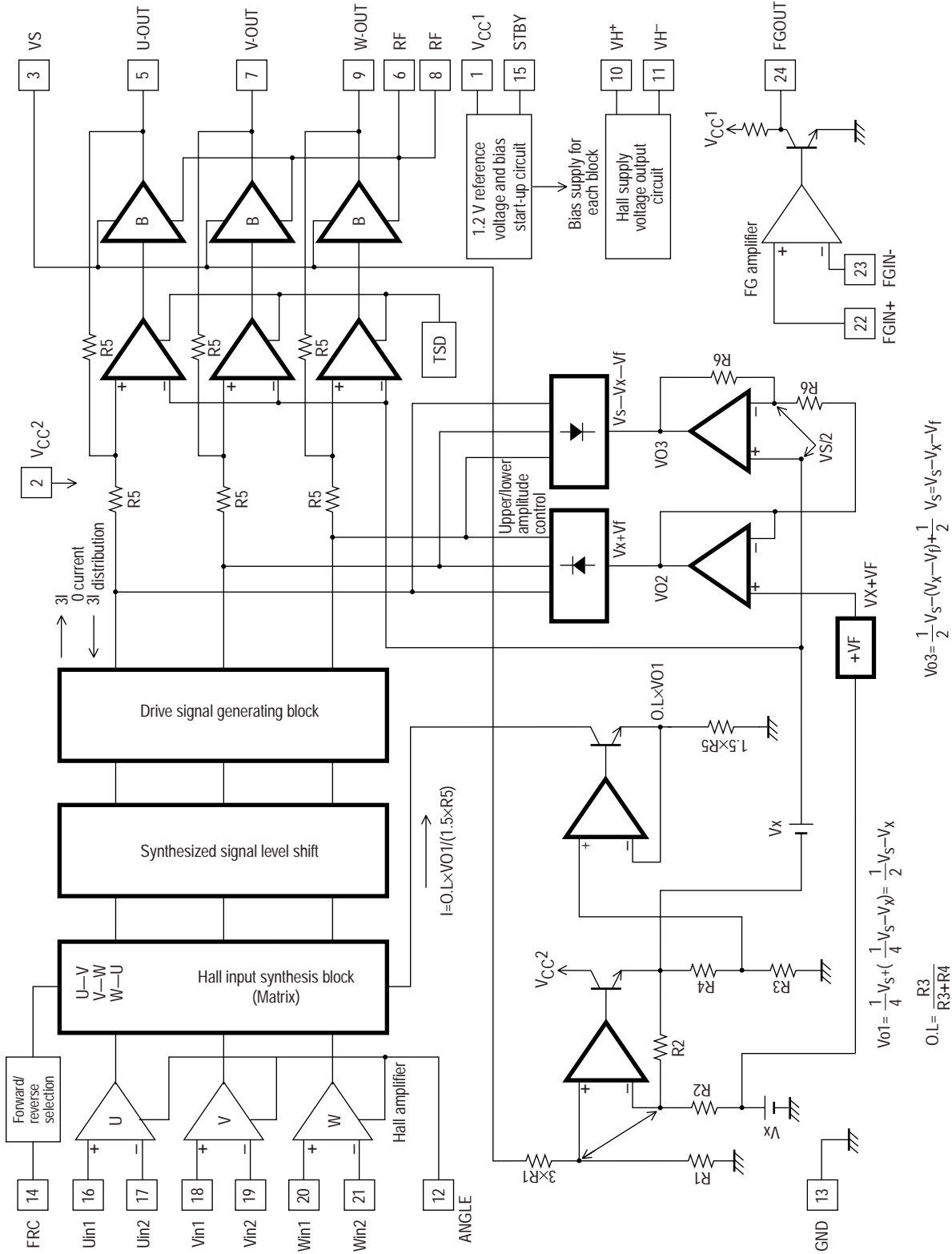
Note: “H” in the FRC column represents a voltage of 2.5 V or more; “L” represents a voltage of 0.4 V or less.
(At $V_{CC1} = 3$ V)

Note: “H” in the Hall input columns represents a state in which “+” has a potential which is higher by 0.02 V or more than that of the “-” phase inputs.

Conversely, “L” represents a state in which “+” has a potential which is lower by 0.02 V or more than that of the “-” phase input.

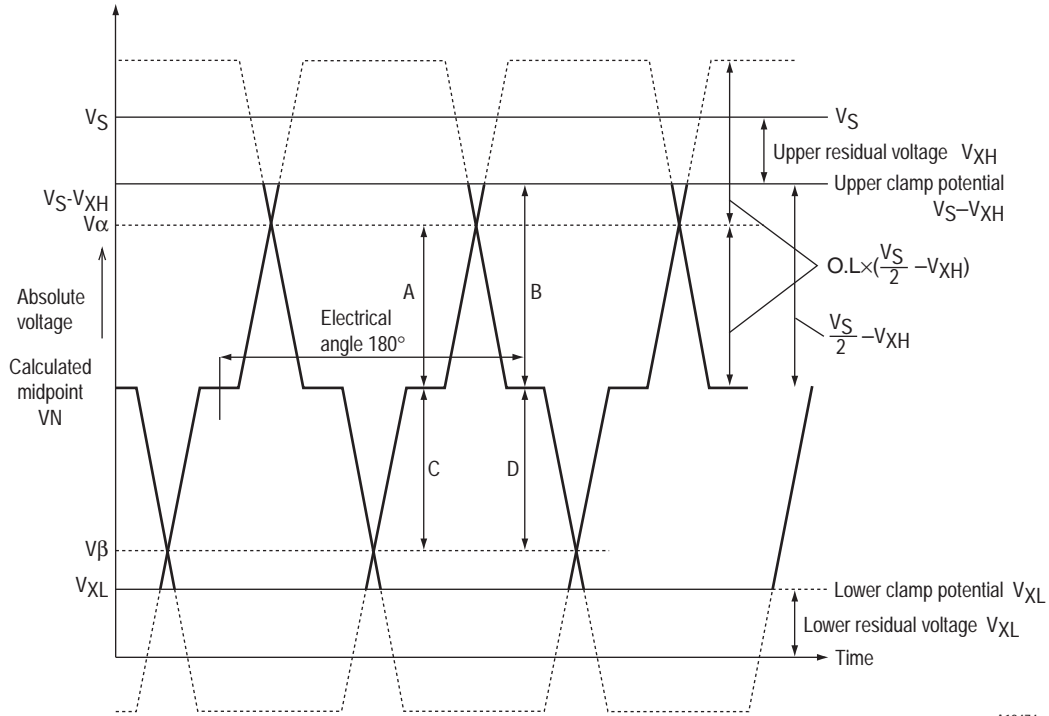
Block Diagram

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* For the blocks drawn with thick lines, power is supplied from VCC2.

Overlap Creation and Calculation



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i) Overlap creation

Because the voltage generated in the amplitude control block is: $2 \times O.L. \times (1/2 V_S - V_X)$ for each side, (using the midpoint as the reference point), the point at which the two waveforms cross each other is $O.L. \times (1/2 V_S - V_X)$ from the midpoint.

Because that waveform is clamped at $(1/2 V_S - V_X)$ with the midpoint as the reference point, the overlap equals $A/B \times 100$, which equals $O.L. \times 100$ (%).

ii) Overlap calculation

(1) Upper overlap amount

$$\text{Calculated midpoint } V_N = \frac{(V_S - V_{XH} - V_{XL})}{2} + V_{XL} = \frac{(V_S - V_{XH} + V_{XL})}{2}$$

Because $A = V_\alpha - V_N$ and $B = V_S - V_{XH} - V_N$, the upper overlap amount is calculated as follows:

$$\begin{aligned} \text{Overlap amount} &= \frac{A}{B} = \frac{V_\alpha - \{(V_S - V_{XH} + V_{XL})/2\}}{V_S - V_{XH} - \{(V_S - V_{XH} + V_{XL})/2\}} \times 100 \\ &= \frac{2V_\alpha - (V_S - V_{XH}) - V_{XL}}{(V_S - V_{XH}) - V_{XL}} \times 100 (\%) \end{aligned}$$

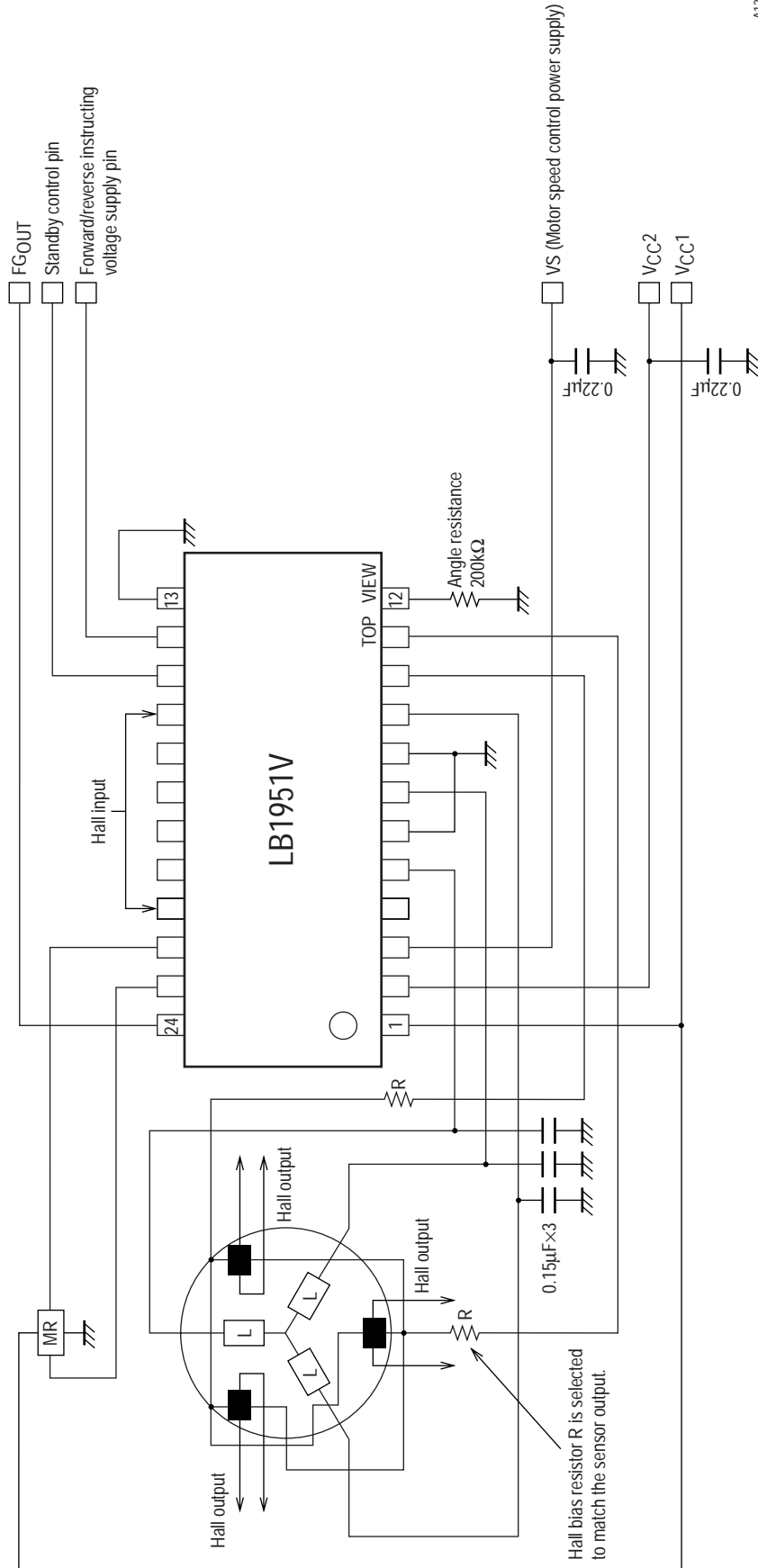
(2) Lower overlap amount

Because $C = V_N - V_\beta$ and $D = V_N - V_{XL}$, the lower overlap amount is calculated as follows:

$$\begin{aligned} \text{Overlap amount} &= \frac{C}{D} = \frac{\{(V_S - V_{XH} + V_{XL})/2\} - V_\beta}{\{(V_S - V_{XH} + V_{XL})/2\} - V_{XL}} \times 100 \\ &= \frac{(V_S - V_{XH}) + V_{XL} - 2V_\beta}{(V_S - V_{XH}) - V_{XL}} \times 100 (\%) \end{aligned}$$

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Sample Application Circuit



AT2475

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