Ordering number : EN5979A

Monolithic Digital IC



## LB1998

# Three-Phase Brushless Motor Driver for CD-ROM Spindle Drive

#### Overview

The LB1998 is a three-phase brushless motor driver especially suited for CD-ROM spindle motor drives.

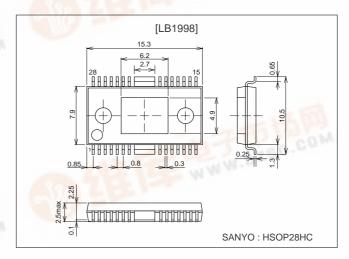
#### **Functions**

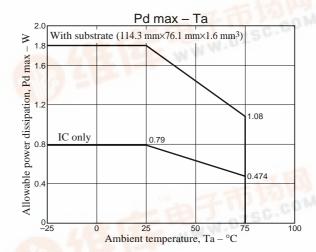
- Current linear drive
- Control V type amplifier
- Top side current detection technique reduces loss voltage of current detection resistor. Voltage effect of this resistor reduces internal current drain of IC.
- Built-in current limiter circuit
- · Built-in reverse blocking circuit
- · Hall FG output
- Built-in 1 Hall FG/3 Hall FG switching circuit
- · Built-in short braking circuit
- Built-in Hall bias cicuit
- Built-in thermal shutdown circuit
- Built-in S/S function
- Built-in 3 mode gain switching function ensures compatibility with 8/12 cm CAV and CLV discs

#### **Package Dimensions**

unit: mm

3234-HSOP28HC





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# **Specifications**

## Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V <sub>CC</sub> 1 max		7.0	V
	V <sub>CC</sub> 2 max		14.4	V
	V <sub>CC</sub> 3 max		14.4	V
Applied output voltage	V <sub>O</sub> max		14.4	V
Applied intput voltage	V <sub>IN</sub> max		V <sub>CC</sub> 1	V
Output current	I <sub>O</sub> max		1.3	А
Allowable power dissipation	Pd max	IC only	0.79	W
		with substrate (114.3 $\times$ 76.1 $\times$ 1.6 mm <sup>3</sup> , glass exposy)	1.80	W
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

## Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V <sub>CC</sub> 1		4 to 6	V
	V <sub>CC</sub> 2	≥V <sub>CC</sub> 1	4 to 13.6	V

## Sample Application at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
12V type	V <sub>CC</sub> 1	Regulated voltage	4 to 6	V
	V <sub>CC</sub> 2	Unregulated voltage	4 to 13.6	V

## LB1998

# Electrical Characteristics at Ta = 25 $^{\circ}$ C, $V_{CC}1$ = 5V, $V_{CC}2$ = 12V

Parameter	Symbol	Conditions		Ratings		Unit		
raidinotor	Oymboi	Conditions	min	typ	max	Offic		
Power supply current]								
Power supply current	I <sub>CC</sub> 1	V <sub>CIN</sub> = V <sub>CREF</sub>		8		mA		
	I <sub>CC</sub> 2	V <sub>CIN</sub> = V <sub>CREF</sub>		250	300	mA		
Output idle current	I <sub>CC</sub> 10Q	$V_{S/S} = 0V$			200	μΑ		
	I <sub>CC</sub> 2OQ	$V_{S/S} = 0V$			60	μΑ		
[Output]								
Saturation voltage, upper side 1	V <sub>OU</sub> 1	$I_{O} = -0.5A, V_{CC}1 = 5V, V_{CC}2 = 12V$		1.0		V		
Saturation voltage, lower side 1	V <sub>OD</sub> 1	$I_{O} = 0.5A, V_{CC}1 = 5V, V_{CC}2 = 12V$		0.3		V		
Current limiter setting voltage	V <sub>CL</sub>	$R_{RF} = 0.25\Omega$		0.25		V		
[Hall amplifier]								
Common mode input voltage range	V <sub>HCOM</sub>		1.2		V <sub>CC</sub> 1–1.0	V		
Input bias current	I <sub>HIB</sub>			1		μΑ		
Minimum Hall input level	$V_{HIN}$		60			$mV_{P-P}$		
[S/S pin]								
High level voltage	V <sub>S/SH</sub>		2.0		V <sub>CC</sub> 1	V		
Low level voltage	V <sub>S/SL</sub>				0.7	V		
Input current	I <sub>S/SI</sub>	V <sub>S/S</sub> = 5V			200	μΑ		
Leak current	I <sub>S/SL</sub>	V <sub>S/S</sub> = 0V	-30			μΑ		
[Control]	•							
V <sub>CIN</sub> pin input current	I <sub>VC</sub>	V <sub>CIN</sub> = V <sub>CREF</sub> = 1.65V			1	μΑ		
V <sub>CREF</sub> pin input current	I <sub>VCREF</sub>	V <sub>CIN</sub> = V <sub>CREF</sub> = 1.65V			1	μΑ		
Voltage gain	GV <sub>CO</sub>	$\Delta V_{RF}/\Delta V_{C}$ , Note 1		0.25		times		
Startup voltage	V <sub>CTH</sub>	V <sub>CREF</sub> = 1.65V, Note 1	1.55		1.85	V		
Startup voltage width	$\Delta V_{CTH}$	V <sub>CREF</sub> = 1.65V, Note 1	100		200	mV		
[Gain switching amplifier]	•							
Input offset voltage	V <sub>GCOFFSET</sub>	Design target value	-8		+8	mV		
OPEN LOOP voltage gain	G <sub>VGC</sub>	f = 10 kHz, Design target value		43		dB		
Same-phase input voltage range	V <sub>GCOM</sub>		0		3.5	V		
[Hall power supply]	•				•			
Hall power supply voltage	V <sub>H</sub>	I <sub>H</sub> = 5 mA		0.8		V		
Allowable current	I <sub>H</sub>		20			mA		
[Thermal shutdown]	•							
Operating temperature	T <sub>TSD</sub>	Design target value	150	180	210	°C		
Hysterisis	$\Delta T_{TSD}$	Design target value		15		°C		
[Short braking]	•				•			
Brake pin at High level	V <sub>BRH</sub>		4		5	V		
Brake pin at Low level	V <sub>BRL</sub>		0		1	V		
[1 Hall FG/3 Hall FG switching]	•							
FG <sub>SEL</sub> pin at High level	V <sub>FSH</sub>		4		5			
FG <sub>SEL</sub> pin at Low level	V <sub>FSL</sub>		0		1			
[Gain switching analog switch]								
Analog switch at High level	R <sub>INH</sub>		V <sub>CC</sub> -0.5		V <sub>CC</sub> 1			
Analog switch at Low level			0		0.2			
Analog switch at Low level  Note:	R <sub>INL</sub>		0		0.2			

#### Note:

- • During S/S OFF (standby), the Hall comparator is at High.
- Gain switching amplifier operated at a factor of 1.
- Design target values are not measured.

#### **Truth Table**

			Hall input		Control
	Source -> Sink	U	V	W	V <sub>CIN</sub>
1	Phase W -> Phase V	Н	Н	1	Н
'	Phase V -> Phase W	'''	''	_	L
2	Phase W -> Phase U	Н	1	1	Н
2	Phase U -> Phase W		H	L	L
3	Phase V -> Phase W	1	1	Н	Н
3	Phase W -> Phase V	1 - 1 - 1		L	
4	Phase U -> Phase V	1	Н	1	Н
4	Phase V -> Phase U	_	''	_	L
5	Phase V -> Phase U	Н	н	Н	Н
	Phase U -> Phase V		_	- 11	Ĺ
6	Phase U -> Phase W	1	Н	Н	Н
	Phase W -> Phase U	_	''		L

Input:

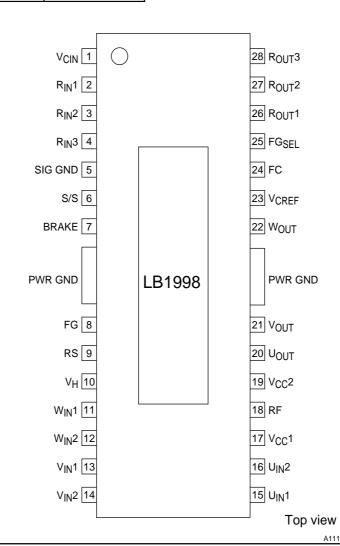
H: Input 1 is higher in potential than input 2 by at least 0.2V.

L: Input 1 is lower in potential than input 2 by at least 0.2V.

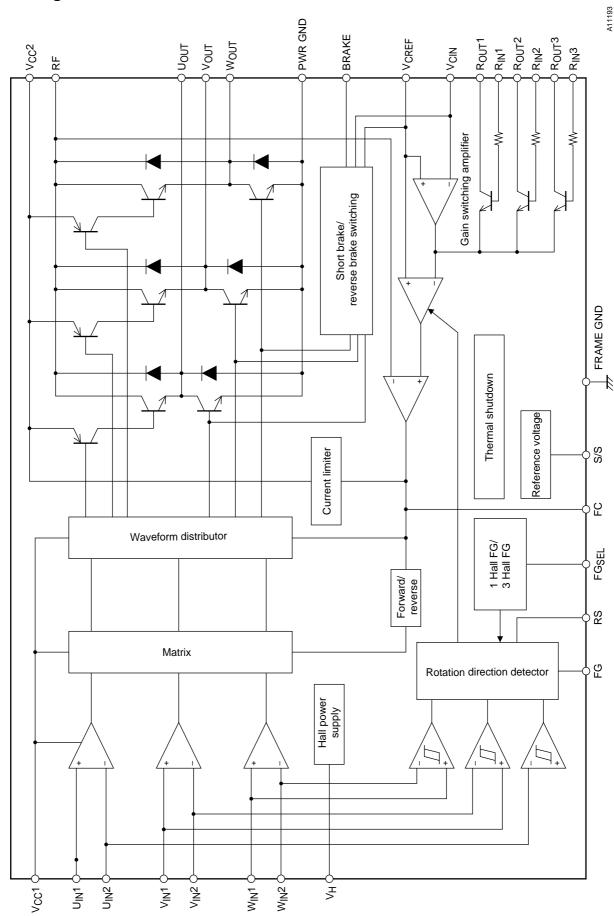
## **Brake Mode Switching Truth Table**

BRAKE pin	V <sub>CIN</sub> > V <sub>CREF</sub>	V <sub>CIN</sub> < V <sub>CREF</sub>
L, OPEN	Foward	Reverse brake
Н	Foward	Short brake

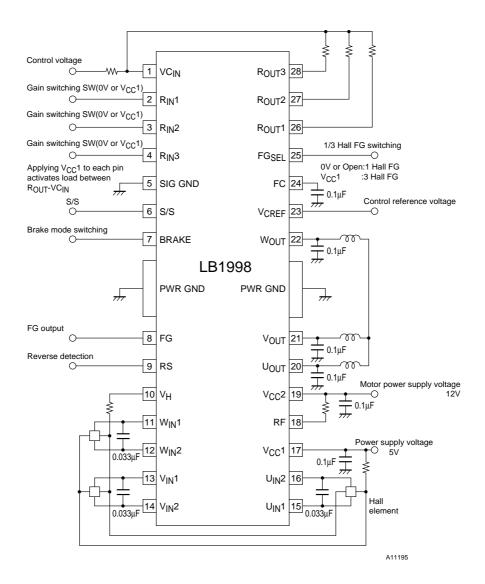
## **Pin Assignment**



## **Block Diagram**



## **Sample Application Circuit**



# **Pin Descriptions**

Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
19	V <sub>CC</sub> 2	4V to 13.6V		Source side predrive voltage and constant current control amplifier voltage supply pin
17	V <sub>CC</sub> 1	4V to 6V		Power supply pin for all circuits except output transistors, source predriver, and low current control amplifier
9	RS		100μA ↓ \$10 kΩ ★ 8 9	Reverse detector pin Forward rotation: High Reverse rotation: Low
8	FG		A11196	1 Hall or 3 Hall element waveform Schmitt comparator combined output
15 16	U <sub>IN</sub> 1 U <sub>IN</sub> 2		Усс1 (1) Т (12)	U phase Hall element input and reverse detector U phase Schmitt comparator input pin Logic High indicates U <sub>IN</sub> 1 > U <sub>IN</sub> 2.
13 14	V <sub>IN</sub> 1 V <sub>IN</sub> 2	1.2V to V <sub>CC</sub> 1–1V	(1) (13) (15) (14) (16) (16) (17) (18) (19) (19) (19) (19) (19) (19) (19) (19	V phase Hall element input and reverse detector V phase Schmitt comparator input pin Logic High indicates V <sub>IN</sub> 1 > V <sub>IN</sub> 2.
11 12	W <sub>IN</sub> 1 W <sub>IN</sub> 2		ती त	W phase Hall element input and reverse detector W phase Schmitt comparator input pin Logic High indicates W <sub>IN</sub> 1 > W <sub>IN</sub> 2.
10	$V_{H}$		75μA VCC1 75μA 11198	Hall element lower side bias voltage supply pin
6	S/S	0V to W <sub>CC</sub> 1	VCC1  75 kΩ  W  50 kΩ ₹  A11199	When this pin is at 0.7V or lower, or when it is open, all circuits are inactive. When driving motor, set this pin to 2V or higher.
5	SIG GND			GND pin for all circuits except output
24	FC		V <sub>CC</sub> 1  V <sub>CC</sub> 1  24  20 kΩ ≤ 5 kΩ  A11200	Control loop frequency compensator pin. Connecting a capacitor between this pin and GND prevents closed loop oscillation in current limiting circuitry.

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Pin number	om preceding Pin name	Pin voltage	Equivalent circuit	Pin function
23	V <sub>CREF</sub>	0V to 3.5V	15μA	Control reference voltage supply pin. Determines control start voltage.
1	V <sub>CIN</sub>	0V to 3.5V	6 pF 200Ω 23 A11202	Speed control voltage supply pin V type control technique $V_C > V_{CREF}$ : Forward $V_C < V_{CREF}$ : Slowdown (Reverse-blocking circuit prevents reverse rotation.)
22	W <sub>OUT</sub>			W phase output
	PWR GND			Output transistor GND
21	V <sub>OUT</sub>		(18) V <sub>CC</sub> <sup>2</sup>	V phase output
20	U <sub>OUT</sub>		3.90	U phase output
18	RF		3.9Ω (20) (21) (22) PWRGND A11203	Upper side output PNP transistor collector pin (common for all 3 phases). For current detection, connect resistor between V <sub>CC</sub> 3 pin and RF pin. Constant current control and current limiter works by detecting this voltage.
25	FG <sub>SEL</sub>		75 kΩ VCC1 75 kΩ 225 ≥ 50 kΩ A11204	1 Hall FG/3 Hall FG output, switching pin: High -> 3 Hall FG Low/Open -> 1 Hall FG
7	BRAKE		100μA ↓ VCC1  75 kΩ  \$50 kΩ  A11205	Brake mode switching pin BRAKE: High -> Short brake Low/Open -> Reverse brake Brake mode changes when V <sub>CIN</sub> > V <sub>CREF</sub> .

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Pin number	Pin name	Pin voltage	Equivalent circuit	Pin function
2	R <sub>IN</sub> 1		- Vcc1	Gain switching selector pin When set to High ( $V_{CC}1$ ), resistor connected between $R_{OUT}1$ and $V_{CIN}$ is selected as negative feedback resistor.
3	R <sub>IN</sub> 2	0 to V <sub>CC</sub> 1 Low: 0V High: V <sub>CC</sub> 1	26 10 kΩ 2 2 3 3 4 4	Gain switching selector pin When set to High (V <sub>CC</sub> 1), resistor connected between R <sub>OUT</sub> 2 and V <sub>CIN</sub> is selected as negative feedback resistor.
4	R <sub>IN</sub> 3		777 M7 A11206	Gain switching selector pin When set to High ( $V_{CC}1$ ), resistor connected between $R_{OUT}3$ and $V_{CIN}$ is selected as negative feedback resistor.
26	R <sub>OUT</sub> 1			Negative feedback resistor
27	R <sub>OUT</sub> 2			connector pins  Connect negative feedback resistors
28	R <sub>OUT</sub> 3			between these pins and V <sub>CIN</sub> .

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