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CMOS IC

LC866448B/44B/40B/36B/32B/28B/24B/20B/16B/12B/08B

8-Bit Single Chip Microcontroller

Preliminary

Overview

The LC866448B/44B/40B/36B/32B/28B/24B/20B/16B/12B/08B microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.5µs (microsecond)
- On-chip ROM Maximum Capacity : 48K bytes
- On-chip RAM Capacity : 1152/768/640/512 bytes
  (LC866448B/44B/40B/36B/32B/28B/24B/20B/16B/12B/08B)
- 16-bit timer /counter (or two 8-bit timers)
- 16-bit timer /PWM (or two 8-bit timers)
- 8-channel × 8-bit AD converter
- Two 8-bit synchronous serial-interface circuits (1-channel × 16bit, 1-channel × 8bit)
- 14-source 10-vectored interrupt system

All of the above functions are fabricated on a single chip.

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Features

(1) Read-Only Memory (ROM)
- : LC866448B 49152 × 8 bits
- : LC866444B 45056 × 8 bits
- : LC866440B 40960 × 8 bits
- : LC866436B 36864 × 8 bits
- : LC866432B 32768 × 8 bits
- : LC866428B 28672 × 8 bits
- : LC866424B 24576 × 8 bits
- : LC866420B 20480 × 8 bits
- : LC866416B 16384 × 8 bits
- : LC866412B 12288 × 8 bits
- : LC866408B 8192 × 8 bits

(2) Random Access Memory (RAM)
- : LC866448B/44B/40B/36B 1152 × 8 bits
- : LC866432B/28B/24B 768 × 8 bits
- : LC866420B/16B 640 × 8 bits
- : LC866412B/08B 512 × 8 bits

(3) Bus Cycle Time/Instruction Cycle Time

The LC866448B/44B/40B/36B/32B/28B/24B/20B/16B/12B/08B are constructed to read ROM twice within one instruction cycle. It has 1.7 times more performance capability within the same instruction cycle compared to our 4-bit microcomputers (LC66000 series).

Bus cycle time indicates the speed to read ROM.

Bus cycle time	Cycle time	Clock divider	System clock oscillation	Oscillation Frequency	Voltage
0.5µs	1µs	1/1	Ceramic resonator oscillation	6MHz	4.5V to 6.0V
2µs	4µs	1/1	Ceramic resonator oscillation	3MHz	2.5V to 6.0V
7.5µs	15µs	1/1	RC resonator oscillation	800kHz	2.5V to 6.0V
183µs	366µs	1/2	Crystal oscillation	32.768kHz	2.5V to 6.0V

(4) Ports
- Input/output ports : 1 port (8 terminals : port 1)
  Input/output programmable in a bit
- 15V withstand Input/Output ports : 2 ports (12 terminals)
  Input/output port programmable in nibble unit : 1 port (8 terminals : port 0)
  (When the N-channel open drain output is selected, the data in a bit can be inputted.)
  Input/output port programmable in a bit : 1 port (4 terminals : port 3)
- Input port : 2 ports (14 terminals : port 7,8)
- VFD output port : 38 terminals
  Large current output for digit : 16 terminals
  Pull-down resistor option available
- Other function
  Input/output port : 1 port (6 terminals : port E)
  Input port : 2 ports (16 terminals : port C,D)

(5) VFD automatic dislay controller
- Segment/digit output pattern programmable
  Any segment/digit combination available
  VFD parallel-drive available
- 16-step dimmer function available

(6) AD converter
- 8-channel × 8-bit AD converter

(7) Serial-interface
- 1 channel × 16-bit serial-interface circuits
- 1 channel × 8-bit serial-interface circuits
- LSB first / MSB first function available

- Internal 8-bit baud-rate generator in common with two serial-interface circuits

(8) Timer

- Timer 0

16-bit timer/counter

2-bit prescaler + 8-bit programmable prescaler

Mode 0 : Two 8-bit timers with programmable prescaler

Mode 1 : 8-bit timer with programmable prescaler + 8-bit counter

Mode 2 : 16-bit timer with programmable prescaler

Mode 3 : 16-bit counter

The resolution of Timer is tCYC. (tCYC: cycle time)

- Timer 1

16-bit timer/PWM

Mode 0 : Two 8-bit timers

Mode 1 : 8-bit timer + 8-bit PWM

Mode 2 : 16-bit timer

Mode 3 : Variable-bit PWM (9-16 bits)

In Mode 0 and Mode 1,the resolution of Timer and PWM is tCYC.

In Mode 2 and Mode 3,the resolution of Timer and PWM selectable: tCYC or 1/2 tCYC by program

- Base timer

Every 500ms overflow system for a clock application (using 32.768kHz crystal oscillation for Base timer clock)

Every 976μs, 3.9ms, 15.6ms, 62.5ms overflow system (using 32.768kHz crystal oscillation for Base timer clock)

The Base timer clock selectable; 32.768kHz crystal oscillation, System clock, and programmable prescaler output of Timer 0

(9) Buzzer output

- The Buzzer sound frequency selectable; 4KHz, 2KHz (using 32.768kHz crystal oscillation for Base timer clock)

(10) Remote-control receiver circuit (Shares with the P73/INT3/T0IN terminal)

- Noise Rejection function (the time constant of noize rejection filter: 1tCYC/16tCYC/64tCYC)
(tCYC: instruction cycle time)

- Switch Polarity function

(11) Watchdog timer

- The watchdog timer is taken on RC outside

- Watchdog timer operation selectable: interrupt system, system reset

(12) Interrupt system

- 14-source 10-vectored interrupts :

1. External interrupt INT0 (include watchdog timer)
2. External interrupt INT1
3. External interrupt INT2, Timer/counter T0L (Lower 8-bit)
4. External interrupt INT3, Base timer
5. Timer/counter T0H (Upper 8-bit)
6. Timer T1L, Timer T1H
7. Serial-interface SIO0
8. Serial-interface SIO1
9. AD converter
10. VFD automatic display controller, Port 0

- Built-in Interrupt Priority control register

Microcontroller allows 3 levels of interrupt; low level, high level, and highest level of multiplex interrupt. It can specify a low level or a high level interrupt priority from INT2/T0L through port 0

(i.e. the above interrupt number from three through ten). It can also specify a low level or the highest level interrupt priority to INT0 and INT1.

(13) Real-time service operation

The Real-Time Service (RTS) functions the 4-byte data-transfer between the Special Function Registers at acknowledging the interrupt request.

The RTS starts within 1 instruction cycle-time and completes within 5 instructions cycle-time after occurring the interrupt request.

(14) Subroutine stack levels

- 128 levels (Max.): Stack area included in RAM area

(15) Multiplication and division

16-bit × 8-bit (7 instruction cycle times)

16-bit / 8-bit (7 instruction cycle times)

(16) Three oscillation circuits

- On-chip RC oscillation circuit using for the system clock.
- On-chip CF oscillation circuit using for the system clock.
- On-chip crystal oscillation circuit using for the system clock and for time-base clock.

(17) Standby function

- HALT mode function

The HALT mode is used to reduce power dissipation. In this operation mode, program execution is stopped. This operation mode can be released by interrupt request signals or the initial system reset request signal.

- HOLD mode function

The HOLD mode is used to freeze all the oscillations;
RC (internal), CF and Crystal oscillations. This mode can be released by the following operations.

- Reset terminal ($\overline{\text{RES}}$) set to Low level
- P70/INT0/T0IN, P71/INT1/T0IN terminals set to assigned level (programmable)
- Input a Port 0 interrupt condition

(18) Factory shipment

- QFP80E delivery form

(19) Development support tools

Evaluation (EVA) chip	:	LC866097
EPROM version	:	LC86E6449
One time version	:	LC86P6449
Emulator	:	EVA-86000 + ECB866400 (Evaluation chip board) + POD866400 (POD)

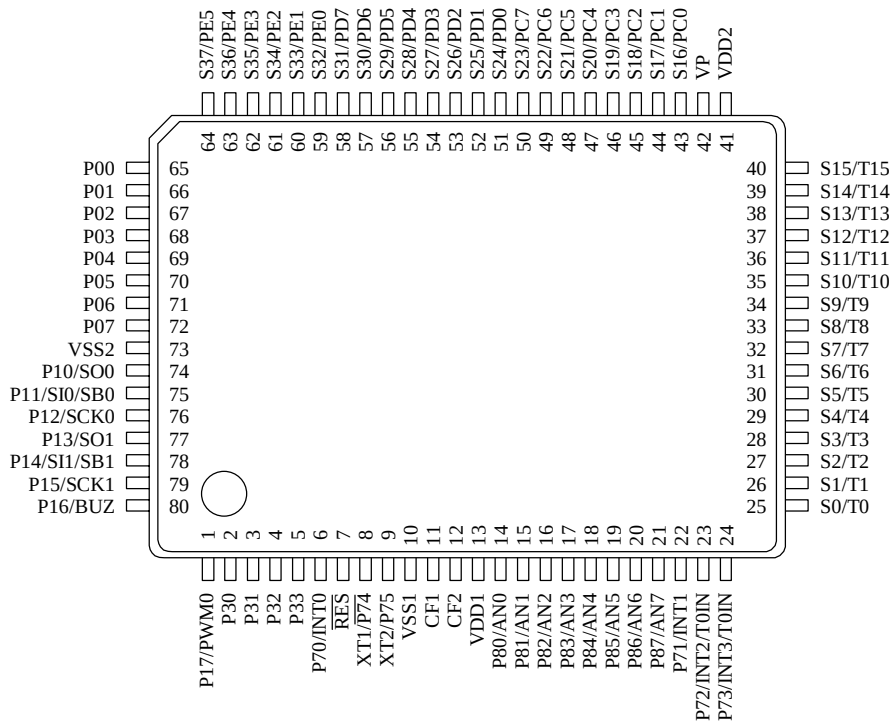
Notice for use

1. Set VDD=4.0V to 6.0V at using S16 to S37 as input port.
2. Follow the under table.

Frequency range of the system clock	Voltage range	Clock Divider	Note
15kHz to 30kHz	4.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 6MHz		1/1,1/2	
15kHz to 30kHz	2.5V to 6.0V	1/1	Can not use 1/2 divider
30kHz to 1.5MHz		1/1,1/2	
1.5MHz to 3MHz		1/2	Can not use 1/1 divider
Internal RC oscillation	4.5V to 6.0V	1/1,1/2	
	2.5V to 6.0V	1/2	Can not use 1/1 divider

Pin Assignment

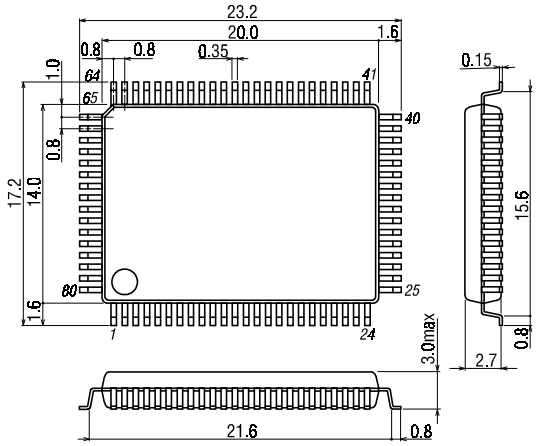
QIP80E



Package Dimension

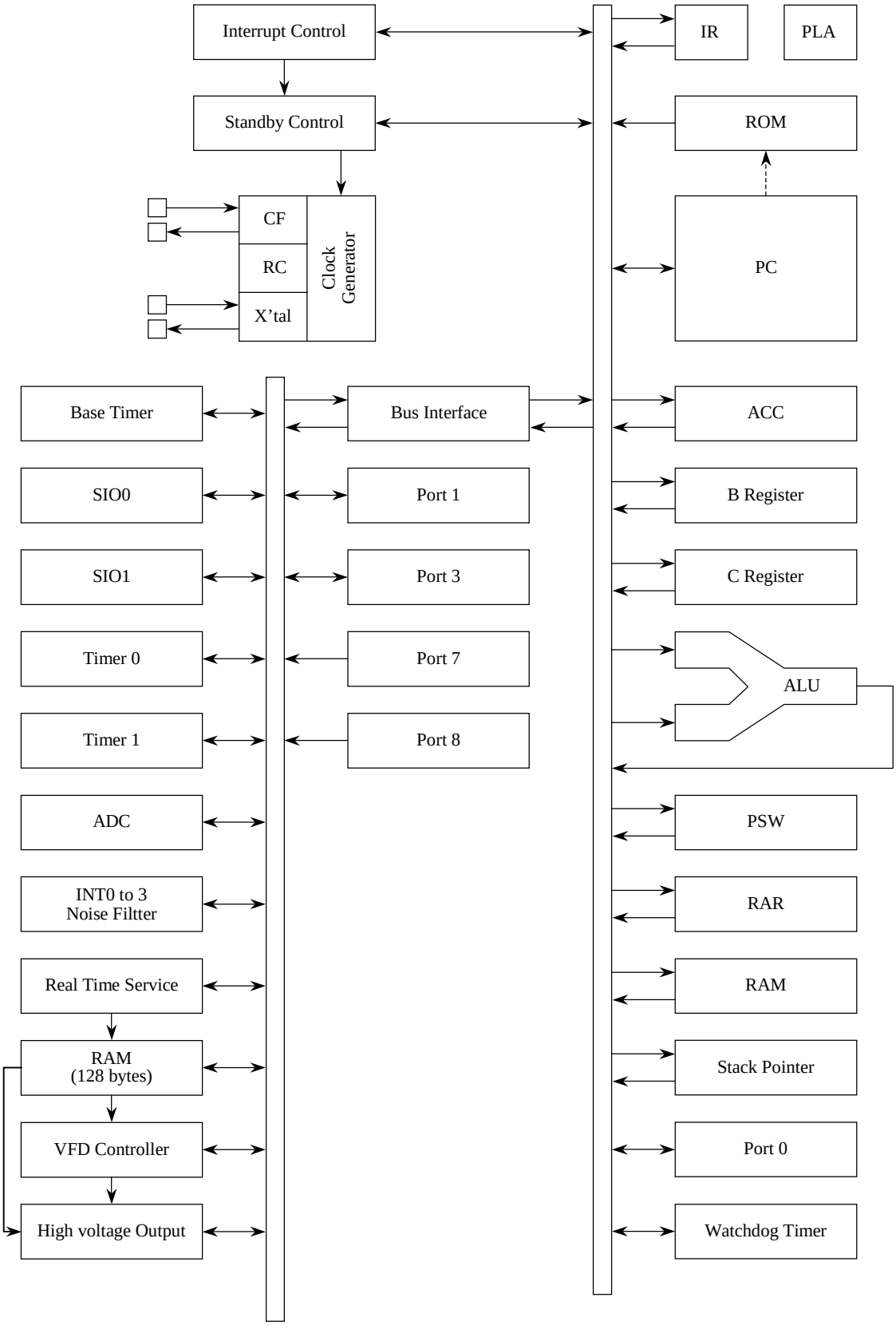
(unit : mm)

3174



SANYO : QIP-80E

System Block Diagram



Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th></tr>
<tr><td>VSS1,2</td><td>-</td><td>Power pin (-) Short-circuit VSS1 to VSS2.</td><td>-</td></tr>
<tr><td>VDD1,2</td><td>-</td><td>Power pin (+) *1 Refer to Notes</td><td>-</td></tr>
<tr><td>VP</td><td>-</td><td>Power pin (+) for the VFD output pull-down resistor</td><td>-</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>•8-bit input/output port
•Input for port 0 interrupt
•Input/output in nibble units
•Input for HOLD release
•15V withstand at N-channel open drain output</td><td>•Pull-up resistor :
Provided/Not provided (each nibble)
•Output form :
CMOS/N-channel open drain (each bit)</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in a bit unit
•Other pin functions
P10 SIO0 data output
P11 SIO0 data input/bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input/bus input/output
P15 SIO1 clock input/output
P16 Buzzer output
P17 Timer 1 output (PWM0 output)</td><td>Output form :
CMOS/N-channel open drain (each bit)</td></tr>
<tr><td>PORT3
P30 to P33</td><td>I/O</td><td>•4-bit input/output port
•Input/output in bit unit
•15V withstand at N-channel open drain output</td><td>Output form :
CMOS/N-channel open drain (each bit)</td></tr>
<tr><td>PORT7

P70

P71 to P75</td><td>

I/O

I</td><td>•6-bit input port
•Other pin functions
P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
P73 : INT3 input with noise filter/timer 0 event input
$\overline{P74}$: 32.768kHz crystal oscillation terminal XT1
P75 : 32.768kHz crystal oscillation terminal XT2
•Interrupt received forms, the vector addresses
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising & falling</th><th>high level</th><th>low level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>Pull-up resistor :
Provided/Not provided
(P70,71,72,73)
∗ $\overline{P74}$, P75 don’t have the pull-up resistor option.</td></tr>
</table>

Continue.

Pin name	I/O	Function description	Option
PORT8 P80 to 87	I	•8-bit input port •Other function AD input port (8 Port pins)	-
S0/T0 to S6/T6	O	Output for VFD display controller segment/timing in common	Pull-down resistor : Provided/Not provided (each nibble)
S7/T7 to S15/T15	O	•Output for VFD display controller segment/timing with internal pull-down resistor in common •Internal pull-down resistor output	
S16 to S31	I/O	•Output for VFD display controller segment •Other function S16 : High voltage input port PC0 S17 : High voltage input port PC1 S18 : High voltage input port PC2 S19 : High voltage input port PC3 S20 : High voltage input port PC4 S21 : High voltage input port PC5 S22 : High voltage input port PC6 S23 : High voltage input port PC7 S24 : High voltage input port PD0 S25 : High voltage input port PD1 S26 : High voltage input port PD2 S27 : High voltage input port PD3 S28 : High voltage input port PD4 S29 : High voltage input port PD5 S30 : High voltage input port PD6 S31 : High voltage input port PD7	Pull-down resistor : Provided/Not provided (each nibble)
S32 to S37	I/O	•Output for VFD display controller Segment •Other function S32 : High voltage I/O port PE0 S33 : High voltage I/O port PE1 S34 : High voltage I/O port PE2 S35 : High voltage I/O port PE3 S36 : High voltage I/O port PE4 S37 : High voltage I/O port PE5	Pull-down resistor : Provided/Not provided (each nibble)
$\overline{\text{RES}}$	I	Reset pin	-
XT1/ $\overline{\text{P74}}$	I	•Input pin for 32.768kHz crystal oscillation •Other function $\overline{\text{P74}}$ for input port •In case of non use, connect to VDD1.	-
XT2/P75	O	•Output pin for 32.768kHz crystal oscillation •Other function P75 for input port •In case of non use, At using as oscillator, should be left opened. At using as a port, connect to VDD1.	-
CF1	I	Input pin for the ceramic resonator oscillation	-
CF2	O	Output pin for the ceramic resonator oscillation	-

* All of port options (except pull-up resistor of port 0) can be specified in bit unit.

*A state of pins at reset

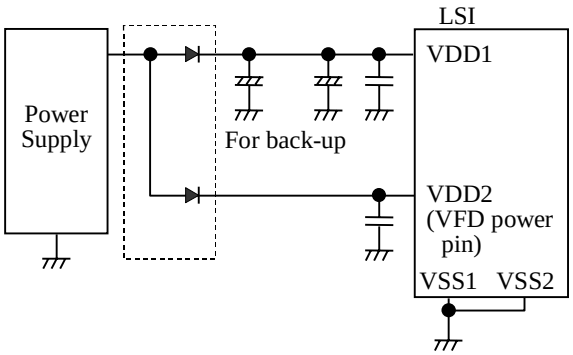
Pin name	Input/output mode	A state of pull-up resistor specified at pull-up option
Port 0	Input	Fixed pull-up resistor OFF
Ports 1,3	Input	Programmable pull-up resistor OFF
Ports 70,71,72,73	Input	Fixed pull-up resistor OFF

S0/T0 to S15/T15	P channel Transistor OFF
S16 to S37	P channel Transistor OFF

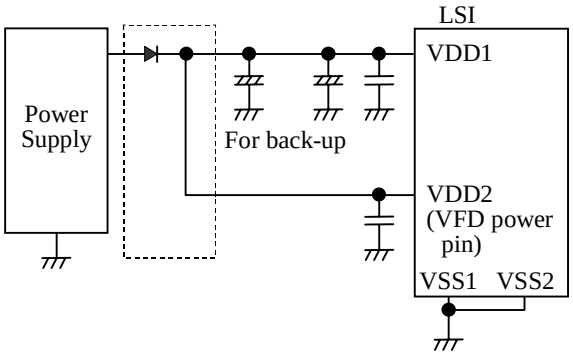
[Notes]

When connecting to the power supply, the power pins must be connected like following figure.

In case for the LC866448B/44B/40B/36B/32B/28B/24B/20B/16B/12B/08B



In case for the LC866432A/28A/24A/20A/16A/12A/08A



*1 Each of the power pins, VDD1 and VDD2, should be connected the capacitors for reducing the noise into the VDD1 pin.

1. Absolute Maximum Ratings at VSS1=VSS2=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	Ratings				unit
					VDD[V]	min.	typ.	max.	
Supply voltage		VDDMAX	VDD1,VDD2	VDD1=VDD2		-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71,72,73 •Ports $\overline{74}$,75 •Port 8 • $\overline{RES}$			-0.3		VDD+0.3	
		VI(2)	VP			VDD-45		VDD+0.3	
Output voltage		VO	S0/T0 to S15/T15			VDD-45		VDD+0.3	
Input/Output voltage		VIO(1)	•Port 1 •Port 70 •Ports 0, 3 at CMOS output option			-0.3		VDD+0.3	
		VIO(2)	Ports 0, 3 at N-ch open drain output option			-0.3		15	
		VIO(3)	S16 to S37			VDD-45		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 3	•CMOS output •At each pins		-10			mA
		IOPH(2)	S0/T0 to S15/T15	At each pins		-30			
		IOPH(3)	S16 to S37	At each pins		-15			
	Total output current	ΣIOAH(1)	Ports 0, 1, 3	The total of all pins		-30			
		ΣIOAH(2)	S0/T0 to S15/T15	The total of all pins		-55			
		ΣIOAH(3)	S16 to S37	The total of all pins		-115			
Low level output current	Peak output current	IOPL(1)	Ports 0, 1, 3	At each pins				20	
		IOPL(2)	Port 70	At each pins				15	
	Total output current	ΣIOAL(1)	Port 0	The total of all pins				40	
		ΣIOAL(2)	Ports 1,3	The total of all pins				40	
Maximum power dissipation		Pdmax	QFP80E	Ta=-30 to+70°C				480	mW
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-55		125	

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating Supply voltage	VDD(1)	VDD1=VDD2	0.98μs ≤ tCYC tCYC ≤ 400μs		4.5		6.0	V
	VDD(2)		3.9μs ≤ tCYC tCYC ≤ 400μs		2.5		6.0	
Hold voltage	VHD	VDD1=VDD2	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Pull-down voltage	VP	VP		2.5 to 6.0	-35		VDD	
Input high voltage	VIH(1)	Port 0 at CMOS output	Output disable	2.5 to 6.0	0.33VDD +1.0		VDD	
	VIH(2)	Port 0 at N-ch open drain output	Output disable	4.0 to 6.0	0.8VDD		13.5	
				2.5 to 4.0	0.75VDD		13.5	
	VIH(3)	•Port 1 •Ports 72,73 •Port 3 at CMOS output option	Output disable	2.5 to 6.0	0.75VDD		VDD	
	VIH(4)	Port 3 at N-ch open drain output option	Output disable Tr. OFF	4.5 to 6.0	0.8VDD		13.5	
				2.5 to 4.0	0.75VDD		13.5	
	VIH(5)	•Port 70 Port input/interrupt •Port 71 • $\overline{RES}$	Output N-channel Tr. OFF	2.5 to 6.0	0.75VDD		VDD	
	VIH(6)	Port 70 Watchdog timer	Output N-channel Tr. OFF	2.5 to 6.0	0.9VDD		VDD	
	VIH(7)	•Port 8 •Ports $\overline{74}$,75	Using as port	2.5 to 6.0	0.75VDD		VDD	
	VIH(8)	S16 to S37	Output P-channel Tr. OFF	4.0 to 6.0	0.33VDD +1.0		VDD	
Input low voltage	VIL(1)	Port 0 at CMOS output option	Output disable	2.5 to 6.0	VSS		0.2VDD	
	VIL(2)	Port 0 at N-ch open drain output	Output disable	2.5 to 6.0	VSS		0.25VDD	
	VIL(3)	•Ports 1,3 •Ports 72,73	Output disable	2.5 to 6.0	VSS		0.25VDD	
	VIL(4)	•Port 70 Port input/interrupt •Port 71 • $\overline{RES}$	Output N-channel Tr. OFF	2.5 to 6.0	VSS		0.25VDD	
	VIL(5)	Port 70 Watchdog timer	Output N-channel Tr. OFF	2.5 to 6.0	VSS		0.8VDD -1.0	
	VIL(6)	•Port 8 •Ports $\overline{74}$,75	Using as port	2.5 to 6.0	VSS		0.25VDD	
	VIL(7)	S16 to S37	Output P-channel Tr. OFF	4.0 to 6.0	VP		0.2VDD	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
				2.5 to 6.0	3.9		400	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0	To be deter-mined	6	To be deter-mined	MHz
	FmCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 1	2.5 to 6.0	To be deter-mined	3	To be deter-mined	
	FmRC		RC oscillation	2.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	2.5 to 6.0		32.768		kHz
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0..1	3.0	ms
	tmsCF(2)	CF1, CF2	•3MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0		0.1	3.0	
				2.5 to 6.0		0.1	3.0	
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 3	4.5 to 6.0		0.7	0.8	s
				2.5 to 6.0		1.4	2.2	

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	typ.	max.	unit
Input high current	IIH(1)	Ports 0,3 at open drain output	•Output disable •VIN=13.5V (including off-leakage current of the output Tr.)	2.5 to 6.0			5	μA
	IIH(2)	•Port 0 without pull-up MOS Tr. •Ports 1,3	•Output disable •Pull-up MOS Tr. OFF. •VIN=VDD (including off-leakage current of the output Tr.)	2.5 to 6.0			1	
	IIH(3)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	VIN=VDD	2.5 to 6.0			1	
	IIH(4)	$\overline{RES}$	VIN=VDD	2.5 to 6.0			1	
	IIH(5)	Ports $\overline{74}$,75	•Using as port •VIN=VDD	2.5 to 6.0			1	
	IIH(6)	S16 to S37 without pull-down resistor (Ports C,D,E)	•Output disable •VIN=VDD	2.5 to 6.0			1	
Input low current	IIL(1)	•Ports 1,3 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. •VIN=VSS (including off-leakage current of the output Tr.)	2.5 to 6.0	-1			
	IIL(2)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	VIN=VSS	2.5 to 6.0	-1			
	IIL(3)	$\overline{RES}$	VIN=VSS	2.5 to 6.0	-1			
	IIL(4)	Ports $\overline{74}$,75	•VIN=VSS •Using as port	2.5 to 6.0	-1			
Output high voltage	VOH(1)	Ports 0,1,3 of CMOS output	IOH=-1.0mA	4.5 to 6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	2.5 to 6.0	VDD-0.5			
	VOH(3)	S0/T0 to S15/T15	IOH=-20mA	4.5 to 6.0	VDD-1.8			
	VOH(4)		•IOH=-1mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0	VDD-1			
	VOH(5)	S16 to S37	IOH=-5mA	4.5 to 6.0	VDD-1.8			
	VOH(6)		The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0	VDD-1			
Output low voltage	VOL(1)	Ports 0,1,3	IOL=10mA	4.5 to 6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(3)		•IOL=1.0mA •The current of any unmeasurement pin is not over 1mA.	2.5 to 6.0			0.4	
	VOL(4)	Port 70	IOL=1mA	4.5 to 6.0			0.4	
	VOL(5)		IOL=0.5mA	2.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0,1,3 •Ports 70,71,72,73	VOH=0.9VDD	4.5 to 6.0	15	40	70	kΩ
				2.5 to 4.5	25	70	150	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Output off-leak current	IOFF(1)	S0/T0 to S6/T6, S16 to S37 without pull-down resistor	•Output P-channel Tr. OFF •VOUT=VSS	2.5 to 6.0	-1			μA
	IOFF(2)		•Output P-channel Tr. OFF •VOUT=VDD-40V	2.5 to 6.0	-30			
Resistance of the low level hold Tr.	Rinpd	S16 to S37	•Output P-channel Tr. OFF •Using as input ports	4.0 to 6.0		200		kΩ
High voltage pull-down resistor	Rpd	S0/T0 to S15/T15, S16 to S37 without pull-down resistor	•Output P-channel Tr. OFF •VOUT=3V •Vp=-30V	5.0	60	100	200	
Hysteresis voltage	VHIS	•Port 1 •Ports 70,71,72,73 • $\overline{RES}$	Output disable	2.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •VIN=VSS for all unmeasured terminals. •Ta=25°C	2.5 to 6.0		10		pF

4. Serial input/output characteristics / Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0,SCK1	Refer to figure 5	2.5 to 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0,SCK1	•Use pull-up resistor (1kΩ) in the open drain output. •Refer to figure 5	2.5 to 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set-up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0	0.1			μs
						2.5 to 6.0	0.4			
	Data hold time		tCKI			4.5 to 6.0	0.1			
						2.5 to 6.0	0.4			
Serial output	Output delay time (External clock using for serial transfer clock)		tCKO(1)	•SO0,SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) in the open drain output. •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0			7/12 tCYC +0.2	
						2.5 to 6.0			7/12 tCYC +1	
	Output delay time (Internal clock using for serial transfer clock)		tCKO(2)			4.5 to 6.0			1/3 tCYC +0.2	
						2.5 to 6.0			1/3 tCYC +1	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock selected to 1/1.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock selected to 1/16.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	32			
	tPIH(4) tPIL(4)	INT3/T0IN (The noise rejection clock selected to 1/64.)	•Interrupt acceptable •Timer0-countable	2.5 to 6.0	128			
	tPIL(5)	$\overline{RES}$	Reset acceptable	2.5 to 6.0	200			μs

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
Resolution	N			4.5 to 6.0		8		bit
Absolute precision (Note 2)	ET			4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 to AN7		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0			1	μA
	IAINL		VAIN=VSS	4.5 to 6.0	-1			

(Note 2) Absolute precision excepts the quantizing error (±1/2 LSB).

(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS1=VSS2=0V

Parameter	Symbol	Pins	Conditions	Ratings				unit
				VDD[V]	min.	typ.	max.	
Current dissipation during basic operation (Note 4)	IDDOP(1)		•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5 to 6.0		10	25	mA
	IDDOP(2)		•FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		3	9	
	IDDOP(3)			2.5 to 4.5		1.5	5	
	IDDOP(4)		•FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5 to 6.0		0.7	3.4	
	IDDOP(5)			2.5 to 4.5		0.4	2.8	
	IDDOP(6)		•FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		35	130	μA
	IDDOP(7)			2.5 to 4.5		15	70	

Continue.

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Current dissipation in HALT mode (Note 4)	IDDHALT(1)		•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/1 divided	4.5 to 6.0		5	14	mA
	IDDHALT(2)		•HALT mode •FmCF=3MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		2.2	7	
	IDDHALT(3)			2.5 to 4.5		0.8	4	
	IDDHALT(4)		•HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation •1/2 divided	4.5 to 6.0		400	1600	μA
	IDDHALT(5)			2.5 to 4.5		200	1300	
	IDDHALT(6)		•HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : crystal oscillation •Internal RC oscillation stops •1/2 divided	4.5 to 6.0		25	100	
	IDDHALT(7)			2.5 to 4.5		8	55	
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)		HOLD mode	4.5 to 6.0		0.05	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main-clock)

Oscillation type	Maker	Oscillator	C1	C2
6MHz ceramic resonator oscillation	Murata	CSA6.00MG	33pF	33pF
		CST6.00MGW	on chip	
	Kyocera	KBR-6.0MSB	33pF	33pF
		PBRC6.00A(chip type)	33pF	33pF
		KBR-6.0MKC	on chip	
		PBRC6.00B(chip type)		
3MHz ceramic resonator oscillation	Murata	CSA3.00MG	33pF	33pF
		CST3.00MGW	on chip	
	Kyocera	KBR-3.0MS	47pF	47pF

* Both C1 and C2 must be use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub-clock)

Oscillation type	Maker	Oscillator	C3	C4	Rd
32.768kHz crystal oscillation	EPSON	C-002RX	18pF	18pF	680kΩ

* Both C3 and C4 must be use J rank (±5%) and CH characteristics.
(Not in need of high precision, use K rank (±10%) and SL characteristics.)

(Notes) • Please place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length since the circuit pattern affects the oscillation frequency.
• If you use other oscillators herein, we provide no guarantee for the characteristics.

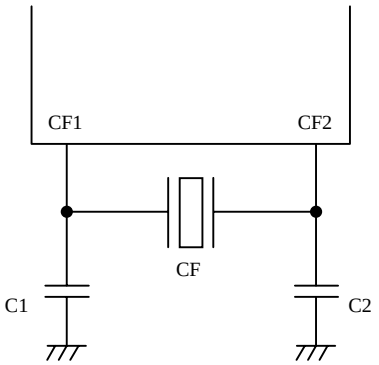


Figure 1 Main-clock circuit
Ceramic resonator oscillation

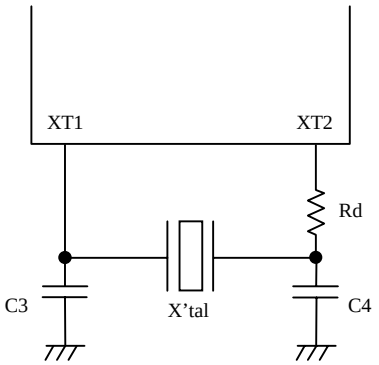


Figure 2 Sub-clock circuit
Crystal oscillation

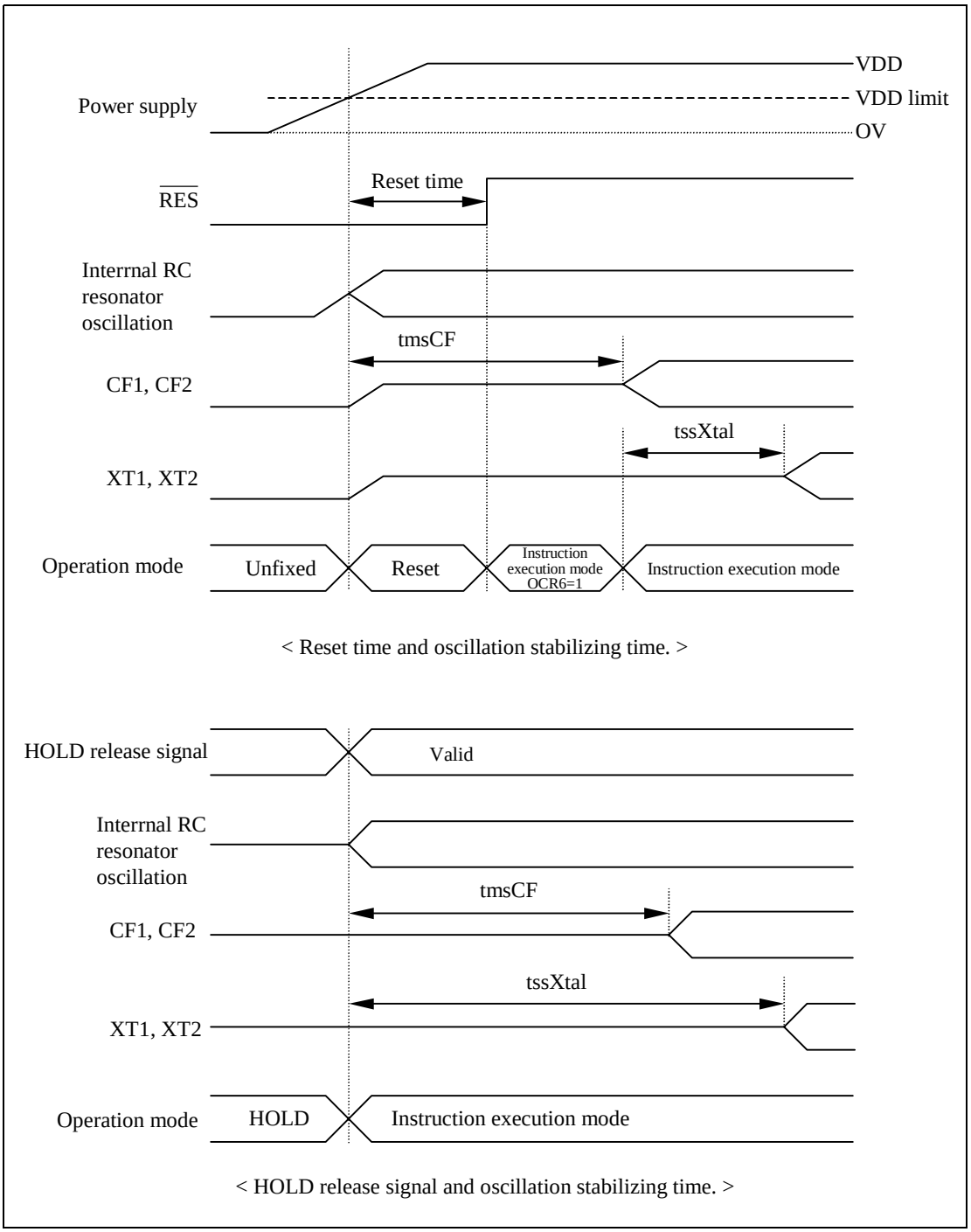
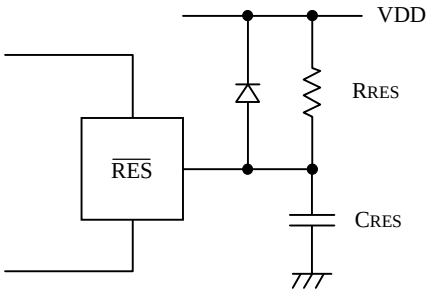


Figure 3 Oscillation stable time



(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit

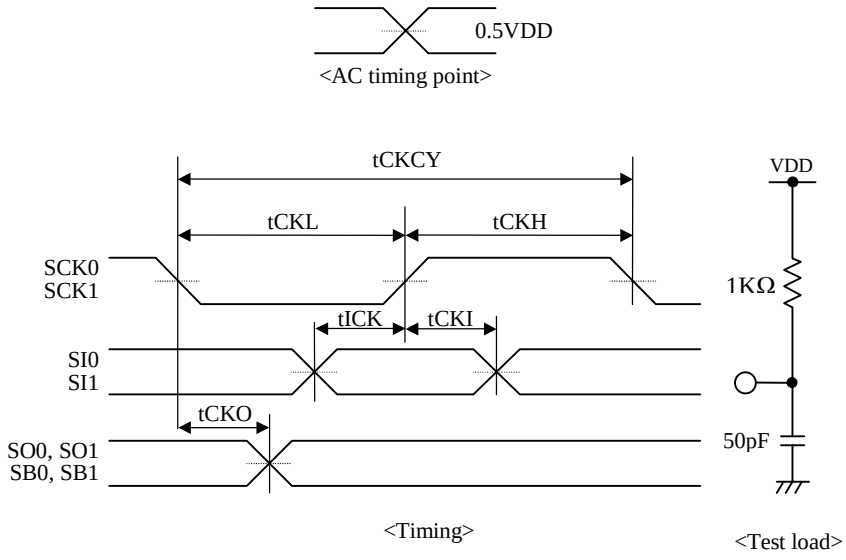


Figure 5 Serial input / output test condition

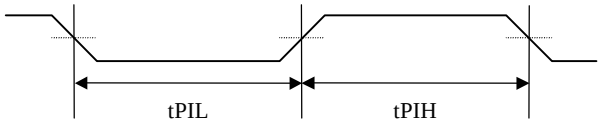


Figure 6 Pulse input timing condition

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