Ordering number : EN*4965

CMOS LSI

**SANYO**

# LC75741E, 75741W

## 1/2 Duty VFD Driver for Frequency Displays

**Preliminary**

## Overview

The LC75741E and LC75741W are 1/2 duty VFD drivers for use in electronic tuning frequency displays controlled by a microcontroller. These products can directly drive VFD displays with up to 106 segments.

## Functions and Features

- 106 segment outputs
- Noise reduction circuit built into the output drivers.
- Display and dimmer data communication with the controller using the CCB* format.
- High generality, since display data is displayed directly without decoder intervention
- All segments can be turned off with the $\overline{BLK}$ pins.
- Package: QFP64E (LC75741E)
          SQFP64 (LC75741W)
- Note: * CCB is Sanyo's original bus format with address management for all Sanyo products.
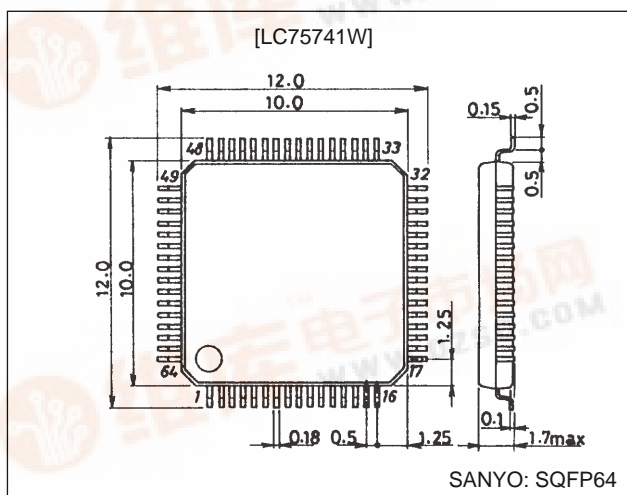
## Package Dimensions

unit: mm

**3159-QFP64E**



[LC75741E]

SANYO: QIP64E
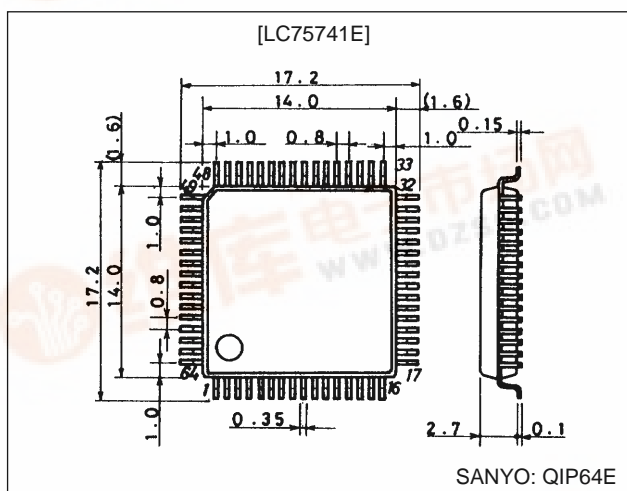
unit: mm

**3190-SQFP64**



[LC75741W]

SANYO: SQFP64

# Specifications

## Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | −0.3 to +6.5 | V |
| | $V_{FL}$ max | $V_{FL}$ | −0.3 to +21.0 | V |
| Input voltage | $V_{IN}1$ | DI, CL, CE, $\overline{BLK}$ | −0.3 to +6.5 | V |
| | $V_{IN}2$ | OSCI | −0.3 to $V_{DD}$ + 0.3 | V |
| Output voltage | $V_{OUT}1$ | S1 to S53, G1, G2 | −0.3 to $V_{FL}$ + 0.3 | V |
| | $V_{OUT}2$ | OSCO | −0.3 to $V_{DD}$ + 0.3 | V |
| Output current | $I_{OUT}1$ | S1 to S53 | 5 | mA |
| | $I_{OUT}2$ | G1, G2 | 60 | mA |
| Allowable power dissipation | Pd max | Ta = 85°C | 400 (LC75741E) | mW |
| | | | 300 (LC75741W) | mW |
| Operating temperature | Topr | | −40 to +85 | °C |
| Storage temperature | Tstg | | −50 to +150 | °C |

## Allowable Operating Ranges at Ta = –40 to +85°C, $V_{DD}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 4.5 | 5.0 | 5.5 | V |
| | $V_{FL}$ | $V_{FL}$ | 8 | 12 | 18 | V |
| Input high level voltage | $V_{IH}1$ | DI, CL, CE, $\overline{BLK}$ | 0.8 $V_{DD}$ | | 5.5 | V |
| | $V_{IH}2$ | OSCI | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| Input low level voltage | $V_{IL}1$ | DI, CL, CE, $\overline{BLK}$ | 0 | | 0.2 $V_{DD}$ | V |
| | $V_{IL}2$ | OSCI | 0 | | 0.3 $V_{DD}$ | V |
| Guaranteed oscillator range | $f_{OSC}$ | OSCI, OSCO | 0.4 | 1.6 | 3.0 | MHz |
| Recommended external resistance | $R_{OSC}$ | OSCI, OSCO | | 20 | | kΩ |
| Recommended external capacitance | $C_{OSC}$ | OSCI, OSCO | | 47 | | pF |
| Low level clock pulse width | $t_{øL}$ | CL: Figure 1 | 0.5 | | | µs |
| High level clock pulse width | $t_{øH}$ | CL: Figure 1 | 0.5 | | | µs |
| Data setup time | $t_{ds}$ | DI, CL: Figure 1 | 0.5 | | | µs |
| Data hold time | $t_{dh}$ | DI, CL: Figure 1 | 0.5 | | | µs |
| CE wait time | $t_{cp}$ | CE, CL: Figure 1 | 0.5 | | | µs |
| CE setup time | $t_{cs}$ | CE, CL: Figure 1 | 0.5 | | | µs |
| CE hold time | $t_{ch}$ | CE, CL: Figure 1 | 0.5 | | | µs |
| $\overline{BLK}$ switching time | $t_c$ | $\overline{BLK}$, CE: Figure 3 | 10 | | | µs |

## Electrical Characteristics in the Allowable Operating Ranges

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input high level current | $I_{IH}$ | DI, CL, CE, $\overline{BLK}$, OSCI: VI = 5.5 V | | | 5 | µA |
| Input low level current | $I_{IL}$ | DI, CL, CE, $\overline{BLK}$, OSCI: VI = 0 V | −5 | | | µA |
| Output high level voltage | $V_{OH}1$ | S1 to S53: $I_O$ = 2 mA | $V_{FL}$ − 0.6 | | | V |
| | $V_{OH}2$ | G1, G2: $I_O$ = 25 mA | $V_{FL}$ − 0.6 | | | V |
| | $V_{OH}3$ | G1, G2: $I_O$ = 50 mA | $V_{FL}$ − 1.3 | | | V |
| | $V_{OH}4$ | OSCO: $I_O$ = 0.5 mA | $V_{DD}$ − 2.0 | | | V |
| Output low level voltage | $V_{OL}1$ | S1 to S53, G1, G2: $I_O$ = −5 µA, Ta = 25°C | | 0.25 | 0.5 | V |
| | $V_{OL}2$ | OSCO: $I_O$ = −0.5 mA | | | 2.0 | V |
| Oscillator frequency | $f_{OSC}$ | $R_{OSC}$ = 20 kΩ, $C_{OSC}$ = 47 pF | | 1.6 | | MHz |
| Hysteresis voltage | $V_H$ | DI, CL, CE, $\overline{BLK}$ | | 0.1 $V_{DD}$ | | V |
| Current drain | $I_{DD}$ | Output open: $f_{OSC}$ = 1.6 MHz | | | 10 | mA |

1.  When CL is stopped at the low level
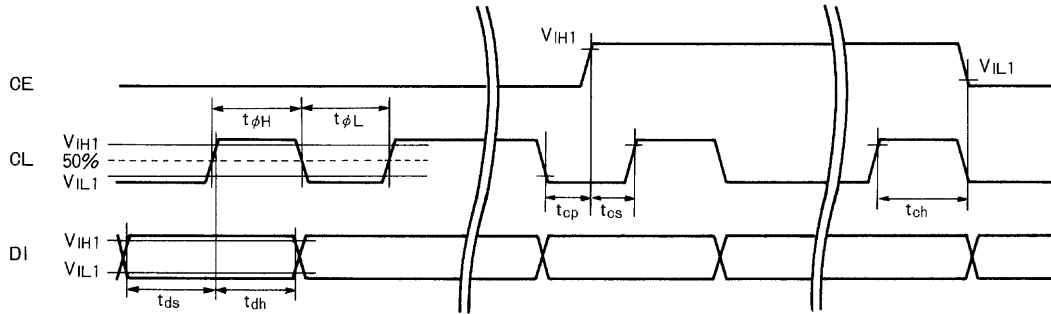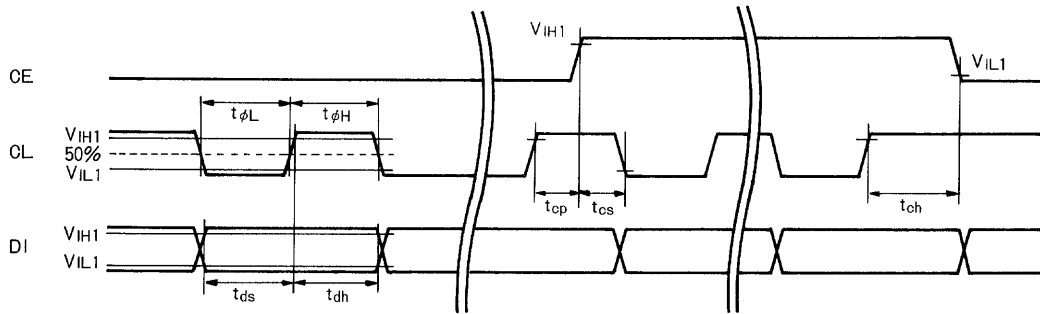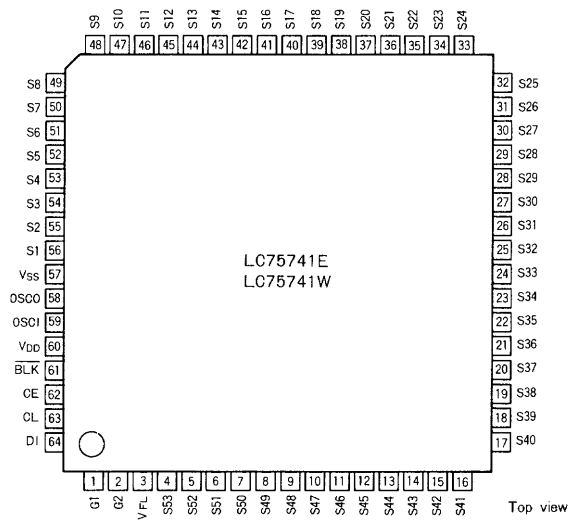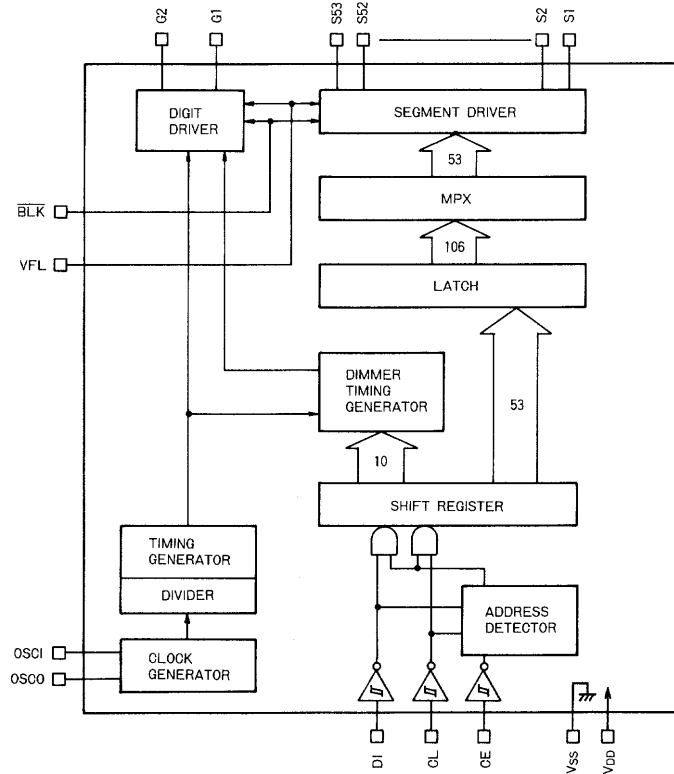


2.  When CL is stopped at the high level



**Figure 1**

## Pin Assignment



Top view

## Block Diagram



## Pin Functions

| Pin | Pin No. | I/O | Function |
|---|---|---|---|
| $V_{FL}$ | 3 | — | Driver block power supply. A voltage of between 8.0 and 18.0 V must be supplied. |
| $V_{DD}$ | 60 | — | Logic block power supply. A voltage of between 4.5 and 5.5 V must be supplied. |
| $V_{SS}$ | 57 | — | Power supply. Must be connected to ground. |
| OSCI, OSCO | 59 58 | I/O | Oscillator connections. An oscillator circuit is formed by connecting an external resistor and capacitor at these pins. |
| $\overline{BLK}$ | 61 | I | Display off control input<br>$\overline{BLK}$ = low ($V_{SS}$): Display off (S1 to S53, G1 and G2 = low)<br>$\overline{BLK}$ = high ($V_{DD}$): Display on<br>Note that serial data transfers are still allowed when display is turned off using this pin. |
| CL | 63 | I | Serial data transfer inputs. Connect to the system microcontroller.<br>CL: Synchronization clock<br>DI: Transfer data<br>CE: Chip enable |
| DI | 64 | | |
| CE | 62 | | |
| G1, G2 | 1, 2 | O | Digit outputs. The frame frequency $f_O$ is $f_{OSC}/4096$ Hz. |
| S1 to S53 | 56 to 4 | O | Segment outputs for displaying the display data transferred by serial data input. |

## Serial Data Transfer Format

1. When CL is stopped at the low level
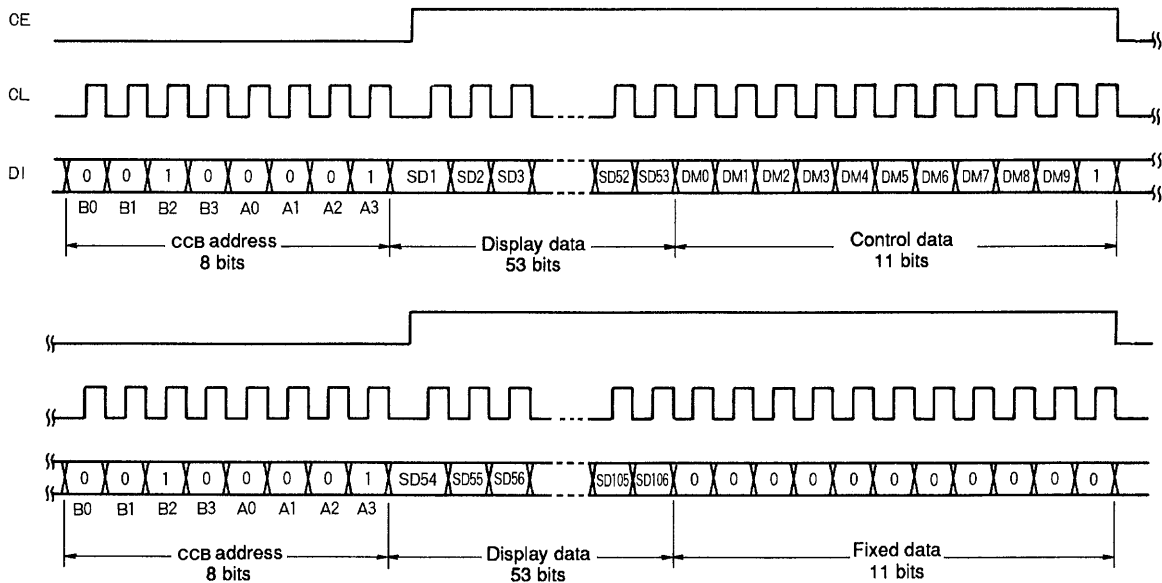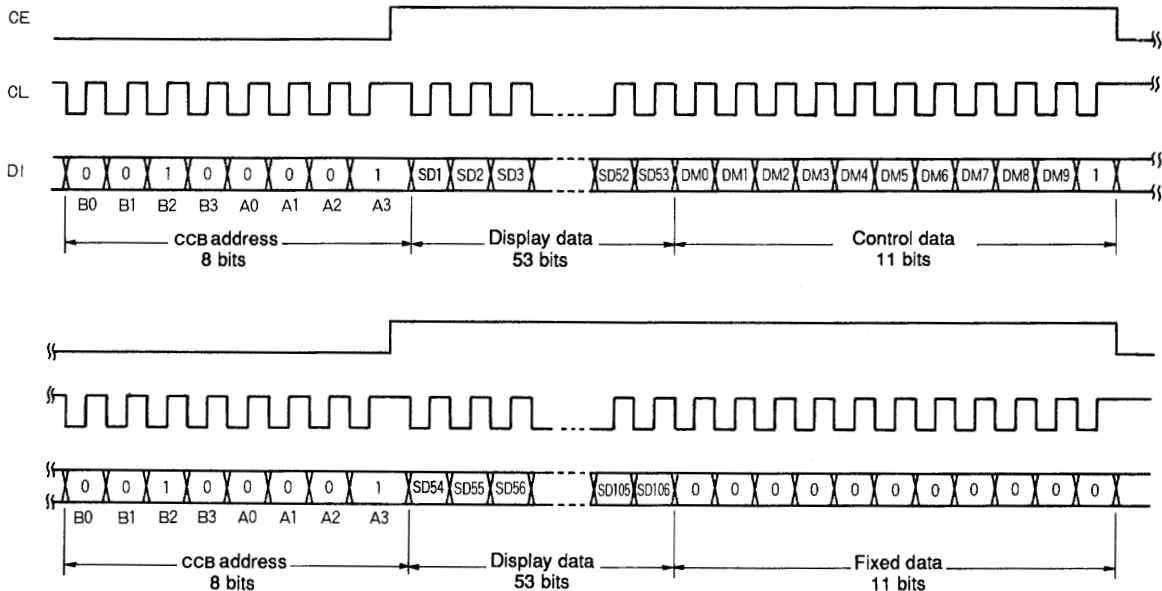


2. When CL is stopped at the high level



**Figure 2**

CCB address: Transfer $00100001_B$ as shown in Figure 2.

DM0 to DM9: Dimmer data

This data controls the duty of the G1 and G2 digit output pins, and consists of 10 bits with DM0 being the LSB. Note that the intensity of the display can be adjusted by controlling the duty of the G1 and G2 digit output pins.

SD1 to SD53: Display data for the G1 digit output pin.

SDn (n = 1 to 53) = 1: On

SDn (n = 1 to 53) = 0: Off

SD54 to SD106: Display data for the G2 digit output pin.

SDn (n = 54 to 106) = 1: On

SDn (n = 54 to 106) = 0: Off

## Correspondence between Display Data (SD1 to SD106) and Segment Output Pins

| Segment output pin | G1 | G2 | | Segment output pin | G1 | G2 |
|---|---|---|---|---|---|---|
| S1 | SD1 | SD54 | | S28 | SD28 | SD81 |
| S2 | SD2 | SD55 | | S29 | SD29 | SD82 |
| S3 | SD3 | SD56 | | S30 | SD30 | SD83 |
| S4 | SD4 | SD57 | | S31 | SD31 | SD84 |
| S5 | SD5 | SD58 | | S32 | SD32 | SD85 |
| S6 | SD6 | SD59 | | S33 | SD33 | SD86 |
| S7 | SD7 | SD60 | | S34 | SD34 | SD87 |
| S8 | SD8 | SD61 | | S35 | SD35 | SD88 |
| S9 | SD9 | SD62 | | S36 | SD36 | SD89 |
| S10 | SD10 | SD63 | | S37 | SD37 | SD90 |
| S11 | SD11 | SD64 | | S38 | SD38 | SD91 |
| S12 | SD12 | SD65 | | S39 | SD39 | SD92 |
| S13 | SD13 | SD66 | | S40 | SD40 | SD93 |
| S14 | SD14 | SD67 | | S41 | SD41 | SD94 |
| S15 | SD15 | SD68 | | S42 | SD42 | SD95 |
| S16 | SD16 | SD69 | | S43 | SD43 | SD96 |
| S17 | SD17 | SD70 | | S44 | SD44 | SD97 |
| S18 | SD18 | SD71 | | S45 | SD45 | SD98 |
| S19 | SD19 | SD72 | | S46 | SD46 | SD99 |
| S20 | SD20 | SD73 | | S47 | SD47 | SD100 |
| S21 | SD21 | SD74 | | S48 | SD48 | SD101 |
| S22 | SD22 | SD75 | | S49 | SD49 | SD102 |
| S23 | SD23 | SD76 | | S50 | SD50 | SD103 |
| S24 | SD24 | SD77 | | S51 | SD51 | SD104 |
| S25 | SD25 | SD78 | | S52 | SD52 | SD105 |
| S26 | SD26 | SD79 | | S53 | SD53 | SD106 |
| S27 | SD27 | SD80 | | | | |

For example, the table below lists the segment output states for the S11 segment output pin.

| Display data | | Segment output pin (S11) state |
|---|---|---|
| SD11 | SD64 | |
| 0 | 0 | Both segments for the G1 and G2 digit output pins are off |
| 0 | 1 | Segment for the G2 digit output pin is on |
| 1 | 0 | Segment for the G1 digit output pin is on |
| 1 | 1 | Both segments for the G1 and G2 digit output pins are on |

## $\overline{\text{BLK}}$ and the Display Control

Since the LSI internal data (SD1 to SD106 and $\overline{\text{DM0}}$ to DM9) is undefined when power is first applied, the display is off (S1 to S53, G1 and G2 = low) by setting the $\overline{\text{BLK}}$ pin low at the same time as power is applied. Then, meaningless display at power-on can be prevented by transferring all 144 bits of serial data from the controller while the display is off and setting $\overline{\text{BLK}}$ pin high after the transfer completes. (See Figure 3.)

## Power Supply Sequence

Observe the following sequences when turning the power on and off. (See Figure 3.)
• Power on: Logic block power supply ($V_{DD}$) on → Driver block power supply ($V_{FL}$) on
• Power off: Driver block power supply ($V_{FL}$) off → Logic block power supply ($V_{DD}$) off

t1 > 0
t2 > 0
t3 > 0　(t2 > t3)
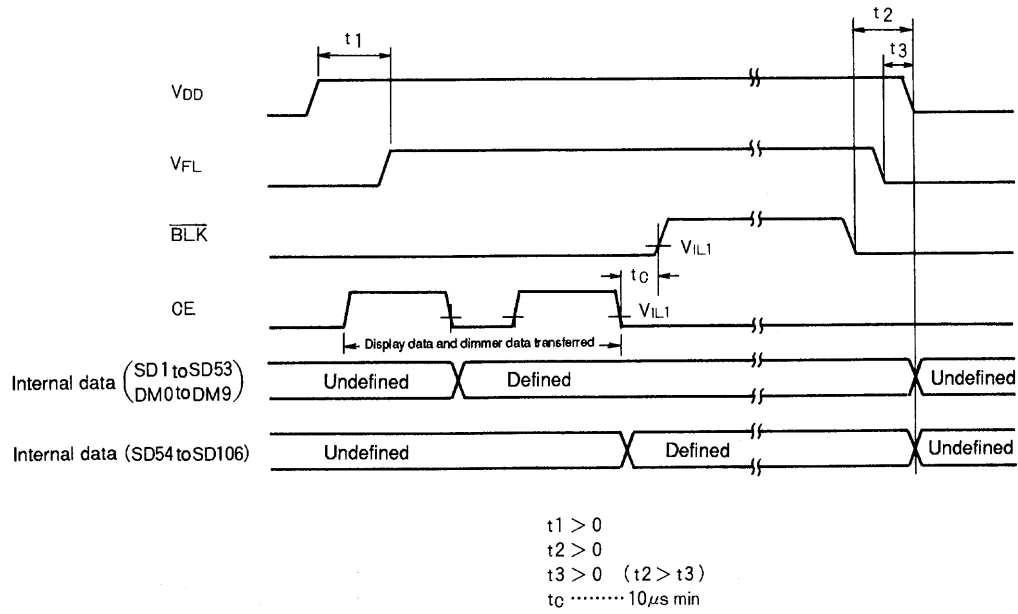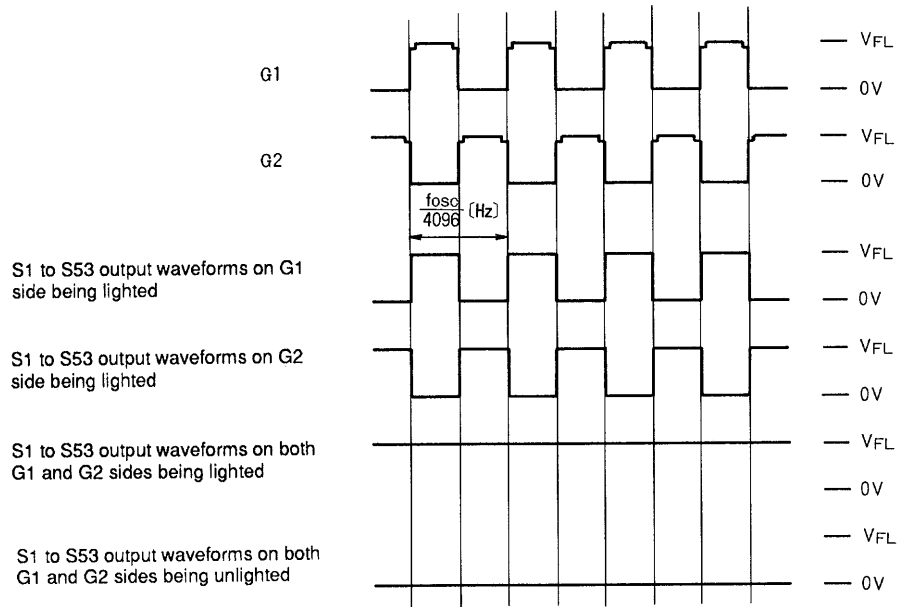tc ·········10μs min

**Figure 3**

## Output Waveforms (S1 to S53)
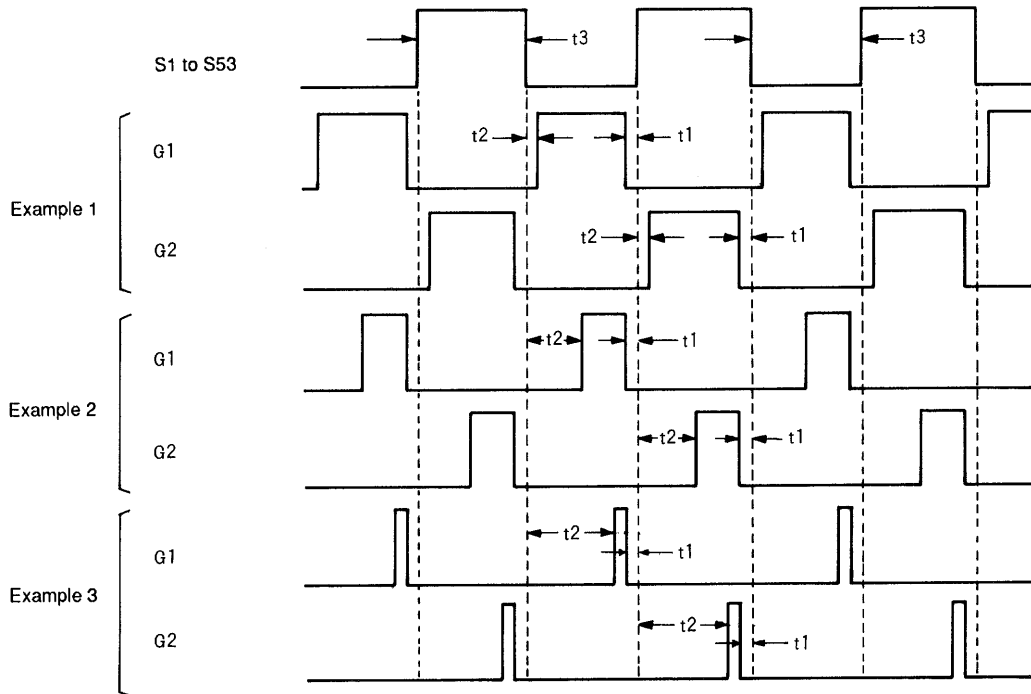
## Relation between Segment and Digit Outputs



**Figure 4**

### Description

1. Consider the examples shown in Figure 4, where data is set up so that the segment outputs S1 to S53 output a low level on the G1 digit output timing and a high level on the G2 digit output timing. (Here, the G2 side being lighted)

2. The waveforms for G1 and G2 in example 1 are output when the 10 bits of dimmer data (DM0 to DM9) are set to $3FE_H$. The relation between t1 and the oscillator frequency $f_{OSC}$ is:

   $$t1 = 2/f_{OSC}$$

   For example, if $f_{OSC}$ is 1.6 [MHz]:
   t1 = 2/1.6 [MHz] = 1.25 [μs]. Note that t1 and t2 will be the same period in example 1.

3. The waveforms for G1 and G2 in example 2 are those when the dimmer data (DM0 to DM9) are set to a smaller value. Although the time t1, which is from the point where digit output falls to segment output changes, does not change, the time t2, which is from the point where segment output changes to the time the digit output rises, becomes longer. When the dimmer data (DM0 to DM9) are set to $0FF_H$ and $f_{OSC}$ is 1.6 [MHz],

   $$\text{the frame frequency } f_{frame} = 1/(t3 \times 2)$$
   $$= f_{OSC}/4096$$
   $$= 391 \text{ [Hz]},$$
   $$\text{and } t3 = 1.28 \text{ [ms]}.$$

   $$\text{Therefore, } t2 = \frac{(1.28 \text{ [ms]} - 1.25 \text{ [μs]} \times 2) \times (3FF_H - 0FF_H)}{1023} = 0.96 \text{ [ms]}.$$

4. When the dimmer data (DM0 to DM9) are set to an even smaller value, the time t2, which is from the point where segment output changes to the time the digit output rises, becomes even longer, as in example 3. Note that t1 does not change here, either.

## Sample Application Circuit
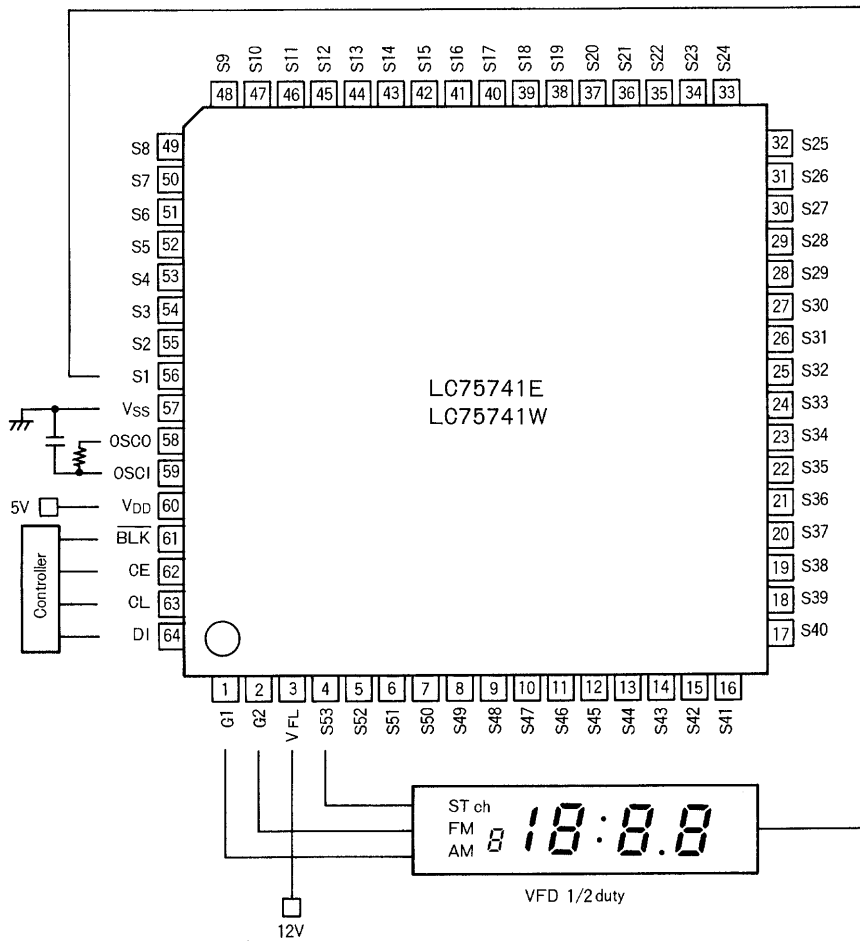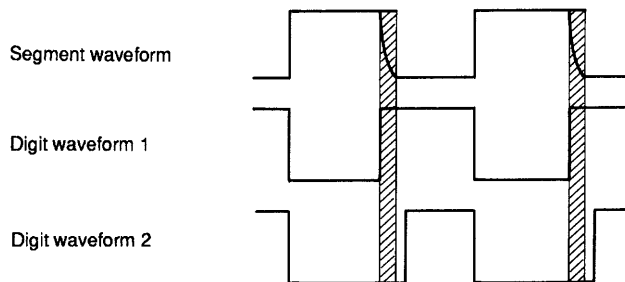


## Usage Notes

1. Segment and digit waveforms



**Figure 5**

The segment waveform is distorted by the wiring of the VFD panel used, and furthermore, in the case of being used with essentially no dimming as in the digit waveform 1, as shown in Figure 5, the VFD panel glow dimly. By carefully considering the segment waveform, it can be seen that this problem can be resolved by applying an adequate amount of dimming, as shown in digit waveform 2. When $f_{OSC}$ is 1.6 [MHz], we recommend using 10 bits of dimmer data in the range $000_H$ to $3E0_H$.

2. Serial data transfer
   Since display data is transferred in two operations as shown in Figure 2, we recommend that all display data be transferred within 30 [ms] to prevent degradation of the visual quality of the displayed image.