

CMOS LSI



LC75822E, 75822W

LCD Display Drivers



Overview

The LC75822E and LC75822W are general-purpose LCD display drivers that can be used for frequency display in microprocessor-controlled radio receivers and in other display applications.

Features

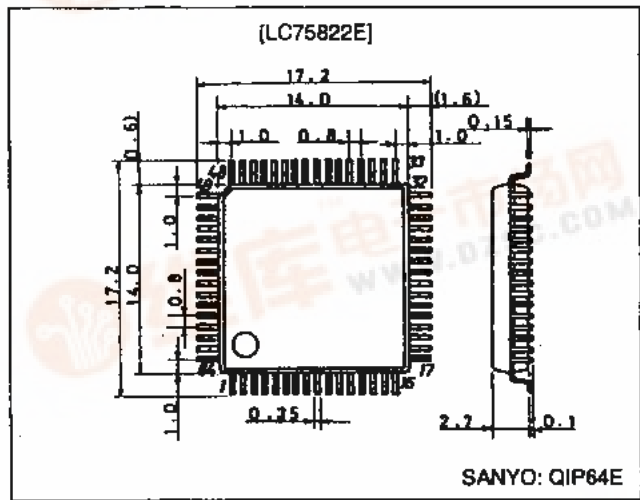
- 53 segment outputs (the maximum for static drive)
- Two drive types: static (1/1) duty (53 segments) and 1/2 duty (104 segments)
- Serial data input supports CCB* format communication with the system controller
- \overline{INH} pin for turning off all display output
- The LC75822 is a CCB version of the LC75821 product.

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

Package Dimensions

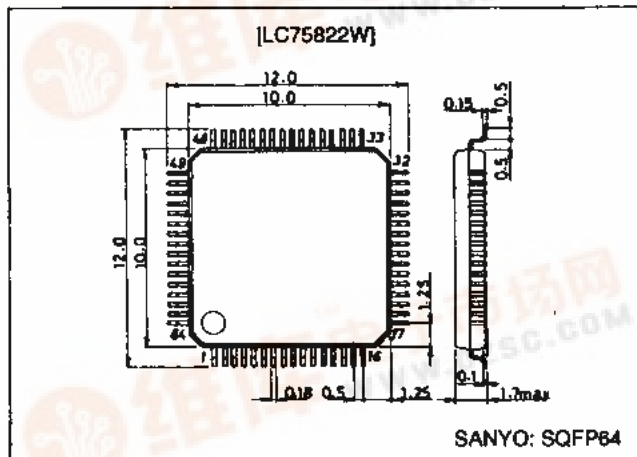
unit: mm

3159-QFP64E



unit: mm

3190-SQFP64



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Specifications

Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{DD max}	V _{DD}	-0.3 to +7.0	V
	V _{LCD}	V _{LCD}	-0.3 to V _{DD} + 0.3	V
Input voltage	V _{IN1}	CE, CL, DI, INH	-0.3 to +7.0	V
	V _{IN2}	OSC: output off	-0.3 to V _{DD} + 0.3	V
Output voltage	V _{OUT}	OSC: output off	-0.3 to V _{DD} + 0.3	V
Output current	I _{OUT1}	S1 to S53	100	μA
	I _{OUT2}	COM1, COM2	1.0	mA
Allowable power dissipation	Pd max	Ta = 85°C	100	mW
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at Ta = -40 to +85°C, VSS = 0 V

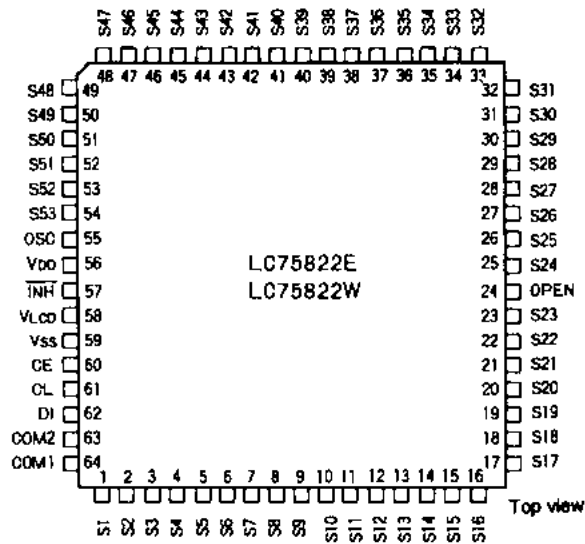
Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V _{DD}	V _{DD}	3.0		6.5	V
	V _{LCD}	V _{LCD}	3.0		V _{DD}	V
Input high-level voltage	V _{IH1}	INH	0.7 V _{DD}		6.5	V
Input low-level voltage	V _{IL1}	INH	0		0.3 V _{DD}	V
Input high-level voltage	V _{IH2}	CE, CL, DI	0.8 V _{DD}		6.5	V
Input low-level voltage	V _{IL2}	CE, CL, DI	0		0.2 V _{DD}	V
Recommended external resistance	R _{OSC}	OSC		51		kΩ
Recommended external capacitance	C _{OSC}	OSC		680		pF
Guaranteed oscillation range	f _{OSC}	OSC	25	50	100	kHz
Clock low-level pulse width	t _{gL}	CL	250			ns
Clock high-level pulse width	t _{gH}	CL	250			ns
Data setup time	t _{ds}	CL, DI	250			ns
Data hold time	t _{dh}	CL, DI	250			ns
CE wait time	t _{cp}	CE, CL	250			ns
CE setup time	t _{cs}	CE, CL	250			ns
CE hold time	t _{ch}	CE, CL	250			ns

Electrical Characteristics for the Allowable Operating Ranges

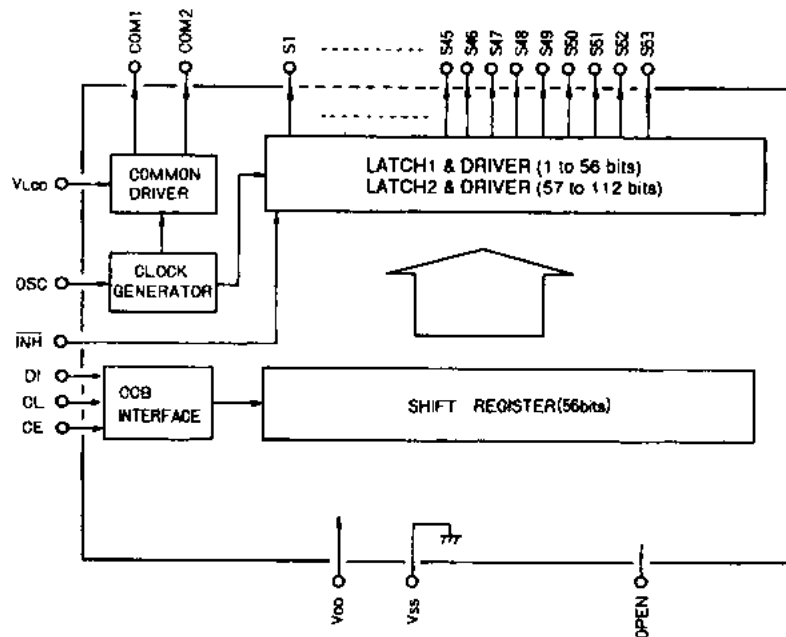
Parameter	Symbol	Conditions	min	typ	max	Unit
Input high-level current	I _{IH}	CE, CL, DI, INH: V _I = 6.5 V			5	μA
Input low-level current	I _{IL}	CE, CL, DI, INH: V _I = 0 V	-5			μA
Output high-level voltage	V _{OH1}	S1 to S53: I _O = -10 μA	V _{DD} - 1.0			V
Output low-level voltage	V _{OL1}	S1 to S53: I _O = 10 μA			1.0	V
Output high-level voltage	V _{OH2}	COM1, COM2: I _O = -100 μA	V _{LCD} - 0.6			V
Output low-level voltage	V _{OL2}	COM1, COM2: I _O = 100 μA			0.6	V
Mid-level voltage	V _{MID1}	COM1, COM2: V _{LCD} = 6.5 V, I _O = ±100 μA	2.65	3.25	3.85	V
	V _{MID2}	COM1, COM2: V _{LCD} = 3.0 V, I _O = ±100 μA	0.9	1.5	2.1	V
Oscillator frequency	f _{OSC}	OSC: R = 51 kΩ, C = 680 pF	40	50	60	kHz
Hysteresis voltage	V _H	CE, CL, DI: V _{OD} = 5 V	0.3			V
Current drain	I _{DD}				0.6	mA
	I _{LCD}	V _{LCD}			2	mA

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Pin Assignment



Block Diagram



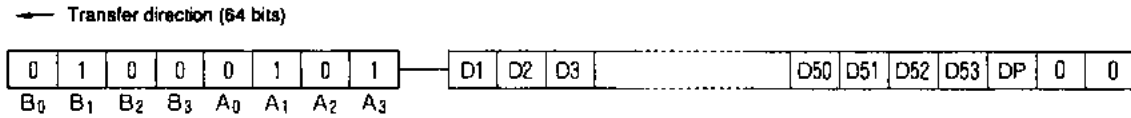
Pin Functions

Pin	Function
S1 to S53	Segment output pins
COM1, COM2	Common output pins (Only COM1 is used in static (1/1) drive. COM2 must be left open in that mode.)
VLCD	LCD bias voltage setting
OSC	Oscillator connection
CE, CL, DI	Serial data transfer inputs
VSS, VDD	Power supply
INH	Display off control input INH = low (VSS) Display off (S1 to S53, COM1, COM2 = low) INH = high (VDD) Display on Note that serial data transfers are still allowed when display output is turned off using this pin.
OPEN	Make no connections to this pin.

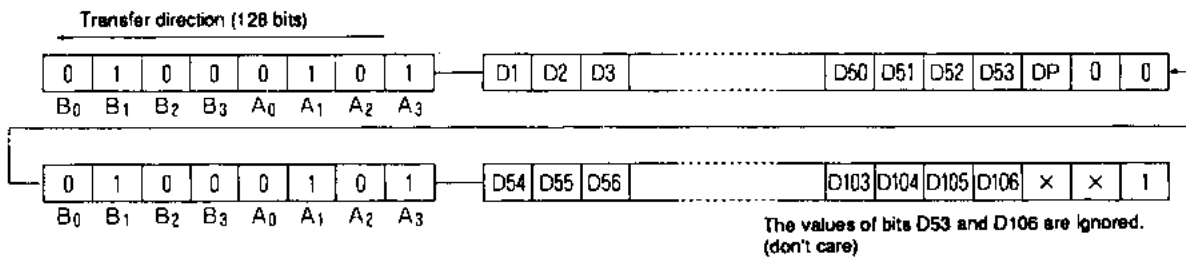
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Data Transfer Format

1. Static (1/1) duty



2. 1/2 duty (Only 64 bits need to be transferred if there are no more than 52 display segments. The transfer format is identical to the static duty case. It is not possible to change the D54 to D106 data without specifying the D1 to D53 data.)



CCB address: A2_H

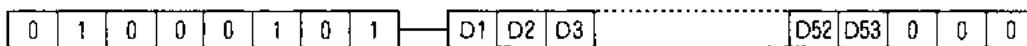
DP: Drive type selection bit
 DP = 0: 1/1 duty
 DP = 1: 1/2 duty

D1 to D106: Display data
 D_n (for n = 1 to 106) = 0: Segment off
 D_n (for n = 1 to 106) = 1: Segment on

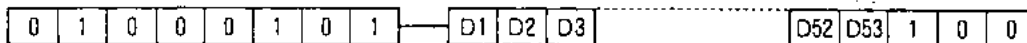
x: don't care

Data Transfer Examples

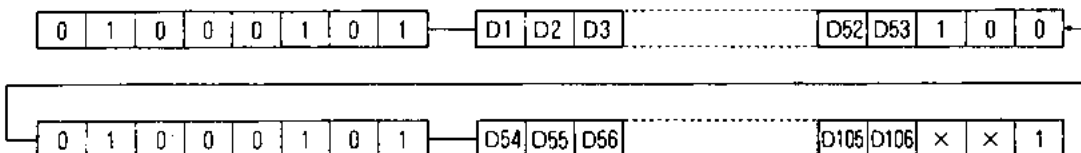
1. Static duty



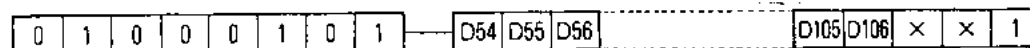
2. 1/2 duty with 52 or fewer segments



3. 1/2 duty with more than 52 segments

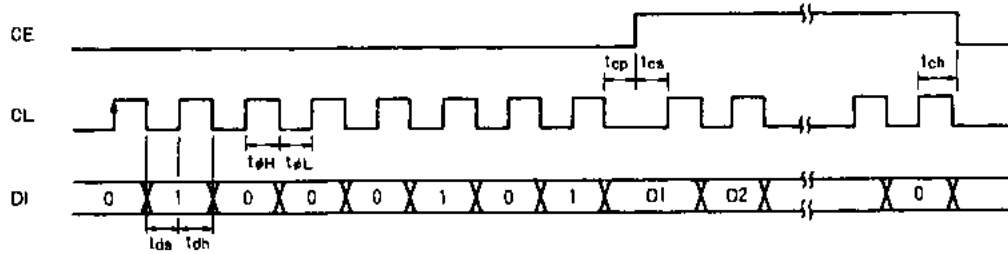


Note: The following transfer format is not allowed in 1/2 duty with 52 or fewer segments.

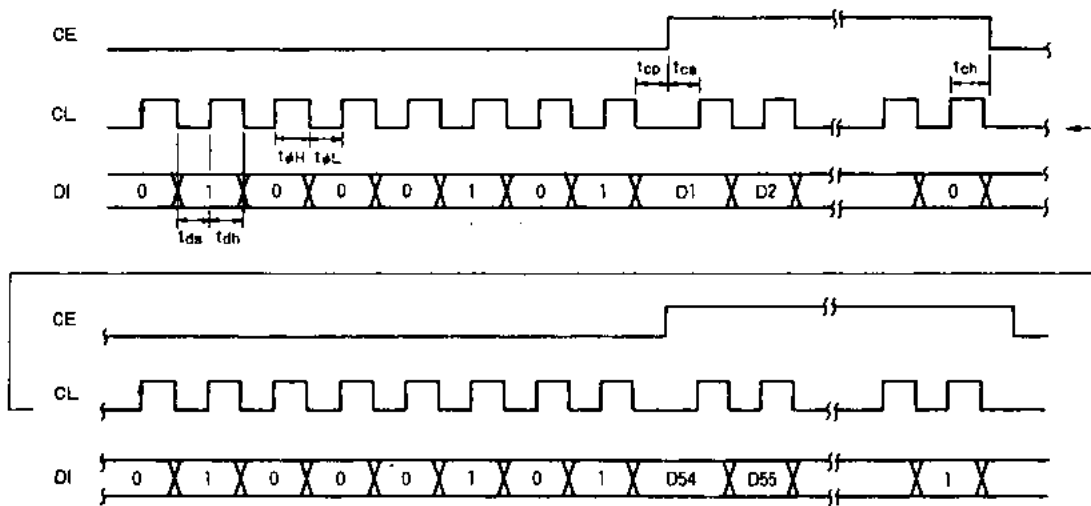


Serial Data

1. Static duty (64 bits)

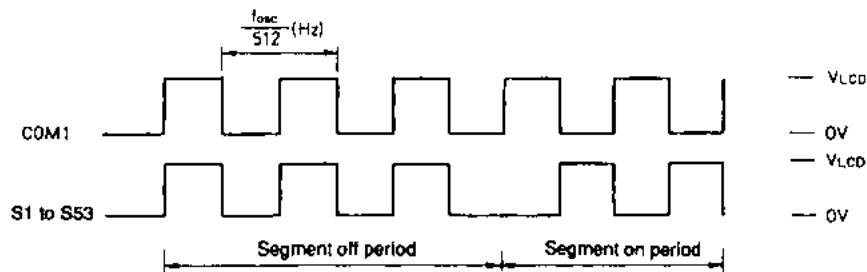


2. 1/2 duty (128 bits)



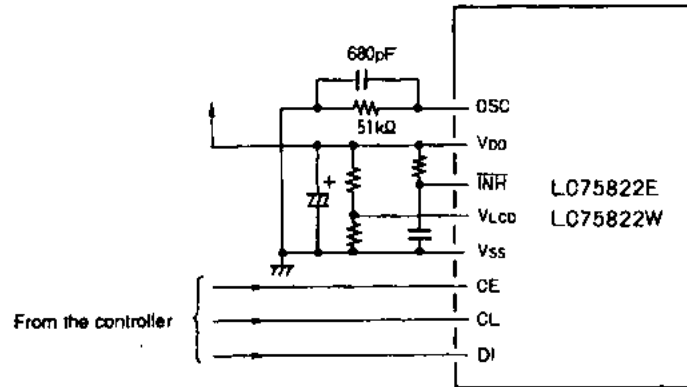
Output Waveforms

1. Static duty

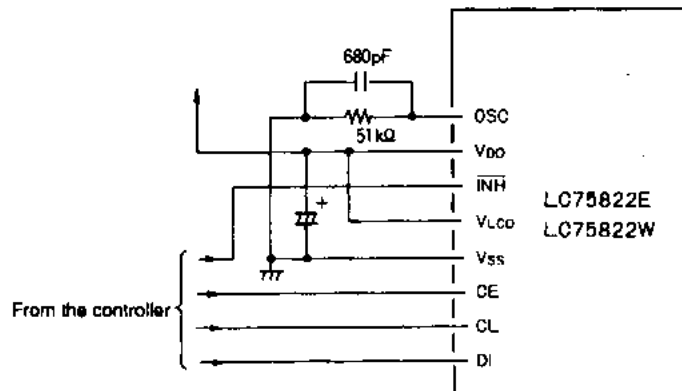


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Sample Application Circuit 1



Sample Application Circuit 2



Note: The internal display data is undefined when power (V_{DD}) is first applied. Since a meaningless pattern will be displayed if the display is turned on in that state, the display should be turned off by setting INH low and turned on only after display data has been sent from the controller.

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Transfer (external Input) Data/Output Pin Correspondence

Output pin	DP	0	1	COM1	COM2
		1/1 duty	1/2 duty		
S1		D1	D1	○	
			D2		○
S2		D2	D3	○	
			D4		○
S3		D3	D5	○	
			D6		○
⋮	⋮	⋮	⋮	⋮	⋮
S26		D26	D51	○	
			D52		○
S27		D27	D54	○	
			D55		○
S28		D28	D56	○	
			D57		○
⋮	⋮	⋮	⋮	⋮	⋮
S43		D43	D86	○	
			D87		○
S44		D44	D88	○	
			D89		○
S45		D45	D90	○	
			D91		○
S46		D46	D92	○	
			D93		○
S47		D47	D94	○	
			D95		○
S48		D48	D96	○	
			D97		○
S49		D49	D98	○	
			D99		○
S50		D50	D100	○	
			D101		○
S51		D51	D102	○	
			D103		○
S52		D52	D104	○	
			D105		○
S53		D53	Always on	○	
			Always on		○

Note: Only COM1 is used in static (1/1 duty) drive.

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Oscillator Frequency

Refer to the figure below when determining the oscillator frequency.

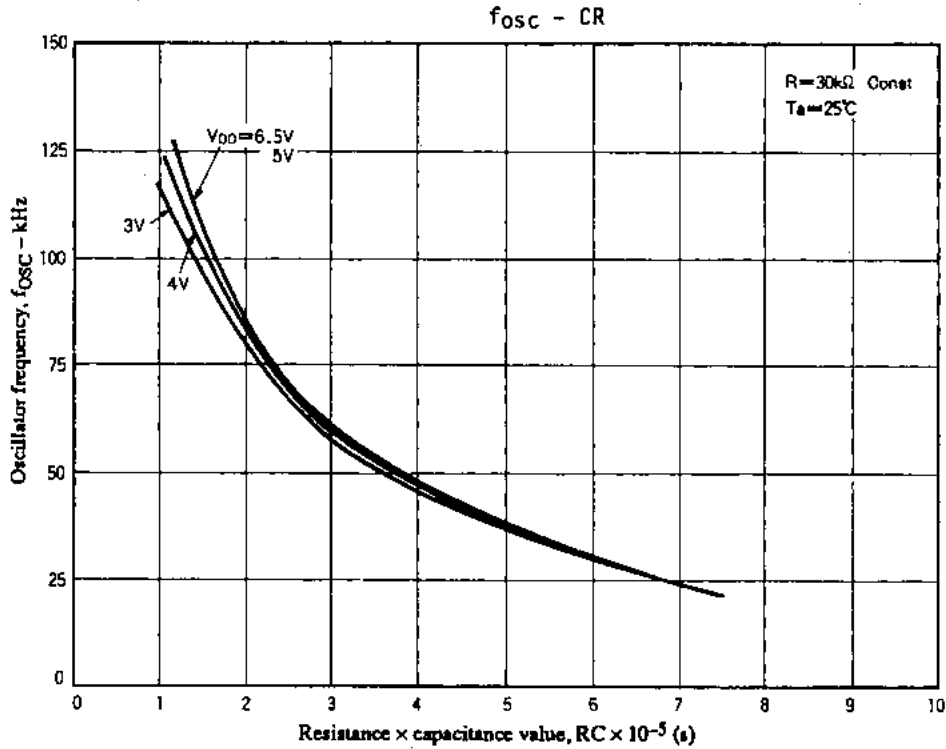


Figure 1 LC75822E, 75822W Oscillator Frequency vs. OSC Pin RC Constant

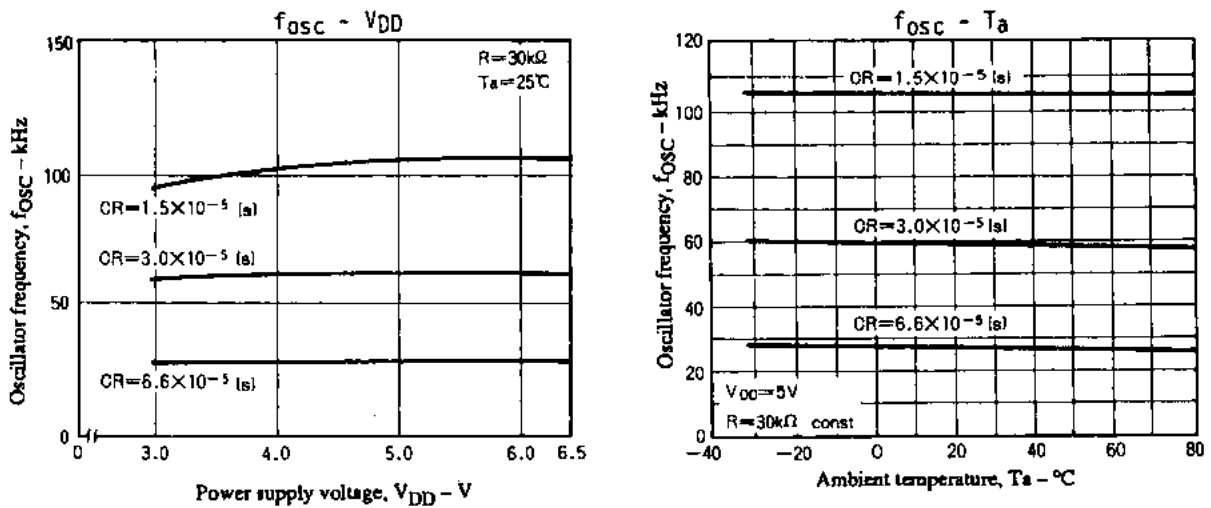


Figure 2 LC75822E, 75822W Oscillator Frequency vs. V_{DD}

Recommended range for external resistance: 10 to 100 kΩ (Carbon resistance)

Recommended range for external capacitance: 330 to 3300 pF

330 to 820 pF: (Ceramic capacitance with a zero temperature coefficient)

1000 to 3300 pF: (Mylar capacitance with a positive temperature coefficient)

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