

Ordering number : ENN4966C

CMOS IC



# LC75842E, LC75842M

## General-Purpose 1/2 Duty LCD Display Driver



### Overview

The LC75842E and LC75842M are 1/2 duty general-purpose LCD display drivers for applications such as microprocessor-controlled electronic tuning. They can drive up to 54 segments directly.

### Features

- 1/2 duty, 1/2 bias drive of up to 54 segments
- Serial data input supports CCB\* format communication with the system controller.
- Backup function which is based on a power saving mode and all segments off functions that are controlled by serial data.
- High generality, since display data is displayed directly without decoder intervention.
- The display can be forced to the off state with the  $\overline{\text{INH}}$  pin.
- RC oscillator circuit

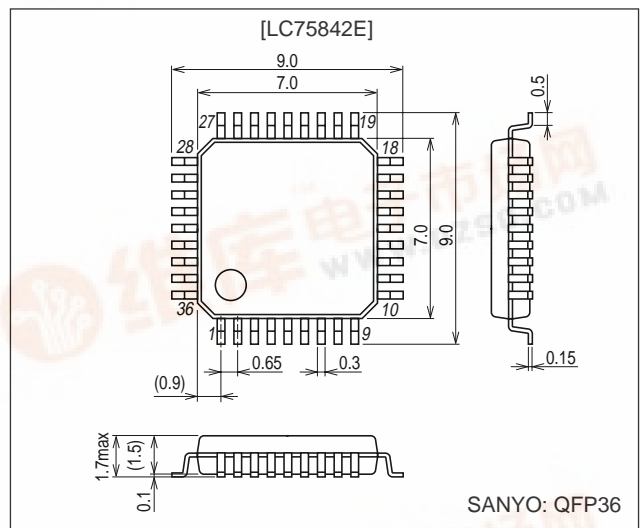
\*

- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

### Package Dimensions

unit: mm

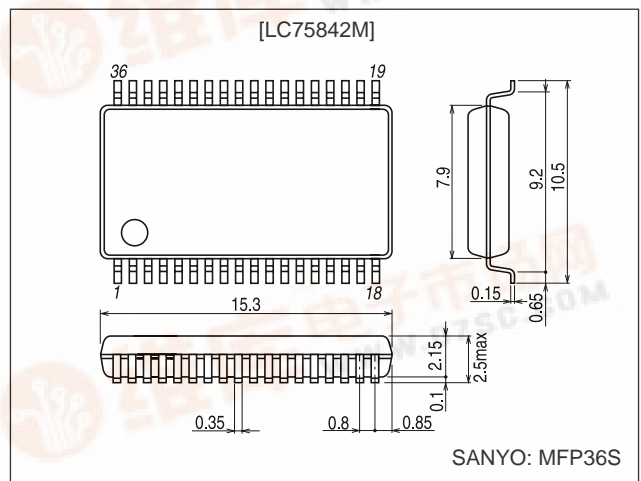
#### 3162C-QFP36



SANYO: QFP36

unit: mm

#### 3204-MFP36S



SANYO: MFP36S

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## LC75842E, LC75842M

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

| Parameter                   | Symbol              | Conditions                          | Ratings                | Unit             |
|-----------------------------|---------------------|-------------------------------------|------------------------|------------------|
| Maximum supply voltage      | $V_{DD\text{ max}}$ | $V_{DD}$                            | -0.3 to +6.5           | V                |
| Input voltage               | $V_{IN1}$           | CE, CL, DI, $\overline{\text{INH}}$ | -0.3 to +6.5           | V                |
|                             | $V_{IN2}$           | OSC                                 | -0.3 to $V_{DD} + 0.3$ | V                |
| Output voltage              | $V_{OUT}$           | OSC, S1 to S27, COM1, COM2          | -0.3 to $V_{DD} + 0.3$ | V                |
| Output current              | $I_{OUT1}$          | S1 to S27                           | 100                    | $\mu\text{A}$    |
|                             | $I_{OUT2}$          | COM1, COM2                          | 1                      | mA               |
| Allowable power dissipation | $P_d\text{ max}$    | $T_a = 85^\circ\text{C}$            | 100                    | mW               |
| Operating temperature       | $T_{opr}$           |                                     | -40 to +85             | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$           |                                     | -55 to +125            | $^\circ\text{C}$ |

#### Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$ , $V_{SS} = 0\text{ V}$

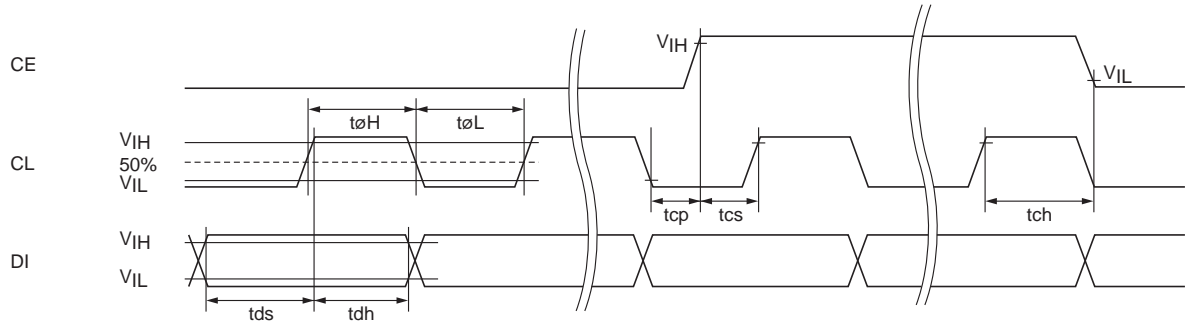
| Parameter                              | Symbol       | Conditions                             | Ratings      |     |              | Unit             |
|--|--------------|--|--------------|-----|--------------|------------------|
|  |              |  | min          | typ | max          |                  |
| Supply voltage                         | $V_{DD}$     | $V_{DD}$                               | 4.0          | 5.0 | 6.0          | V                |
| Input high level voltage               | $V_{IH}$     | CE, CL, DI, $\overline{\text{INH}}$    | $0.8 V_{DD}$ |     | 6.0          | V                |
| Input low level voltage                | $V_{IL}$     | CE, CL, DI, $\overline{\text{INH}}$    | 0            |     | $0.2 V_{DD}$ | V                |
| Recommended external resistance        | $R_{OSC}$    | OSC                                    |              | 68  |              | $\text{k}\Omega$ |
| Recommended external capacitance       | $C_{OSC}$    | OSC                                    |              | 680 |              | pF               |
| Guaranteed oscillator range            | $f_{OSC}$    | OSC                                    | 25           | 50  | 100          | kHz              |
| Low level clock pulse width            | $t_{\phi L}$ | CL: Figure 1                           | 160          |     |              | ns               |
| High level clock pulse width           | $t_{\phi H}$ | CL: Figure 1                           | 160          |     |              | ns               |
| Data setup time                        | $t_{ds}$     | CL, DI: Figure 1                       | 160          |     |              | ns               |
| Data hold time                         | $t_{dh}$     | CL, DI: Figure 1                       | 160          |     |              | ns               |
| CE wait time                           | $t_{cp}$     | CE, CL: Figure 1                       | 160          |     |              | ns               |
| CE setup time                          | $t_{cs}$     | CE, CL: Figure 1                       | 160          |     |              | ns               |
| CE hold time                           | $t_{ch}$     | CE, CL: Figure 1                       | 160          |     |              | ns               |
| $\overline{\text{INH}}$ switching time | $t_c$        | $\overline{\text{INH}}$ , CE: Figure 3 | 10           |     |              | $\mu\text{s}$    |

#### Electrical Characteristics in the Allowable Operating Ranges

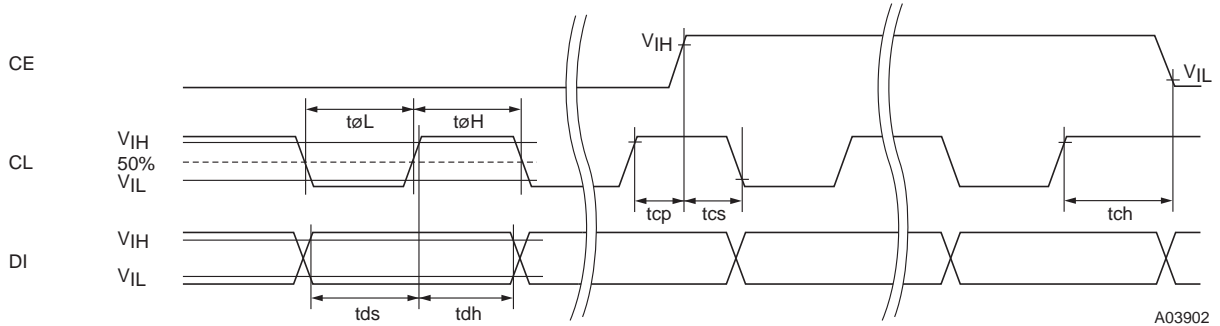
| Parameter                   | Symbol     | Conditions   | Ratings        |     |     | Unit          |
|-----------------------------|------------|--|----------------|-----|-----|---------------|
|                             |            |  | min            | typ | max |               |
| Hysteresis voltage          | $V_H$      | CE, CL, DI, $\overline{\text{INH}}$ : $V_{DD} = 5.0\text{ V}$      |                | 0.4 |     | V             |
| Input high level current    | $I_{IH}$   | CE, CL, DI, $\overline{\text{INH}}$ : $V_I = 6.0\text{ V}$         |                |     | 5.0 | $\mu\text{A}$ |
| Input low level current     | $I_{IL}$   | CE, CL, DI, $\overline{\text{INH}}$ : $V_I = 0\text{ V}$           | -5.0           |     |     | $\mu\text{A}$ |
| Output high level voltage   | $V_{OH1}$  | S1 to S27: $I_O = -10\ \mu\text{A}$                                | $V_{DD} - 1.0$ |     |     | V             |
|                             | $V_{OH2}$  | COM1, COM2: $I_O = -100\ \mu\text{A}$                              | $V_{DD} - 0.6$ |     |     | V             |
| Output low level voltage    | $V_{OL1}$  | S1 to S27: $I_O = 10\ \mu\text{A}$                                 |                |     | 1.0 | V             |
|                             | $V_{OL2}$  | COM1, COM2: $I_O = 100\ \mu\text{A}$                               |                |     | 0.6 | V             |
| Output middle level voltage | $V_{MID1}$ | COM1, COM2: $V_{DD} = 6.0\text{ V}$ , $I_O = \pm 100\ \mu\text{A}$ | 2.4            | 3.0 | 3.6 | V             |
|                             | $V_{MID2}$ | COM1, COM2: $V_{DD} = 4.0\text{ V}$ , $I_O = \pm 100\ \mu\text{A}$ | 1.4            | 2.0 | 2.6 | V             |
| Oscillator frequency        | $f_{OSC}$  | OSC: $R_{OSC} = 68\ \text{k}\Omega$ , $C_{OSC} = 680\ \text{pF}$   | 40             | 50  | 60  | kHz           |
| Current drain               | $I_{DD1}$  | Power saving mode  |                |     | 5   | $\mu\text{A}$ |
|                             | $I_{DD2}$  | $V_{DD} = 6.0\text{ V}$ , output open, $f_{OSC} = 50\ \text{kHz}$  |                | 1.2 | 2.0 | mA            |

## LC75842E, LC75842M

1. When CL is stopped at the low level



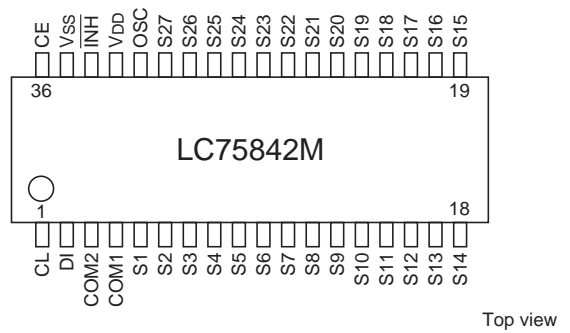
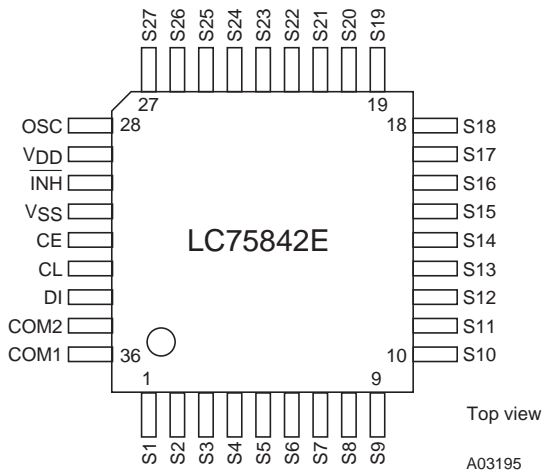
2. When CL is stopped at the high level



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**Figure 1**

### Pin Assignments

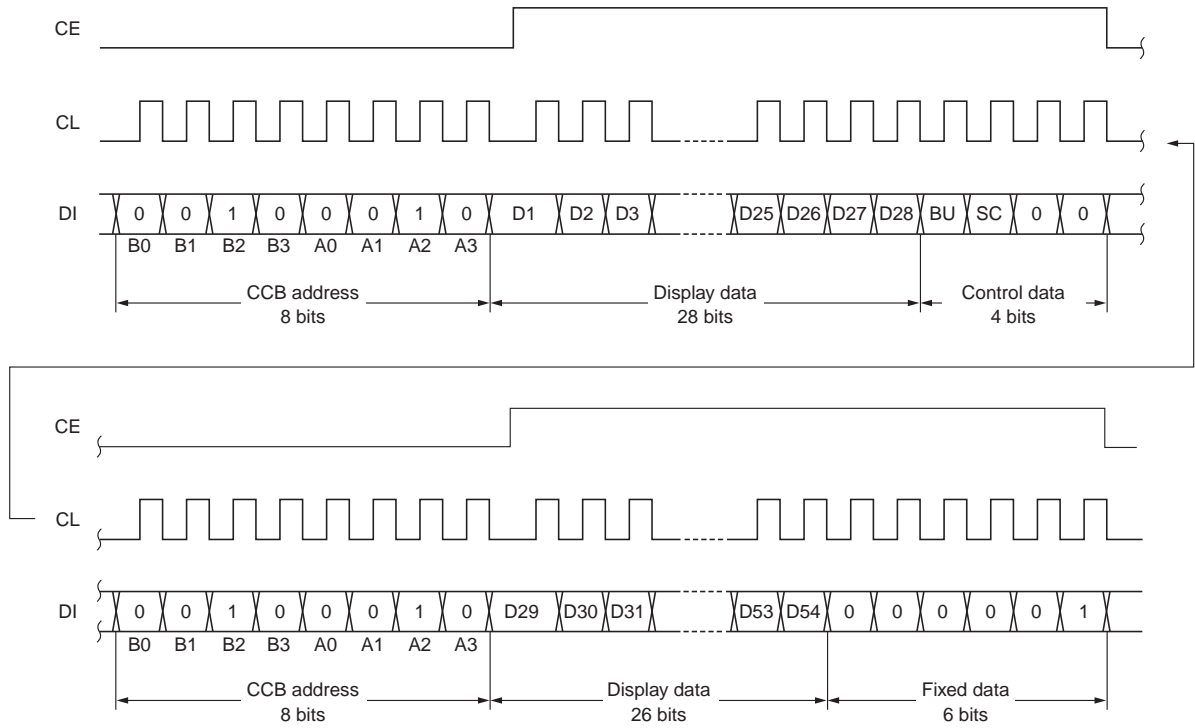




## LC75842E, LC75842M

### Serial Data Transfer Format

1. When CL is stopped at the low level



2. When CL is stopped at the high level

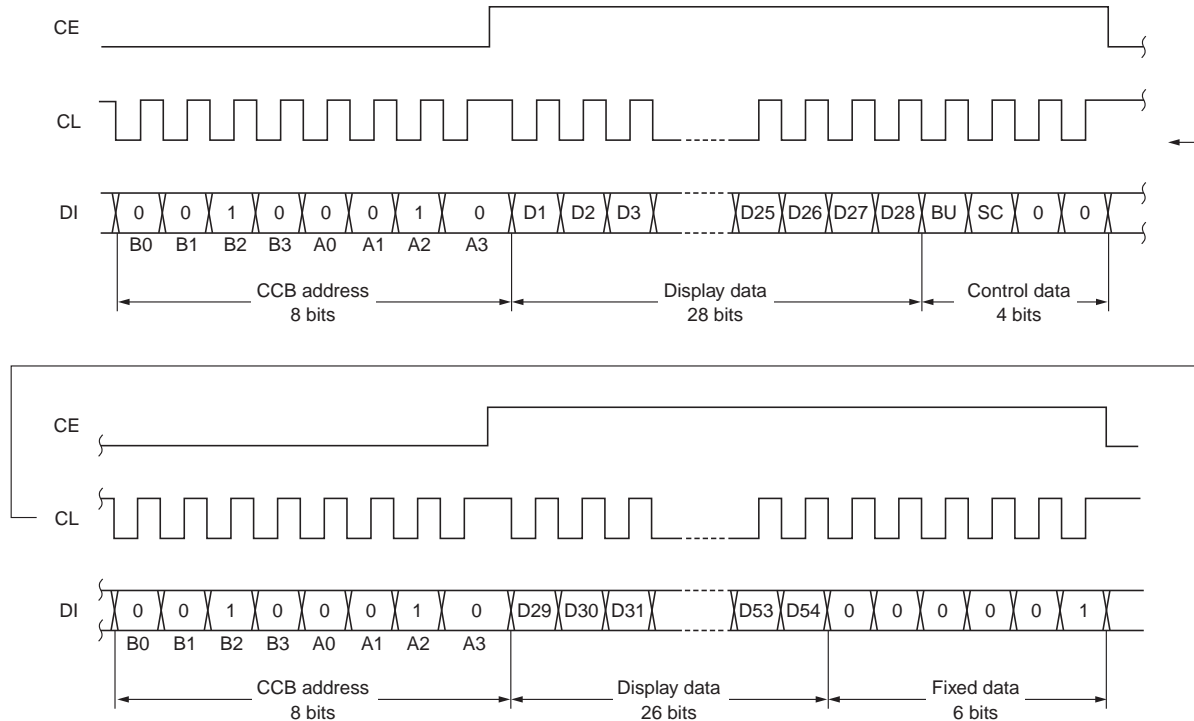
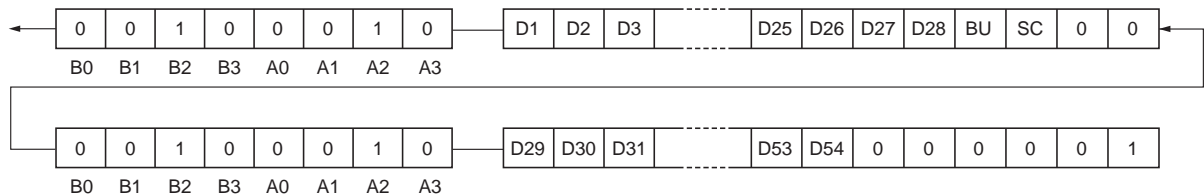


Figure 2

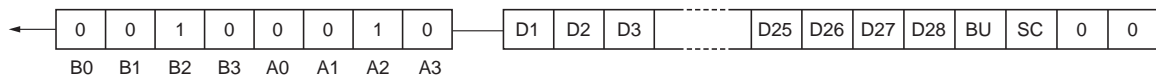
- CCB address.....44<sub>H</sub>
- D1 to D54.....Display data  
 D<sub>n</sub> (n = 1 to 54) = 1: Segment on  
 D<sub>n</sub> (n = 1 to 54) = 0: Segment off
- BU .....Control data for specifying normal mode or power saving mode
- SC.....Control data for specifying all segments on or off

Serial Data Transfer Example

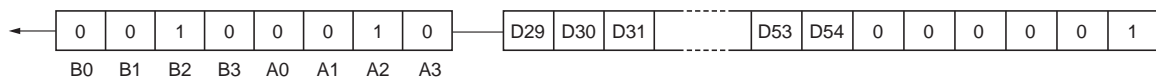
When 29 or more segments are used all 80 bits of the serial data must be sent.



When fewer than 29 segments are used only the first 40 bits of the serial data can be sent. However, all 80 bits must be sent after power is first applied.



Note: The following type of transfer cannot be used when fewer than 29 segments are used.



## LC75842E, LC75842M

### Control Data Functions

1. BU: Control data for specifying normal mode or power saving mode

This control data bit is used to control the normal mode/power saving mode state of the LC75842E and LC75842M.

| BU | Mode   |
|----|--|
| 0  | Normal mode  |
| 1  | Power saving mode (The OSC pin oscillator is stopped and the common and segment output pins go to the $V_{SS}$ level.) |

2. SC: Control data for specifying all segments on or off

This control data bit is used to turn all segments on or off.

| SC | Display state |
|----|---------------|
| 0  | On            |
| 1  | Off           |

Note that when SC is 1 the display is turned off by outputting the segment off waveforms from the segment pins.

### Correspondence between Display Data and Segment Output Pins

| Segment output pin | COM1 | COM2 |
|--------------------|------|------|
| S1                 | D1   | D2   |
| S2                 | D3   | D4   |
| S3                 | D5   | D6   |
| S4                 | D7   | D8   |
| S5                 | D9   | D10  |
| S6                 | D11  | D12  |
| S7                 | D13  | D14  |
| S8                 | D15  | D16  |
| S9                 | D17  | D18  |
| S10                | D19  | D20  |
| S11                | D21  | D22  |
| S12                | D23  | D24  |
| S13                | D25  | D26  |
| S14                | D27  | D28  |

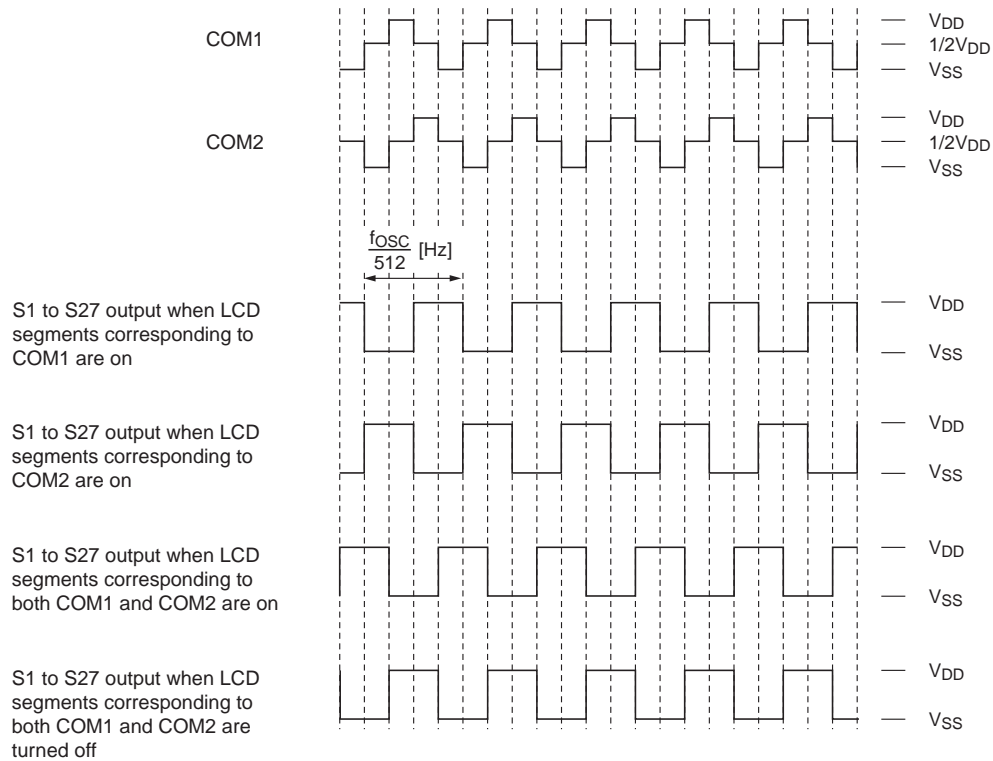
| Segment output pin | COM1 | COM2 |
|--------------------|------|------|
| S15                | D29  | D30  |
| S16                | D31  | D32  |
| S17                | D33  | D34  |
| S18                | D35  | D36  |
| S19                | D37  | D38  |
| S20                | D39  | D40  |
| S21                | D41  | D42  |
| S22                | D43  | D44  |
| S23                | D45  | D46  |
| S24                | D47  | D48  |
| S25                | D49  | D50  |
| S26                | D51  | D52  |
| S27                | D53  | D54  |

For example, the table below lists the output states for the S11 segment output pin.

| Display data |     | Segment output pin (S11) state           |
|--------------|-----|--|
| D21          | D22 |  |
| 0            | 0   | Both segments for COM1 and COM2 are off. |
| 0            | 1   | Segment for COM2 is on.                  |
| 1            | 0   | Segment for COM1 is on.                  |
| 1            | 1   | Both segments for COM1 and COM2 are on.  |

## LC75842E, LC75842M

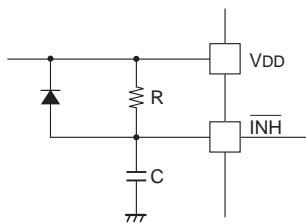
### Output Waveforms (1/2 duty, 1/2 bias drive)



A03198

### INH and Display Control

Since the IC internal data (D1 to D54 and control data) is undefined when power is first applied, the display is turned off (S1 to S27, COM1 and COM2 = low) by setting  $\overline{\text{INH}}$  pin low at the same time as power is applied. Then, meaningless display at the power on can be prevented by transferring all 80 bits of serial data from the controller while the display is turned off and  $\overline{\text{INH}}$  pin high after the transfer completes. (See Figure 3.)



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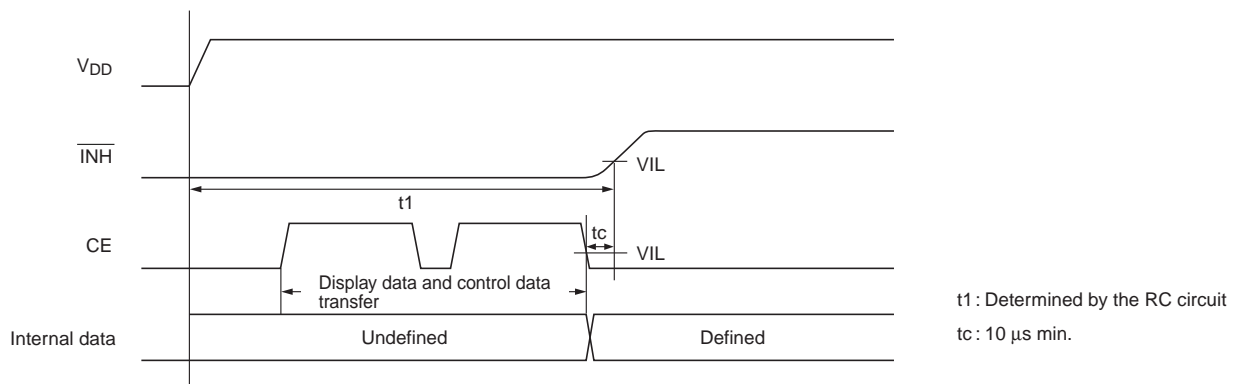


Figure 3

A03200



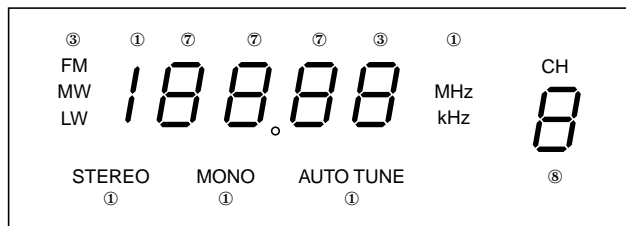
## LC75842E, LC75842M

### Notes on Transferring Display Data from the Controller

Since the LC75842E and LC75842M take the display data (D1 to D54) in two separate transfer operations as shown in Figure 2, we recommend that all the display data be transferred within 30 [ms] to maintain the quality of the displayed image.

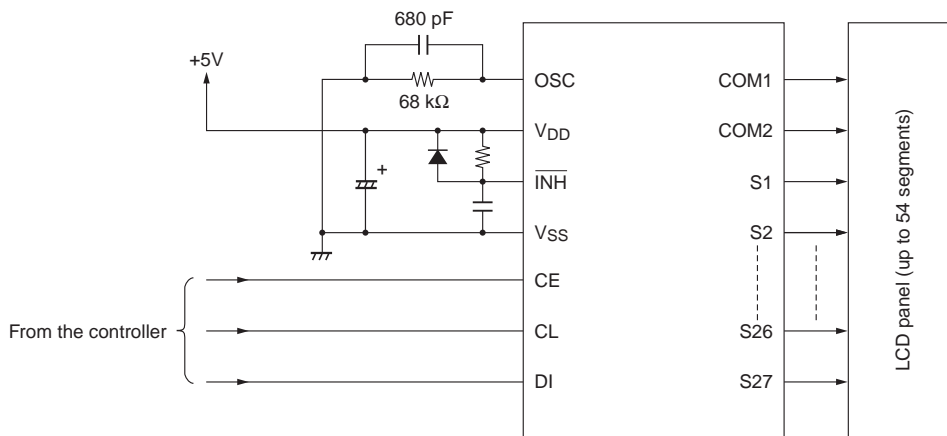
### Sample Display

Example in which 40 segments are used (up to 54 segments can be used)



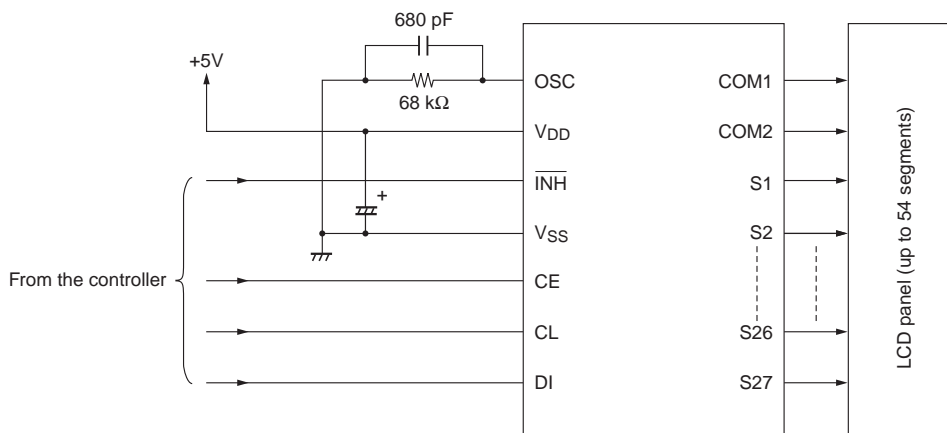
Note: The numbers in circles indicate the number of segments.

### Sample Application Circuit 1



A03201

### Sample Application Circuit 2



A03202

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