



LC75850E, 75850W

1/3 Duty General Purpose LCD Drivers

Overview

The LC75850E and LC75850W are general purpose LCD drivers for use in microprocessor controlled applications such as radio tuner frequency displays.

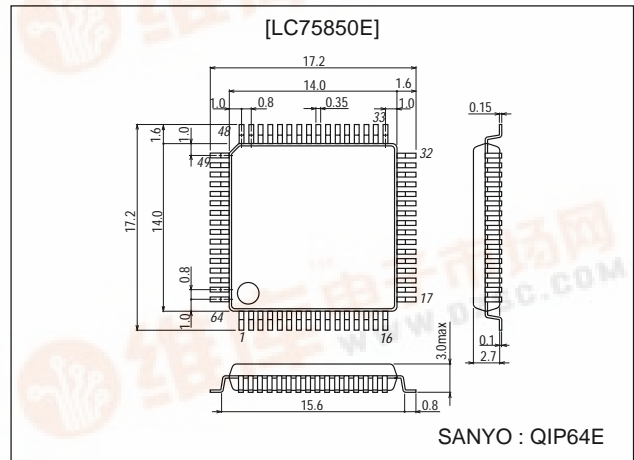
Functions

- Supports both 1/3 duty 1/2 bias and 1/3 duty 1/3 bias LCD driver techniques for a maximum of 156 segments.
- Power saving mode allows the backup function to be switched on or off and all segments to be turned off unconditionally.
- Can be controlled by three serial data lines (CE, CL, and DI) from the microprocessor. (CCB handling)
- High generality, since segment data can be displayed without going through a decoder.
- The INH pin unconditionally turns off display.
- The LCD drive bias voltage can be provided internally or externally.
- Power supply voltage: 4.5 to 8V.

Package Dimensions

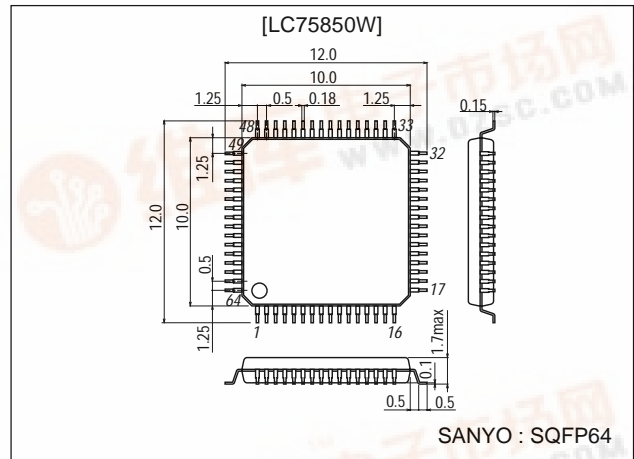
unit:mm

3159-QIP64E



unit:mm

3190-SQFP64



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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{V}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|-------------------------------------|------------------------|------------------|
| Maximum supply voltage | $V_{DD\text{ max}}$ | V_{DD} | -0.3 to +9.0 | V |
| Input voltage | V_{IN1} | CE, CL, DI, $\overline{\text{INH}}$ | -0.3 to +9.0 | V |
| | V_{IN2} | OSC | -0.3 to $V_{DD} + 0.3$ | V |
| Output voltage | V_{OUT} | OSC | -0.3 to $V_{DD} + 0.3$ | V |
| Output current | I_{OUT1} | S1 to S52 | 300 | μA |
| | I_{OUT2} | COM1 to COM3 | 3 | mA |
| Allowable power dissipation | $P_d\text{ max}$ | $T_a \leq 85^\circ\text{C}$ | 200 | mW |
| Operating temperature | T_{opr} | | -40 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|--|--------------|-------------------------------------|---------|-------------|-----|------------------|
| | | | min | typ | max | |
| Supply voltage | V_{DD} | V_{DD} | 4.5 | | 8.0 | V |
| Input voltage | V_{DD1} | V_{DD1} | | $2/3V_{DD}$ | 8.0 | V |
| | V_{DD2} | V_{DD2} | | $1/3V_{DD}$ | 8.0 | V |
| Input high level voltage | V_{IH} | CE, CL, DI, $\overline{\text{INH}}$ | 4.0 | | 8.0 | V |
| Input low level voltage | V_{IL} | CE, CL, DI, $\overline{\text{INH}}$ | 0 | | 0.7 | V |
| Recommended external resistance | R_{OSC} | OSC | | 47 | | $\text{k}\Omega$ |
| Recommended external capacitance | C_{OSC} | OSC | | 1000 | | pF |
| Guaranteed oscillator range | f_{OSC} | OSC | 19 | 38 | 76 | kHz |
| Data setup time | t_{ds} | CL, DI: Figure 2 | 100 | | | ns |
| Data hold time | t_{dh} | CL, DI: Figure 2 | 100 | | | ns |
| CE wait time | t_{cp} | CE, CL: Figure 2 | 100 | | | ns |
| CE setup time | t_{cs} | CE, CL: Figure 2 | 100 | | | ns |
| CE hold time | t_{ch} | CE, CL: Figure 2 | 100 | | | ns |
| CL high level time | $t_{\phi H}$ | CL: Figure 2 | 100 | | | ns |
| CL low level time | $t_{\phi L}$ | CL: Figure 2 | 100 | | | ns |
| Rise time | t_r | CE, CL, DI: Figure 2 | | 100 | | ns |
| Fall time | t_f | CE, CL, DI: Figure 2 | | 100 | | ns |
| $\overline{\text{INH}}$ switching time | t_2 | Figure 3 | 10 | | | μs |

Electrical Characteristics at $T_a = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{V}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|-----------------------------|------------|---|--------------|--------------------|------|---------------|
| | | | min | typ | max | |
| Input high level current | I_{IH1} | CE, CL, DI $\overline{\text{INH}}$; $V_{IH}=8\text{V}$ | | | 5 | μA |
| Input low level current | I_{IL2} | CE, CL, DI $\overline{\text{INH}}$; $V_{IL}=0\text{V}$ | | | 5 | μA |
| Oscillator frequency | f_{OSC} | OSC; $R_{OSC}=47\text{k}\Omega$, $C_{OSC}=1000\text{pF}$ | | 38 | | kHz |
| Hysteresis | V_H | CE, CL, DI $\overline{\text{INH}}$; $V_{DD}=5\text{V}$ | 0.3 | | | V |
| Output high level voltage | V_{OH1} | S1 to S52; $I_{OUT1}=-20\mu\text{A}$ | $V_{DD}-1.0$ | | | V |
| Output low level voltage | V_{OL1} | S1 to S52; $I_{OUT1}=20\mu\text{A}$ | | | 1.0 | V |
| Output high level voltage | V_{OH2} | COM1 to COM3; $I_{OUT2}=-100\mu\text{A}$ | $V_{DD}-1.0$ | | | V |
| Output low level voltage | V_{OL2} | COM1 to COM3; $I_{OUT2}=100\mu\text{A}$ | | | 1.0 | V |
| Intermediate level voltage* | V_{MID1} | 1/2 bias, COM1 to COM3; $I_{OUT2}=\pm 100\mu\text{A}$ | | $1/2V_{DD}\pm 1.0$ | | V |
| | V_{MID2} | 1/3 bias, COM1 to COM3; $I_{OUT2}=\pm 100\mu\text{A}$ | | $2/3V_{DD}\pm 1.0$ | | V |
| | V_{MID3} | 1/3 bias, COM1 to COM3; $I_{OUT2}=\pm 100\mu\text{A}$ | | $1/3V_{DD}\pm 1.0$ | | V |
| | V_{MID4} | 1/3 bias, S1 to S52; $I_{OUT1}=\pm 20\mu\text{A}$ | | $2/3V_{DD}\pm 1.0$ | | V |
| | V_{MID5} | 1/3 bias, S1 to S52; $I_{OUT1}=\pm 20\mu\text{A}$ | | $1/3V_{DD}\pm 1.0$ | | V |
| Supply current | I_{DD1} | Power saving mode | | | 5 | μA |
| | I_{DD2} | $f=38\text{kHz}$, 1/2 bias, $V_{DD}=5\text{V}$ | | 400 | 800 | μA |
| | I_{DD3} | $f=38\text{kHz}$, 1/3 bias, $V_{DD}=5\text{V}$ | | 300 | 600 | μA |
| | I_{DD4} | $f=38\text{kHz}$, 1/2 bias, $V_{DD}=8\text{V}$ | | 650 | 1300 | μA |
| | I_{DD5} | $f=38\text{kHz}$, 1/3 bias, $V_{DD}=8\text{V}$ | | 580 | 1200 | μA |

Note: *Except the bias voltage generation divider resistors that are built into V_{DD1} and V_{DD2} . (See figure 1.)

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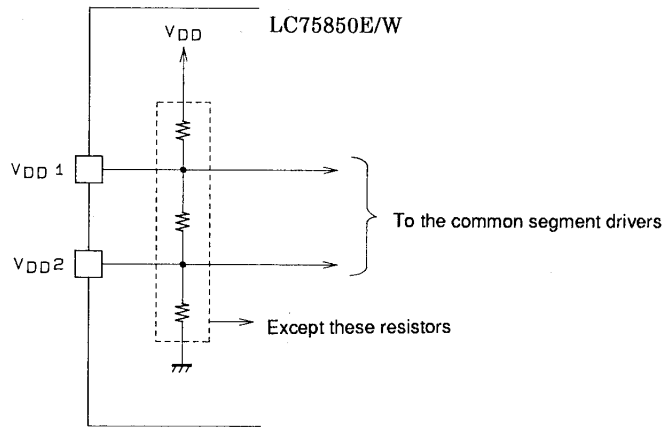
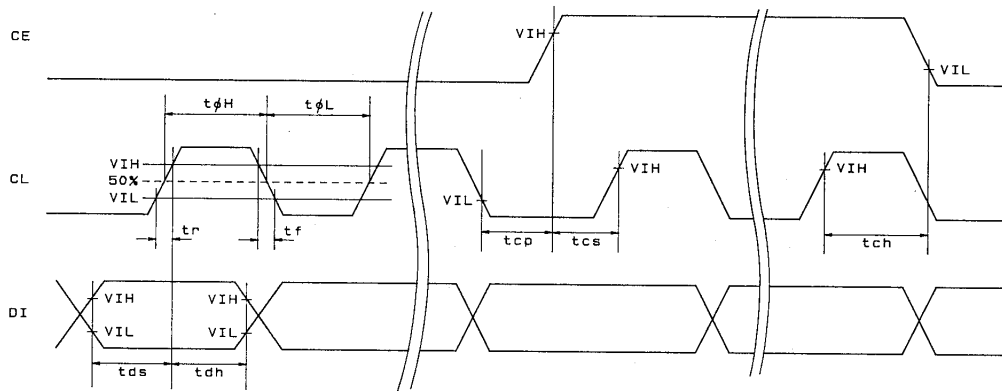


Figure 1

When CL is stopped at the low level



When CL is stopped at the high level

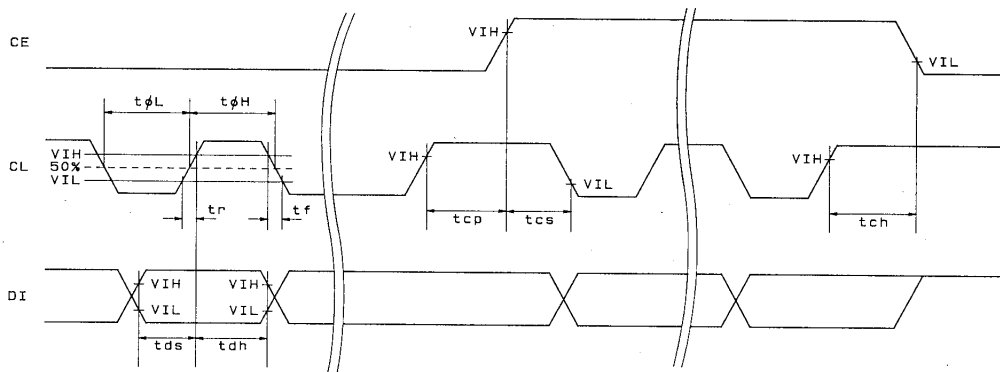
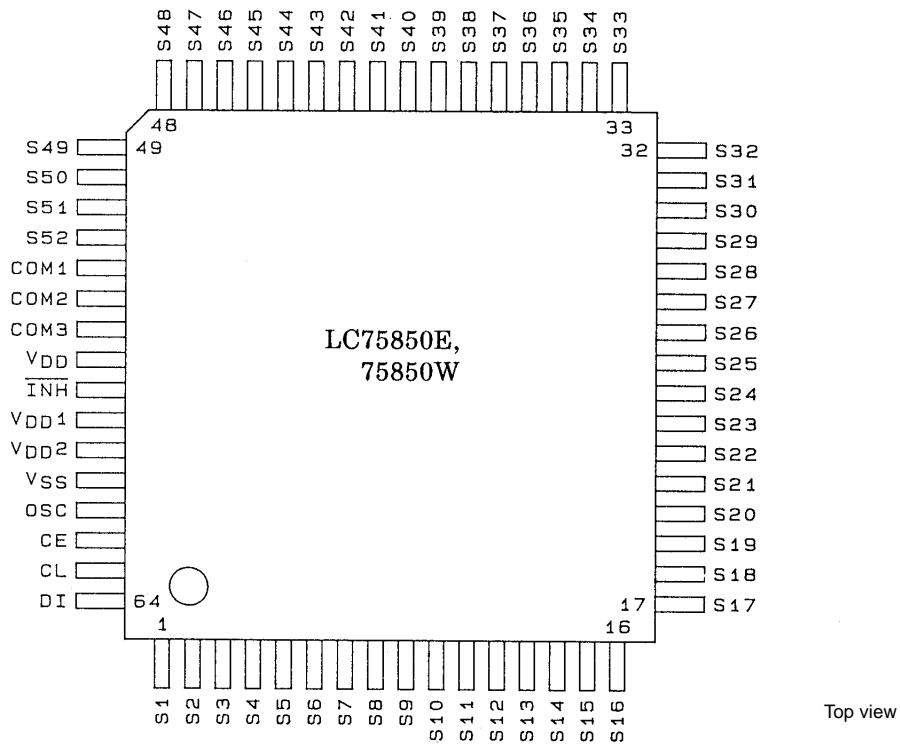


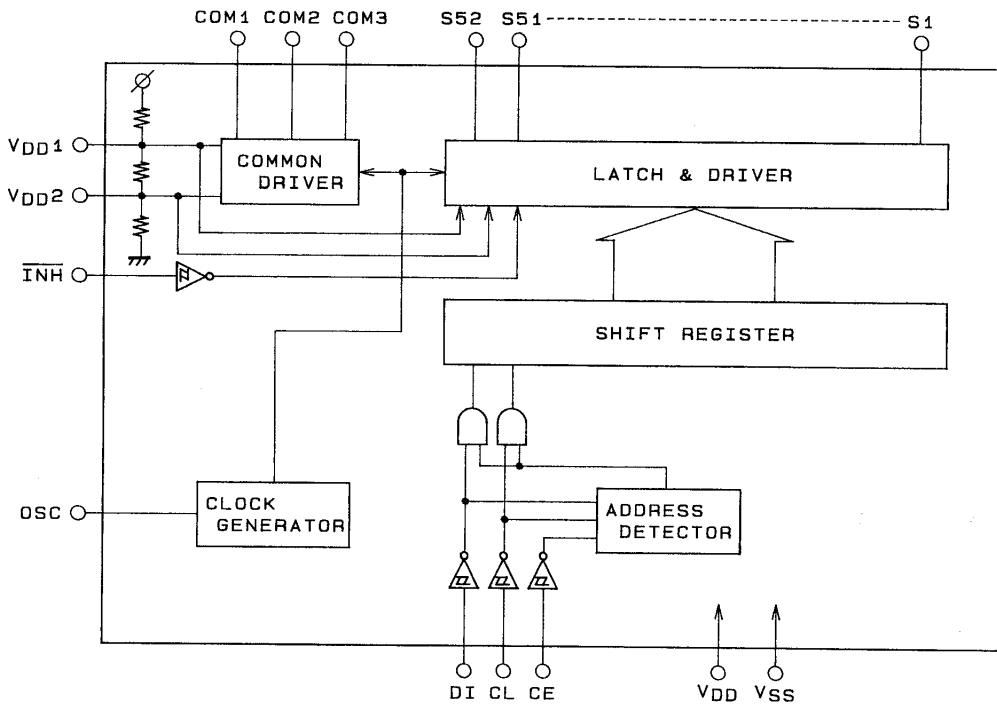
Figure 2

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Pin Assignment



Block Diagram



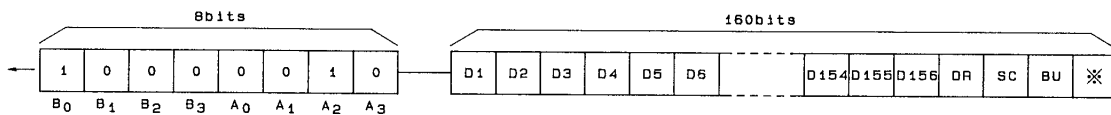
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Pin Functions

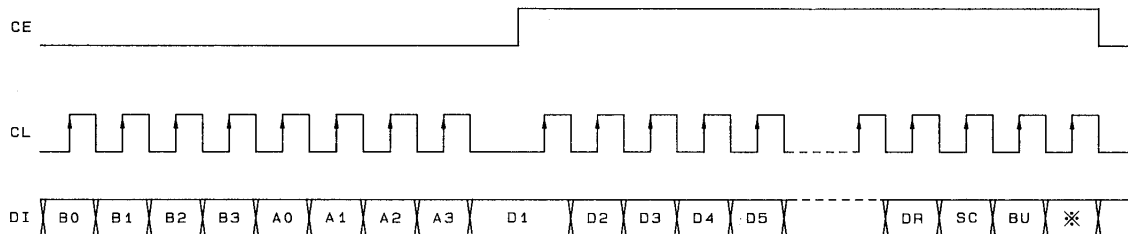
| Pin | Pin No. | Function | Active | I/O | Handling when unused |
|-------------------------|----------------|--|------------------------------------|-----|----------------------|
| S1 to S52 | 1 to 52 | Segment outputs that display the data transferred as serial data | – | O | Open |
| COM1 COM2 COM3 | 53 54 55 | Common driver outputs. The frame frequency is $f_O=(f_{OSC}/384)$ Hz. | – | O | Open |
| OSC | 61 | Oscillator connection (for generating the common segment alternation waveform) | – | I | GND |
| CE CL DI | 62 63 64 | Serial data transfer pins : connected to the microprocessor. | CE: chip enable H | I | GND |
| | | | CL: synchronization clock L → H | | |
| | | | DI: transfer data – | | |
| $\overline{\text{INH}}$ | 57 | Forcibly turns off the display without regard for the internal data. Serial data can always be input, whatever the state of this pin. | L | I | GND |
| V _{DD1} | 58 | Used for the 2/3 bias voltage when bias voltages are provided externally. Connect to V _{DD2} when 1/2 bias is used. | – | I | Open |
| V _{DD2} | 59 | Used for the 1/3 bias voltage when bias voltages are provided externally. Connect to V _{DD1} when 1/2 bias is used. | – | I | Open |

Serial Data Transfer Format

1. Serial data



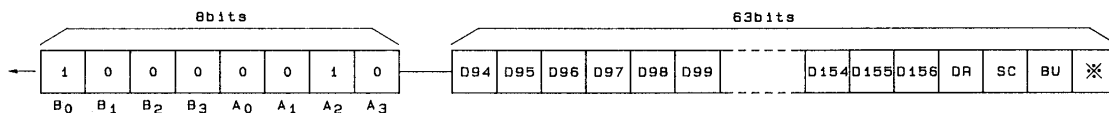
2. Data transfer format



3. When used with fewer than 156 segments

<Example> Using 63 segments

Segment allocation method.....Sixty three segments are allocated starting at D156.



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- CCB address 41
- D1 to D156 Display data
- DR Drive method selection bit
 - 1 = 1/3 duty, 1/3 bias
 - 0 = 1/3 duty, 1/2 bias
- SC Segment drive/clear control bit
 - 1 = Clear (Display clearing waveforms are output from common and segment pins.)
 - 0 = Drive (Normal drive)
- BU Normal mode/power saving mode control bit
 - 1 = Power saving mode (The oscillator is stopped and the common and segment pins go to the ground level.)
 - 0 = Normal mode
- * Dont't care

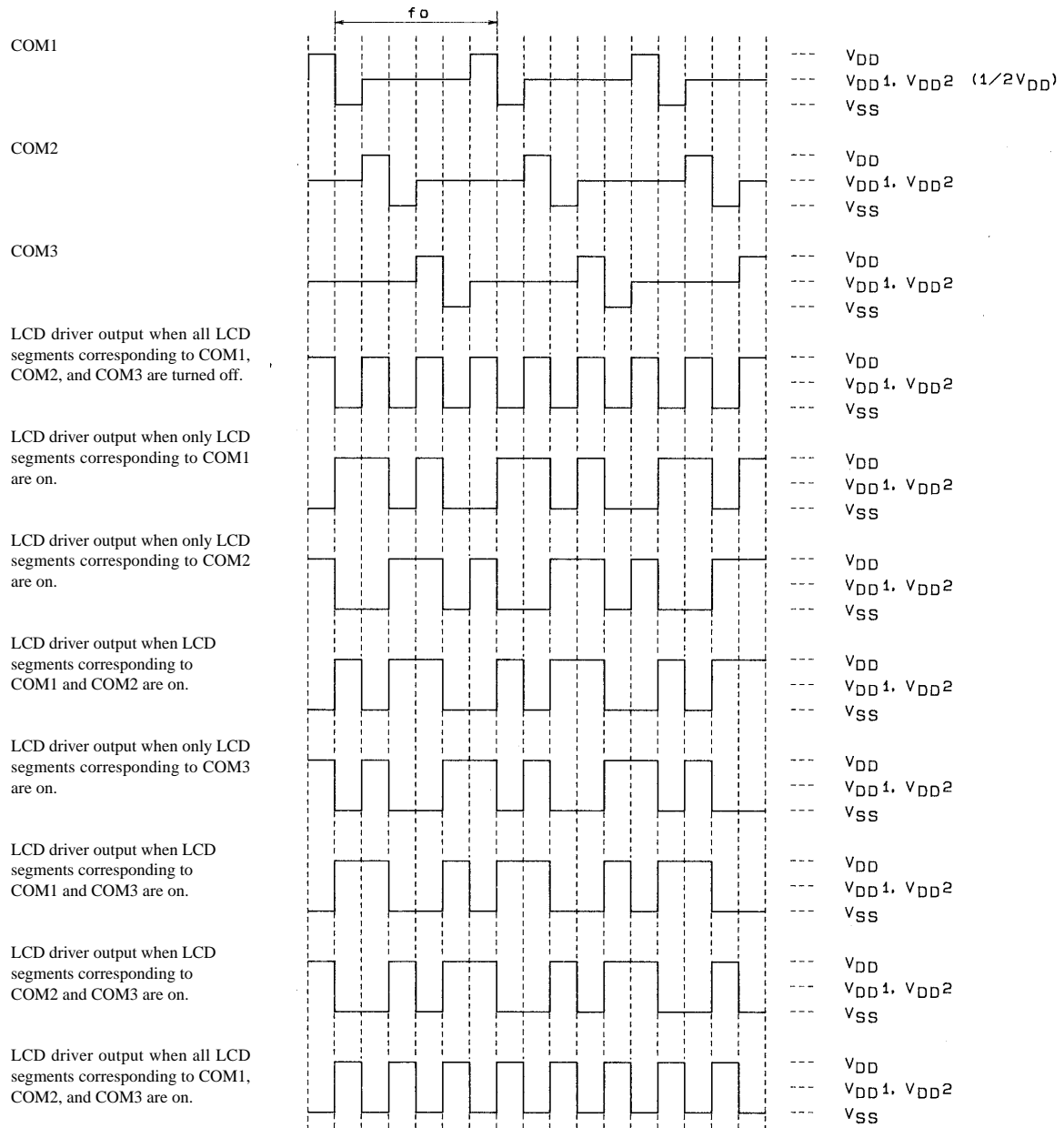
Transferred Data/Output Pin Correspondence

| | COM3 | COM2 | COM1 |
|-----|------|------|------|
| S1 | D1 | D2 | D3 |
| S2 | D4 | D5 | D6 |
| S3 | D7 | D8 | D9 |
| S4 | D10 | D11 | D12 |
| S5 | D13 | D14 | D15 |
| S6 | D16 | D17 | D18 |
| S7 | D19 | D20 | D21 |
| S8 | D22 | D23 | D24 |
| S9 | D25 | D26 | D27 |
| S10 | D28 | D29 | D30 |
| S11 | D31 | D32 | D33 |
| S12 | D34 | D35 | D36 |
| S13 | D37 | D38 | D39 |
| S14 | D40 | D41 | D42 |
| S15 | D43 | D44 | D45 |
| S16 | D46 | D47 | D48 |
| S17 | D49 | D50 | D51 |
| S18 | D52 | D53 | D54 |
| S19 | D55 | D56 | D57 |
| S20 | D58 | D59 | D60 |
| S21 | D61 | D62 | D63 |
| S22 | D64 | D65 | D66 |
| S23 | D67 | D68 | D69 |
| S24 | D70 | D71 | D72 |
| S25 | D73 | D74 | D75 |
| S26 | D76 | D77 | D78 |

| | COM3 | COM2 | COM1 |
|-----|------|------|------|
| S27 | D79 | D80 | D81 |
| S28 | D82 | D83 | D84 |
| S29 | D85 | D86 | D87 |
| S30 | D88 | D89 | D90 |
| S31 | D91 | D92 | D93 |
| S32 | D94 | D95 | D96 |
| S33 | D97 | D98 | D99 |
| S34 | D100 | D101 | D102 |
| S35 | D103 | D104 | D105 |
| S36 | D106 | D107 | D108 |
| S37 | D109 | D110 | D111 |
| S38 | D112 | D113 | D114 |
| S39 | D115 | D116 | D117 |
| S40 | D118 | D119 | D120 |
| S41 | D121 | D122 | D123 |
| S42 | D124 | D125 | D126 |
| S43 | D127 | D128 | D129 |
| S44 | D130 | D131 | D132 |
| S45 | D133 | D134 | D135 |
| S46 | D136 | D137 | D138 |
| S47 | D139 | D140 | D141 |
| S48 | D142 | D143 | D144 |
| S49 | D145 | D146 | D147 |
| S50 | D148 | D149 | D150 |
| S51 | D151 | D152 | D153 |
| S52 | D154 | D155 | D156 |

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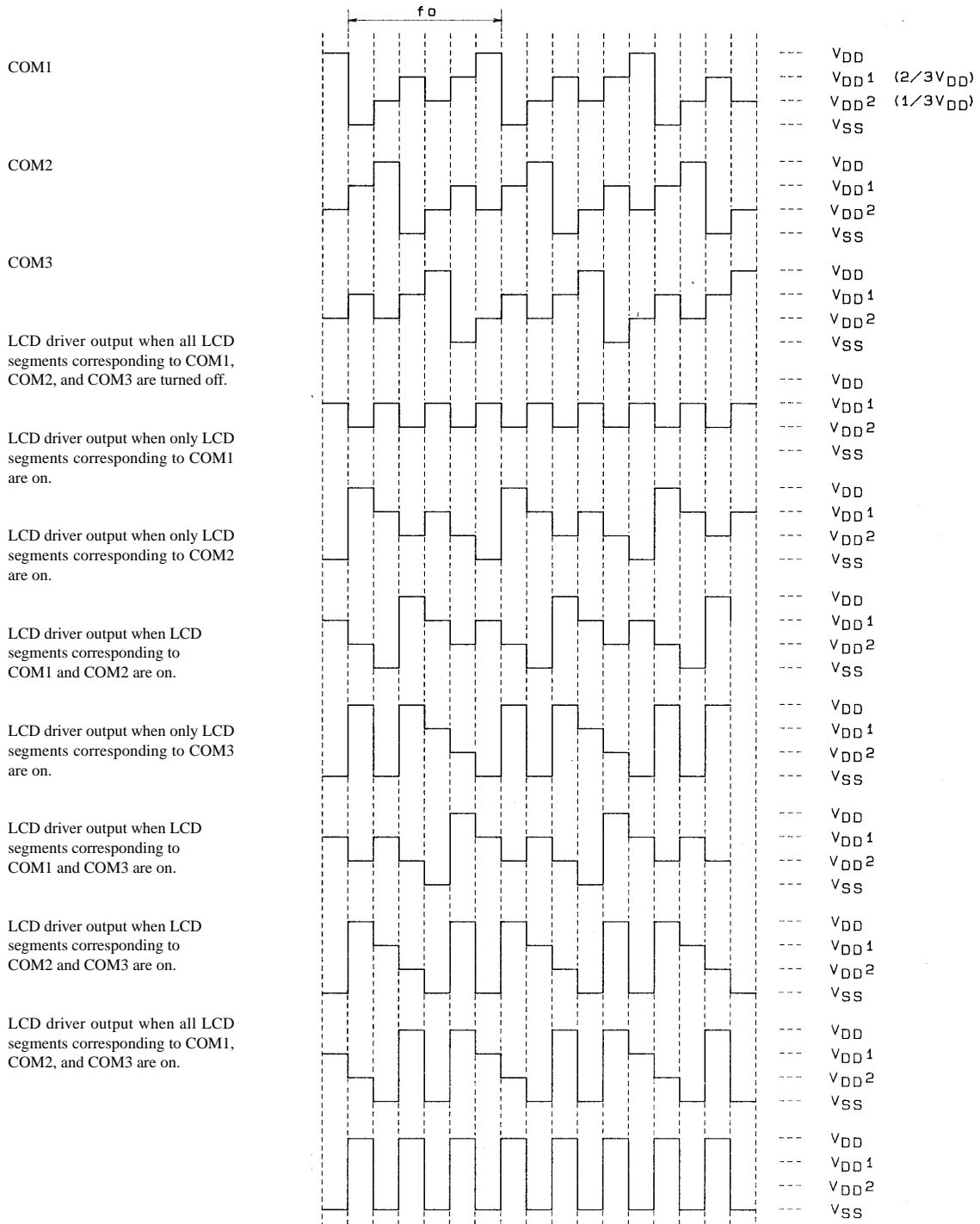
1/2 Bias, 1/3 Duty Drive Technique



1/2 Bias, 1/3 Duty Waveforms

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1/3 Bias, 1/3 Duty Drive Technique



1/3 Bias, 1/3 Duty Waveforms

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$\overline{\text{INH}}$ and Display Control

Since the IC internal data (D1 to D156, DR, SC, and BU) is undefined when power is first applied, $\overline{\text{INH}}$ should be set low at the same time as power is applied, and data should be transferred from the microprocessor while $\overline{\text{INH}}$ is held low. When the data transfer has completed, set $\overline{\text{INH}}$ high. This will prevent meaningless displays at power on.

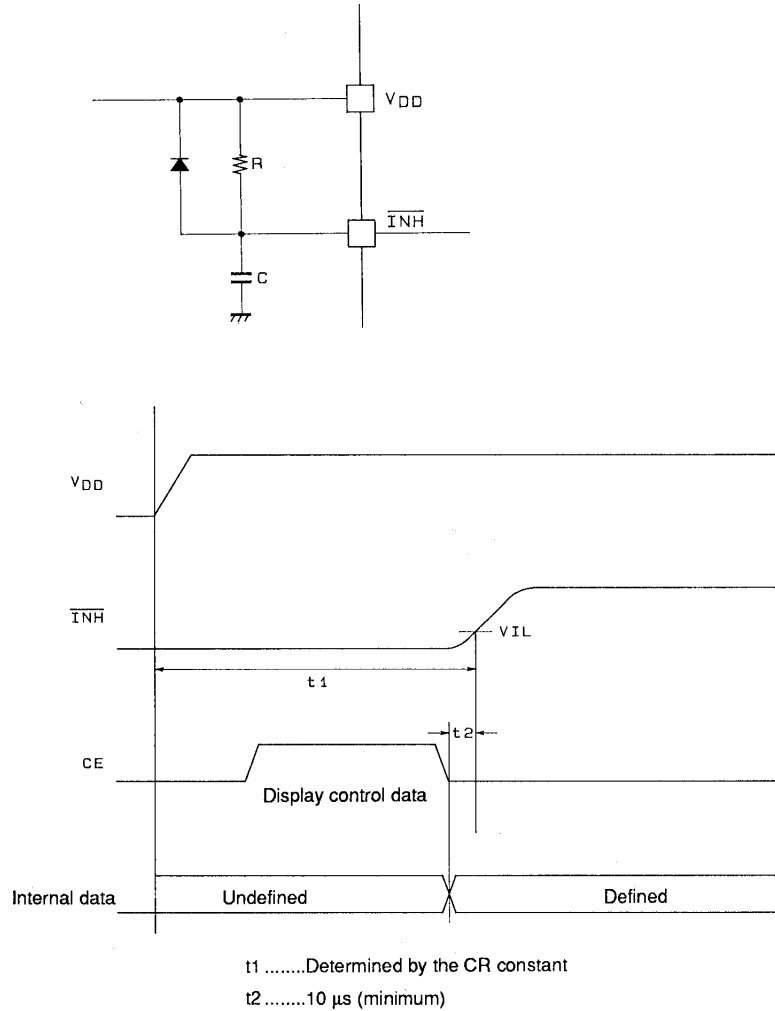
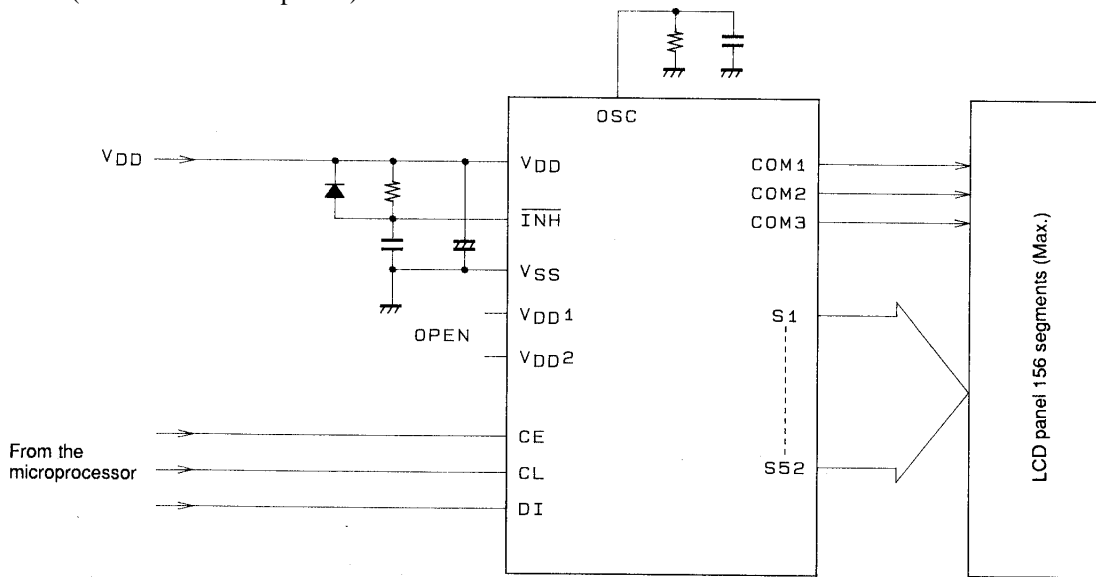


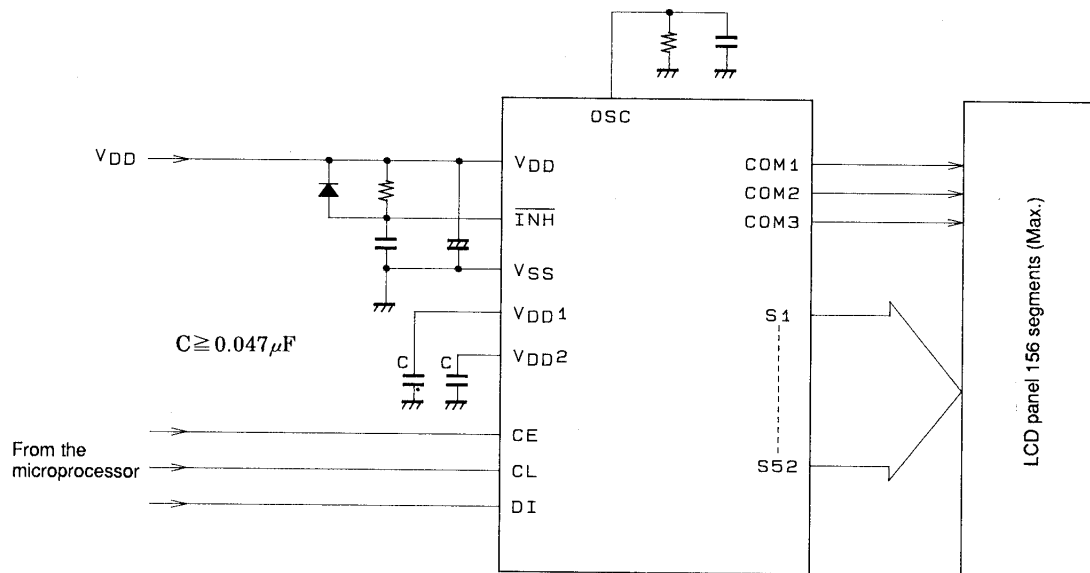
Figure 3

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Application Circuit Example 1 1/3 Bias (for use with small panels)



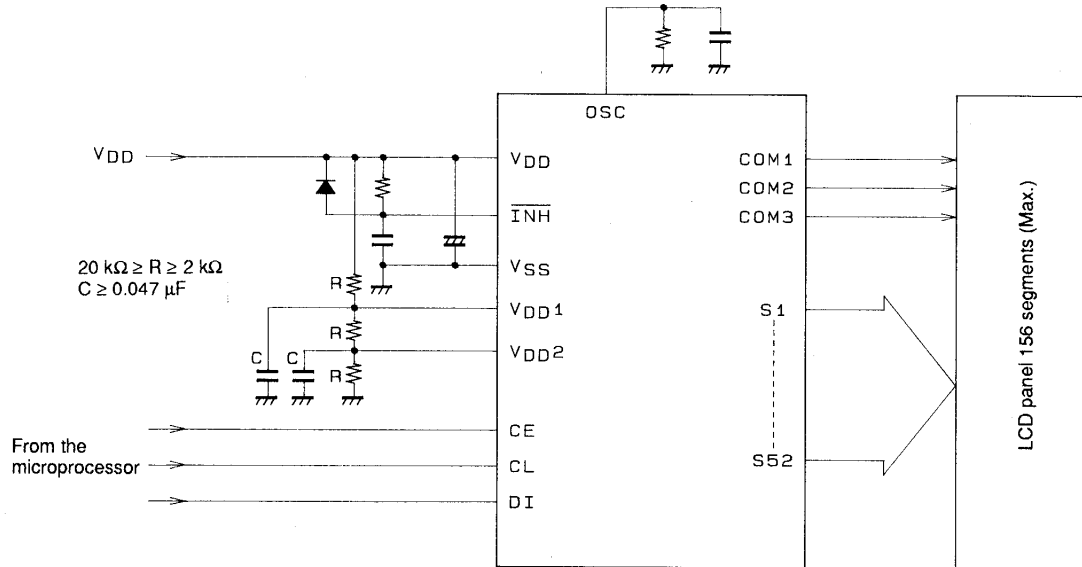
Application Circuit Example 2 1/3 Bias (for use with normal size panels)



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Application Circuit Example 3

1/3 Bias (for use with large panels)



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