Ordering number : EN5811

CMOS LSI

LC78624E

Compact Disc Player DSP

Overview

The LC78624E is a CMOS LSI that implements the signal processing and servo control required by compact disc players. Including an EFM-PLL and text decoder, the LC78624E strictly limits functionality to basic signal processing and servo system operation to achieve the best cost-performance balance for low-end players. As basic functions, the LC78624E provides demodulation of the EFM signal from the optical pickup, de-interleaving, error detection and correction, and processes servo commands sent from the control microcontroller.

Functions

- Input signal processing: The LC78624E takes an HF signal as input, digitizes (slices) that signal at a precise level, converts that signal to an EFM signal, and generates a PLL clock with an average frequency of 4.3218 MHz by comparing the phases of that signal and an internal VCO.
- Precise reference clock and necessary internal timing generation using an external 16.9344 MHz crystal oscillator
- Disk motor speed control using a frame phase difference signal generated from the playback clock and the reference clock
- Frame synchronization signal detection, protection and interpolation to assure stable data readout
- EFM signal demodulation and conversion to 8-bit symbol data
- Subcode data separation from the EFM demodulated signal and output of that data to an external microcontroller
- Subcode Q signal output to a microcontroller over the serial I/O interface after performing a CRC error check (LSB first)
- Serial output to a microcontroller via the text decoder of the song titles and other text data stored in the Subcode R through W channels of the read-in area
- Demodulated EFM signal buffering in internal RAM to handle up to ±4 frames of disk rotational jitter
- Demodulated EFM signal reordering in the prescribed order for data unscrambling and de-interleaving
- Error detection, correction, and flag processing (error correction scheme: dual C1 plus dual C2 correction)
- The LC78624E sets the C2 flags based on the C1 flags and a C2 check, and then performs signal interpolation or muting depending on the C2 flags. The interpolation circuit uses a dual-interpolation scheme. The previous value is held if the C2 flags indicate errors two or more times consecutively.
- Support for command input from a microcontroller: commands include track jump, focus start, disk motor start/stop, muting on/off and track count (8 bit serial input)
- Built-in digital output circuits.
- Arbitrary track counting to support high-speed data access
- Zero cross muting
- Supports the implementation of a double-speed dubbing function.
- Support for bilingual applications.
- General-purpose I/O ports: 5 pins

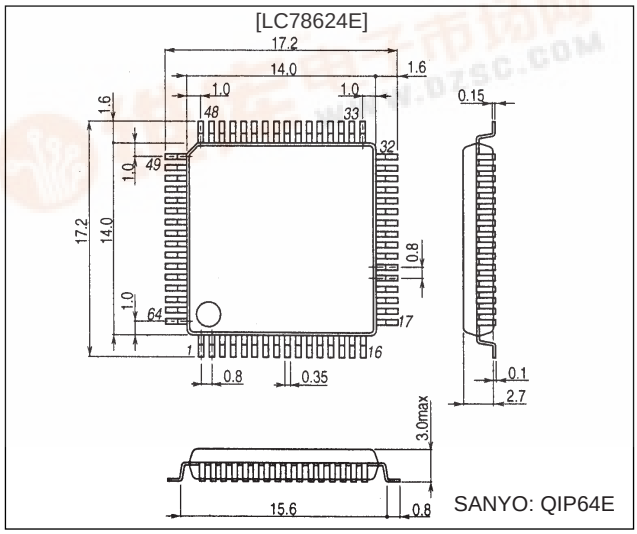
Features

- 64 pin QFP
- 5 V single-voltage power supply

Package Dimensions

unit: mm

3159-QFP64E



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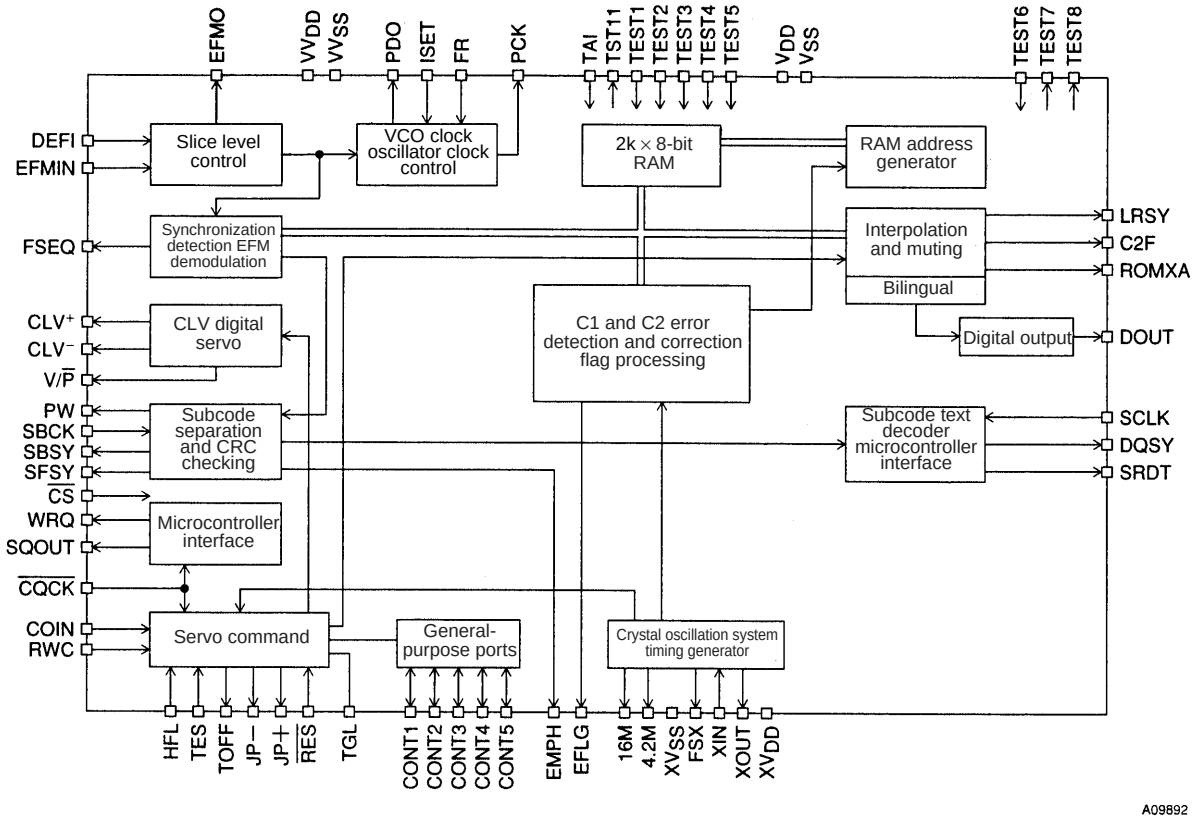
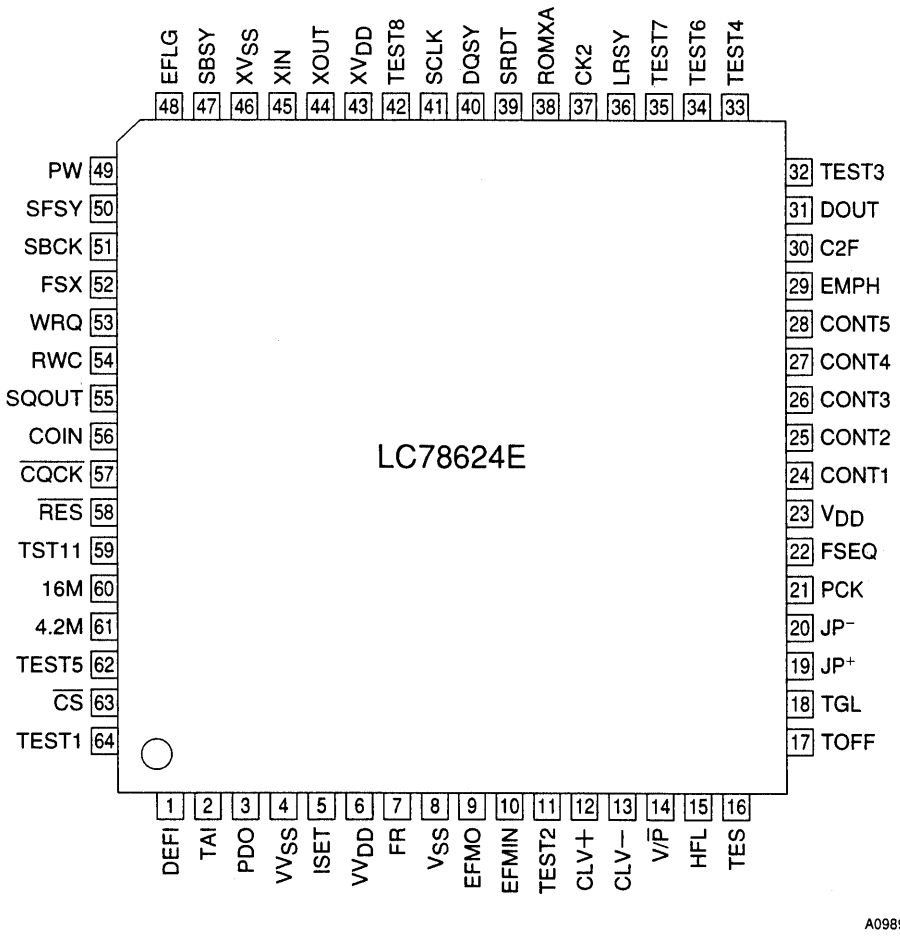
Equivalent Circuit Block Diagram



Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{SS} – 0.3 to V_{SS} + 7.0	V
Input voltage	V_{IN}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD} (1)	V_{DD}, XV_{DD}, VV_{DD}: During normal-speed playback	3.0		5.5	V
	V_{DD} (2)	V_{DD}, XV_{DD}, VV_{DD}: During double-speed playback	3.0		5.5	V
Input high level voltage	V_{IH} (1)	DEFI, COIN, $\overline{RES}$, HFL, TES, SBCK, RWC, $\overline{CQCK}$, TAI, TEST1 to TEST6, $\overline{CS}$, CONT1 to CONT5, SCLK	0.7 V_{DD}		V_{DD}	V
	V_{IH} (2)	EFMIN	0.6 V_{DD}		V_{DD}	V
Input low level voltage	V_{IL} (1)	DEFI, COIN, $\overline{RES}$, HFL, TES, SBCK, RWC, $\overline{CQCK}$, TAI, TEST1 to TEST6, $\overline{CS}$, CONT1 to CONT5, SCLK	0		0.3 V_{DD}	V
	V_{IL} (2)	EFMIN	0		0.4 V_{DD}	V
Data setup time	t_{SU}	COIN, RWC: Figure 1	400			ns
Data hold time	t_{HD}	COIN, RWC: Figure 1	400			ns
High level clock pulse width	t_{WH}	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Low level clock pulse width	t_{WL}	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Data read access time	t_{RAC}	SQOUT, PW: Figures 2 and 3	0		400	ns
Command transfer time	t_{RWC}	RWC: Figure 1	1000			ns
Subcode Q read enable time	t_{SQE}	WRQ: Figure 2, with no RWC signal		11.2		ms
Subcode read cycle time	t_{SC}	SFSY: Figure 3		136		µs
Subcode read enable time	t_{SE}	SFSY: Figure 3	400			ns
Port input data setup time	t_{CSU}	CONT1 to CONT5, RWC: Figure 4	400			ns
Port input data hold time	t_{CHD}	CONT1 to CONT5, RWC: Figure 4	400			ns
Port input clock setup time	t_{RCQ}	RWC, $\overline{CQCK}$: Figure 4	100			ns
Port output data delay time	t_{CDD}	CONT1 to CONT5, RWC: Figure 5			1200	ns
Input level	V_{IN} (1)	EFMIN: Slice level control	1.0			Vp-p
	V_{IN} (2)	X_{IN}: Capacitor-coupled input	1.0			Vp-p
Operating frequency range	fop	EFMIN			10	MHz
Crystal oscillator frequency	f_X	X_{IN}, X_{OUT}		16.9344		MHz
Text readout time	t_{CW}	DQSY : Figure 6.	1.5	3.3	3.7	ms
DQSY pulse width	t_W	DQSY : Figure 6.	60	136	150	µs
SCLK “low” level pulse width	t_{WTL}	SCLK : Figure 6.	100			ns
SCLK “high” level pulse width	t_{WTH}	SCLK : Figure 6.	100			ns
SCLK delay time	t_D1	SCLK : Figure 6.	100			ns
Text data delay time	t_D2	SRDT : Figure 6.			50	ns
	t_D3	SRDT : Figure 6.			50	ns
Reset time	t_{RES}	$\overline{RES}$	400			ns

Electrical Characteristics at Ta = 25°C, V_{DD} = 5 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	I_{DD}	V_{DD}, XV_{DD}, VV_{DD}		25	35	mA
Input high level current	I_{IH} (1)	DEFI, EFMIN, COIN, $\overline{RES}$, HFL, TES, SBCK, RWC, $\overline{CQCK}$: TEST1, SCLK: V_{IN} = V_{DD}			5	µA
	I_{IH} (2)	TAI, TEST2 to TEST6, $\overline{CS}$: V_{IN} = V_{DD} = 5.5 V	25		75	µA
Input low level current	I_{IL}	DEFI, EFMIN, COIN, $\overline{RES}$, HFL, TES, SBCK, RWC, $\overline{CQCK}$: TAI, TEST1 to TEST6, $\overline{CS}$, SCLK: V_{IN} = 0 V	–5			µA
Output high level voltage	V_{OH} (1)	EFMO, CLV+, CLV–, V/$\overline{P}$, PCK, FSEQ, TOFF, TGL, JP+, JP–, EMPH, EFLG, FSX: I_{OH} = –1 mA	4			V
	V_{OH} (2)	TEST7 to TEST8, DQSY, SRDT, LRSY, CK2, ROMXA, C2F, SBSY, PW, SFSY, WRQ, SQOUT, TST11, 16M, 4.2M, CONT1 to CONT5: I_{OH} = –0.5 mA	4			V
	V_{OH} (3)	DOUT: I_{OH} = –12 mA	4.5			V
Output low level voltage	V_{OL} (1)	EFMO, CLV+, CLV–, V/$\overline{P}$, PCK, FSEQ, TOFF, TGL, JP+, JP–, EMPH, EFLG, FSX: I_{OL} = 1 mA			1	V
	V_{OL} (2)	TEST7 to TEST8, DQSY, SRDT, LRSY, CK2, ROMXA, C2F, SBSY, PW, SFSY, WRQ, SQOUT, TST11, 16M, 4.2M, CONT1 to CONT5: I_{OL} = 2 mA			0.4	V
	V_{OL} (3)	DOUT: I_{OL} = 12 mA			0.5	V
Output off leakage current	I_{OFF} (1)	PDO, CLV+, CLV–, JP+, JP–, CONT1 to CONT5: V_{OUT} = V_{DD}			5	µA
	I_{OFF} (2)	PDO, CLV+, CLV–, JP+, JP–, CONT1 to CONT5: V_{OUT} = 0 V	–5			µA
Charge pump output current	I_{PDOH}	PDO: R_{ISET} = 68 kΩ	64	80	96	µA
	I_{PDOL}	PDO: R_{ISET} = 68 kΩ	–96	–80	–64	µA

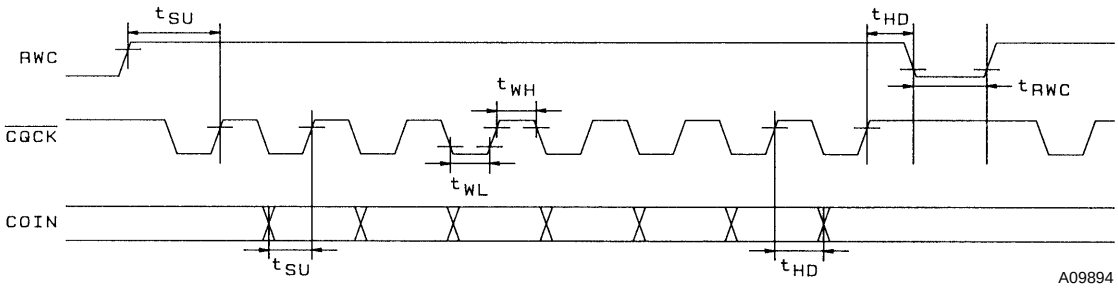


Figure 1 Command Input

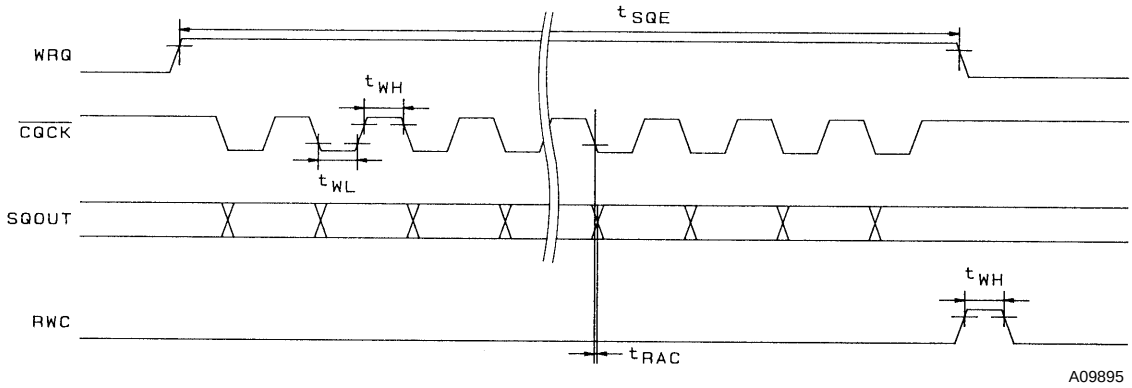


Figure 2 Subcode Q Output

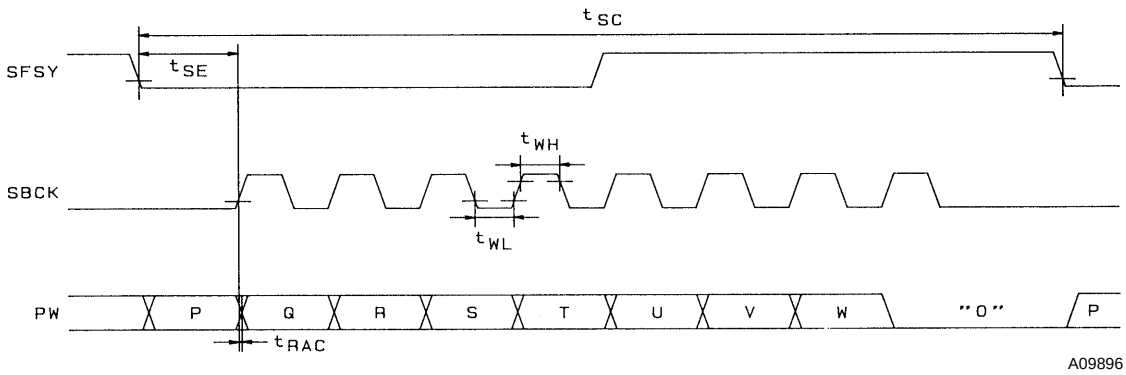


Figure 3 Subcode Output

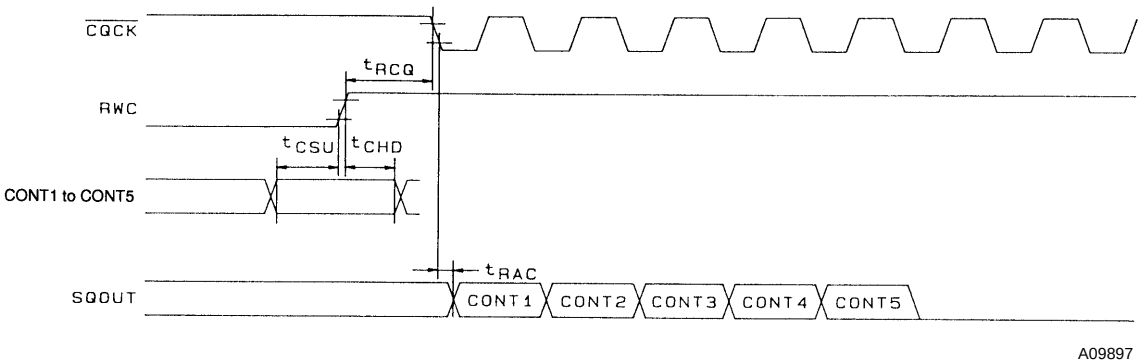


Figure 4 General-Purpose Port Input Timing

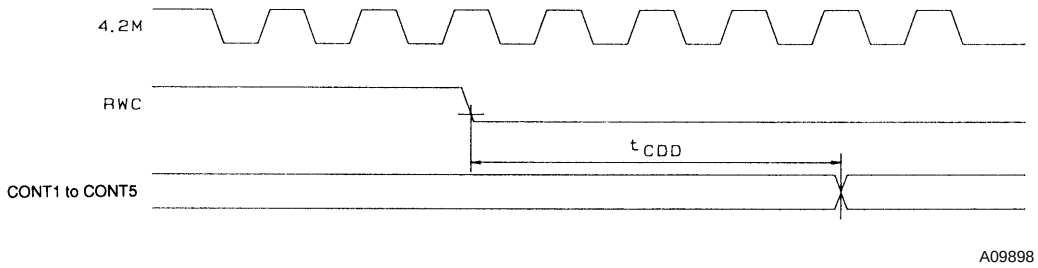


Figure 5 General-Purpose Port Output Timing

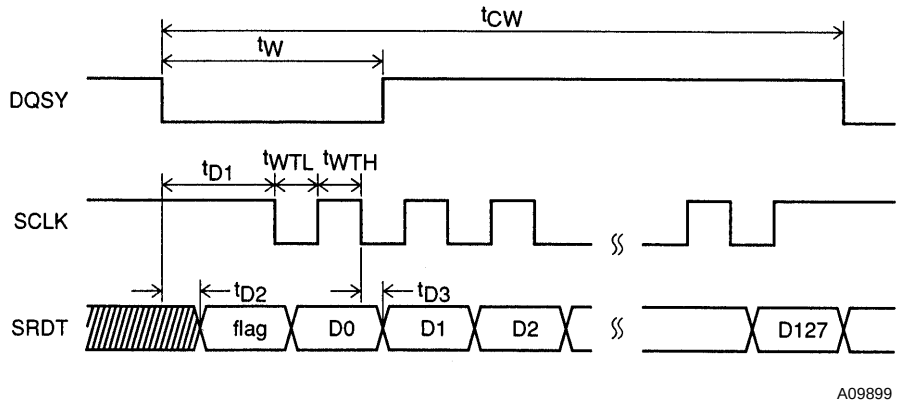


Figure 6 Text Data Output Timing

Pin Functions

Pin No.	Symbol	I/O	Function	
1	DEFI	I	Defect detection signal (DEF) input. (Must be connected to 0 V when unused.)	
2	TAI	I	PLL pins	Test input. A pull-down resistor is built in. Must be connected to 0 V.
3	PDO	O		External VCO control phase comparator output
4	VV_{SS}	–		Internal VCO ground. Must be connected to 0 V.
5	ISET	AI		PDO output current adjustment resistor connection
6	VV_{DD}	–		Internal VCO power supply
7	FR	AI		VCO frequency range adjustment
8	V_{SS}	–	Digital system ground. Must be connected to 0 V.	
9	EFMO	O	Slice level control	EFM signal output
10	EFMIN	I		EFM signal input
11	TEST2	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
12	CLV^+	O	Disc motor control output. Three-value output is also possible when specified by microcontroller command.	
13	CLV^-	O		
14	$V/\overline{P}$	O	Rough servo/phase control automatic switching monitor output. Outputs a high level during rough servo and a low level during phase control.	
15	HFL	I	Track detection signal input. This is a Schmitt input.	
16	TES	I	Tracking error signal input. This is a Schmitt input.	
17	TOFF	O	Tracking off output	
18	TGL	O	Tracking gain switching output. Increase the gain when low.	
19	JP^+	O	Track jump control output. Three-value output is also possible when specified by microcontroller command.	
20	JP^-	O		
21	PCK	O	EFM data playback clock monitor. Outputs 4.3218 MHz when the phase is locked.	
22	FSEQ	O	Synchronization signal detection output. Outputs a high level when the synchronization signal detected from the EFM signal and the internally generated synchronization signal agree.	
23	V_{DD}	–	Digital system power supply.	
24	CONT1	I/O	General-purpose I/O pin 1	Controlled by serial data commands from the microcontroller. Any of these that are unused must be either set up as input ports and connected to 0 V, or set up as output ports and left open.
25	CONT2	I/O	General-purpose I/O pin 2	
26	CONT3	I/O	General-purpose I/O pin 3	
27	CONT4	I/O	General-purpose I/O pin 4	
28	CONT5	I/O	General-purpose I/O pin 5	
29	EMPH	O	De-emphasis monitor pin. A high level indicates playback of a de-emphasis disk.	
30	C2F	O	C2 flag output	
31	DOUT	O	Digital output. (EIAJ format)	
32	TEST3	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
33	TEST4	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
34	TEST6	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.	
35	TEST7	O	Test output	
36	LRSY	O	ROMXA output	L/R clock output
37	CK2	O		Bit clock output
38	ROMXA	O		Interpolated data output, not ROM output
39	SRDT	O	Text data output	
40	DQSY	O	Text readout enable output	
41	SCLK	I	Text shift clock input	
42	TEST8	O	Test output	
43	XV_{DD}	–	Crystal oscillator power supply.	
44	X_{OUT}	O	Connections for a 16.9344 crystal oscillator element	
45	X_{IN}	I		
46	XV_{SS}	–	Crystal oscillator ground. Must be connected to 0 V.	
47	SBSY	O	Subcode block synchronization signal output	
48	EFLG	O	C1, C2, single and double error correction monitor pin	
49	PW	O	Subcode P, Q, R, S, T, U, V and W output	
50	SFSY	O	Subcode frame synchronization signal output. This signal falls when the subcodes are in the standby state.	

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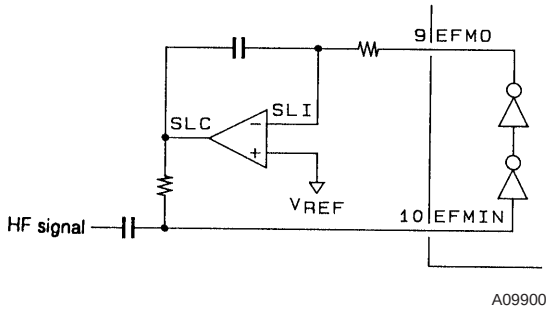
Pin No.	Symbol	I/O	Function
51	SBCK	I	Subcode readout clock input. This is a Schmitt input. (Must be connected to 0 V when unused.)
52	FSX	O	Output for the 7.35 kHz synchronization signal divided from the crystal oscillator
53	WRQ	O	Subcode Q output standby output
54	RWC	I	Read/write control input. This is a Schmitt input.
55	SQOUT	O	Subcode Q output
56	COIN	I	Command input from the control microcontroller
57	$\overline{\text{CQCK}}$	I	Input for both the command input clock and the subcode readout clock. This is a Schmitt input.
58	$\overline{\text{RES}}$	I	Chip reset input. This pin must be set low briefly after power is first applied.
59	TST11	O	Test output. Leave open. (Normally outputs a low level.)
60	16M	O	16.9344 MHz output.
61	4.2M	O	4.2336 MHz output
62	TEST5	I	Test input. A pull-down resistor is built in. Must be connected to 0 V.
63	$\overline{\text{CS}}$	I	Chip select input. A pull-down resistor is built in. Must be connected to 0 V if not controlled.
64	TEST1	I	Test input. No pull-down resistor. Must be connected to 0 V.

Note: The same potential must be supplied to all power supply pins, i.e., V_{DD}, VV_{DD} and XV_{DD}.

Pin Applications

1. HF Signal Input Circuit; Pin 10: EFMIN, pin 9: EFMO, pin 1: DEFI, pin 12: CLV+

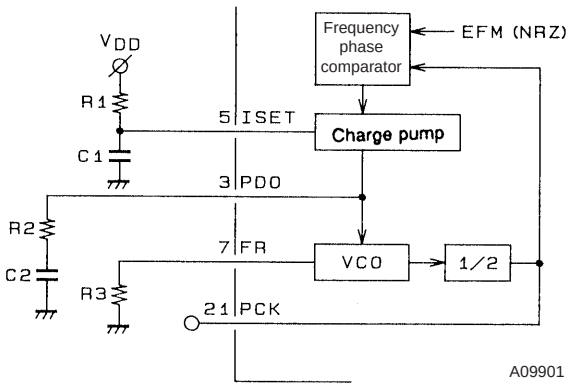


An EFM signal (NRZ) sliced at an optimal level can be acquired by inputting the HF signal to EFMIN.

The LC78624E handles defects as follows. When a high level is input to the DEFI pin (pin 1), EFMO (pin 9) pins (the slice level control outputs) go to the high-impedance state, and the slice level is held. However, note that this function is only valid in CLV phase control mode, that is, when the V/$\overline{\text{P}}$ pin (pin 14) is low. This function can be used in combination with the LA9230M, and LA9240M DEF pins.

Note: If the EFMIN and CLV+ signal lines are too close to each other, unwanted radiation can result in error rate degradation. We recommend laying a ground or V_{DD} shield line between these two lines.

2. PLL Clock Generation Circuit; Pin 3: PDO, pin 5: ISET, pin 7: FR, pin 21: PCK



Since the LC78624E includes a VCO circuit, a PLL circuit can be formed by connecting external R and C (resistors and capacitors). ISET is the charge pump reference current, PDO is the VCO circuit loop filter, and FR is a resistor that determines the VCO frequency range.

(Reference values)

R1 = 68 kΩ, C1 = 0.1 µF

R2 = 680 Ω, C2 = 0.1 µF

R3 = 1.2 kΩ

Code	COMMAND	$\overline{\text{RES}}$ = low
$AC	VCO × 2 SET	
$AD	VCO × 1 SET	○

The $V_{CO} \times 2$ command is an auxiliary command for characteristics guarantee in low-voltage operations. This command supports the low-voltage operations at V_{DD} = 3.0 to 3.6 V.

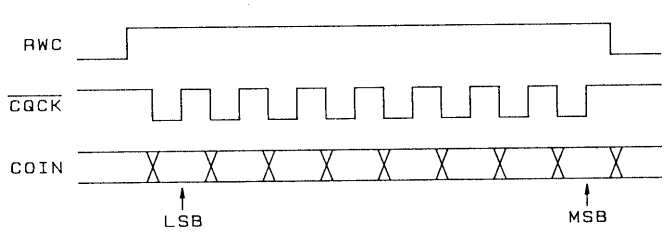
3. 1/2 VCO Monitor; Pin 21: PCK
   PCK is a monitor pin that outputs an average frequency of 4.3218 MHz, which is divided by two from the VCO frequency.

4. Synchronization Detection Monitor; Pin 22: FSEQ
   Pin 22 goes high when the frame synchronization (a positive polarity synchronization signal) from the EFM signal read in by PCK and the timing generated by the counter (the interpolation synchronization signal) agree. This pin is thus a synchronization detection monitor. (It is held high for a single frame.)

5. Servo Command Function; Pin 54: RWC, pin 56: COIN, pin 57: $\overline{\text{CQCK}}$
   Commands can be executed by setting RWC high and inputting commands to the COIN pin in synchronization with the $\overline{\text{CQCK}}$ clock. Note that commands are executed on the falling edge of RWC.

Focus start Track jump Muting control Disk motor control Miscellaneous control	One-byte commands
Track check	Two-byte command (RWC set twice)
General-purpose I/O, E/D	Two-byte commands (RWC set once)

• One-byte commands



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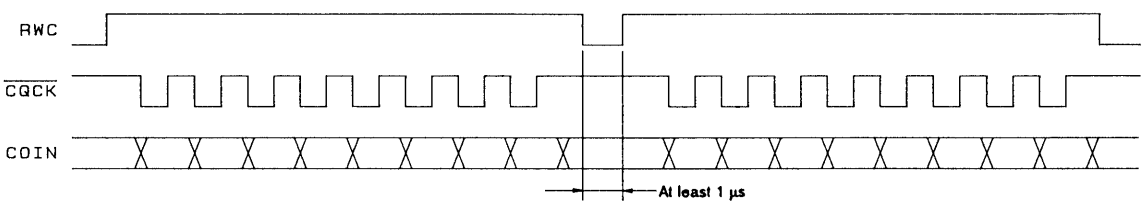
• Two-byte commands (RWC set twice : For track checking)



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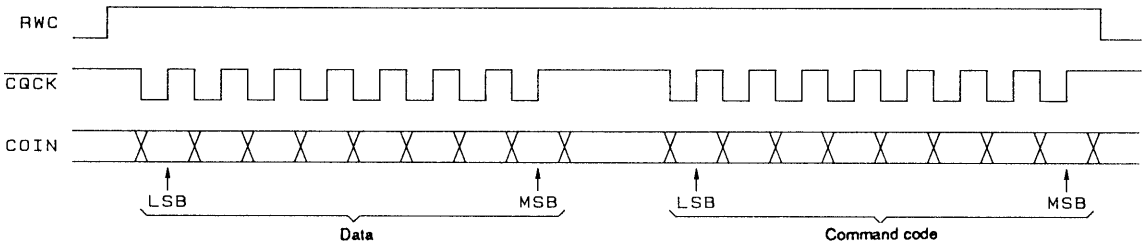
• Two-byte commands (RWC set once: Sets up the general-purpose I/O ports)



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• Command noise rejection

Code	Command	$\overline{\text{RES}}$ = low
$EF	COMMAND INPUT NOISE REDUCTION MODE	
$EE	RESET THE MODE ABOVE	○

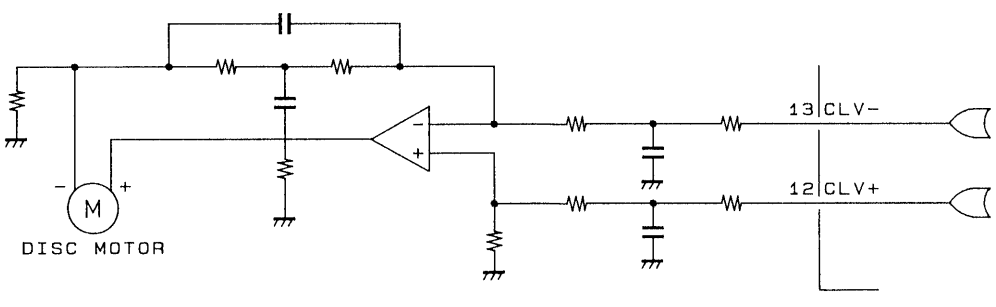
This command reduces the noise on the $\overline{\text{CQCK}}$ clock signal. While this is effective for noise pulses shorter than 500 ns, the $\overline{\text{CQCK}}$ timings t_{WL}, t_{WH}, and t_{SU}, must be set for at least 1 µs.

6. CLV Servo Circuit; Pin 12: CLV+, pin 13: CLV–, pin 14: V/$\overline{\text{P}}$

Code	Command	$\overline{\text{RES}}$ = low
$04	DISC MOTOR START (accelerate)	
$05	DISC MOTOR CLV (CLV)	
$06	DISC MOTOR BRAKE (decelerate)	
$07	DISC MOTOR STOP (stop)	○

The CLV+ pin provides the signal that accelerates the disk in the forward direction and the CLV– pin provides the signal that decelerates the disk. Commands from the microcontroller select one of four modes; accelerate, decelerate, CLV and stop. The table below lists the CLV+ and CLV– outputs in each of these modes.

Mode	CLV+	CLV–
Accelerate	High	Low
Decelerate	Low	High
CLV	Pulse output	Pulse output
Stop	Low	Low



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Note: CLV servo control commands can set the TOFF pin low only in CLV mode. That pin will be at the high level at all other times. Control of the TOFF pin by microcontroller command is only valid in CLV mode.

- CLV mode

  In CLV mode the LC78624E detects the disk speed from the HF signal and provides proper linear speed using several different control schemes by switching the DSP internal modes. The PWM reference period corresponds to a frequency of 7.35 kHz. The V/$\overline{P}$ pin outputs a high level during rough servo and a low level during phase control.

Internal mode	CLV+	CLV−	V/$\overline{P}$
Rough servo (velocity too low)	High	Low	High
Rough servo (velocity too high)	Low	High	High
Phase control (PCK locked)	PWM	PWM	Low

- Rough servo gain switching

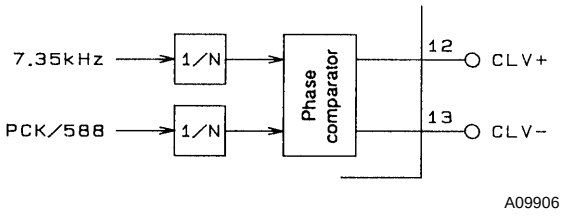
Code	Command	$\overline{RES}$ = low
$A8	DISC 8 cm SET	
$A9	DISC 12 cm SET	○

For 8 cm disks, the rough servo mode CLV control gain can be set about 8.5 dB lower than the gain used for 12 cm disks.

- Phase control gain switching

Code	Command	$\overline{RES}$ = low
$B1	CLV PHASE COMPARATOR DIVISOR: 1/2	
$B2	CLV PHASE COMPARATOR DIVISOR: 1/4	
$B3	CLV PHASE COMPARATOR DIVISOR: 1/8	
$B0	NO CLV PHASE COMPARATOR DIVISOR USED	○

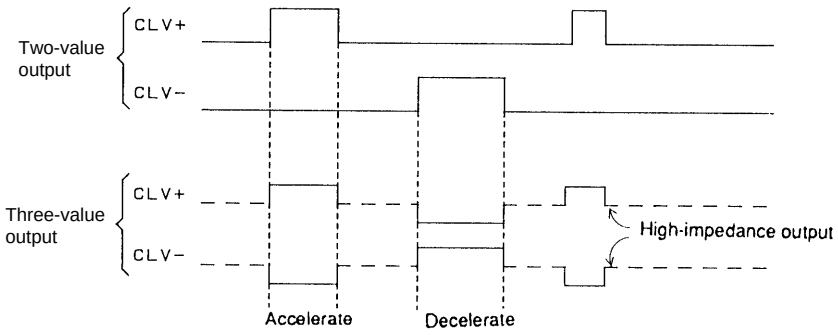
The phase control gain can be changed by changing the divisor used by the dividers in the stage immediately preceding the phase comparator.



• CLV three-value output

Code	Command	$\overline{RES}$ = low
$B4	CLV THREE-VALUE OUTPUT	
$B5	CLV TWO-VALUE OUTPUT (the scheme used by previous products)	○

The CLV three-value output command allows the CLV to be controlled by a single pin.



A09907

• Internal brake modes

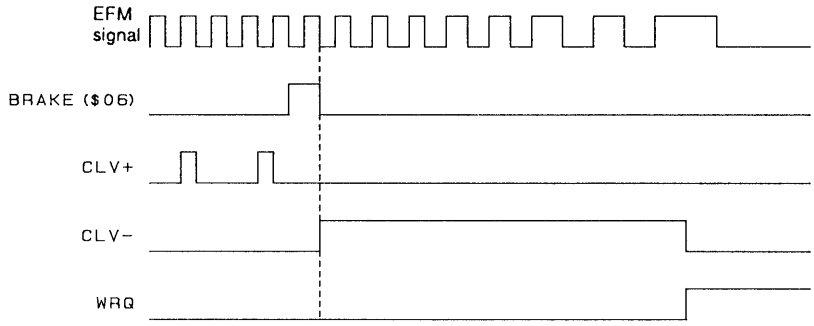
Code	Command	$\overline{RES}$ = low
$C5	INTERNAL BRAKE ON	
$C4	INTERNAL BRAKE OFF	○
$A3	INTERNAL BRAKE CONTROL	
$CB	INTERNAL BRAKE CONTINUOUS MODE	
$CA	RESET CONTINUOUS MODE	○
$CD	TON MODE DURING INTERNAL BRAKING	
$CC	RESET TON MODE	○

— Issuing the internal brake-on ($C5) command sets the LC78624E to internal brake mode. In this mode, the disk deceleration state can be monitored from the WRQ pin when a brake command ($06) is executed.

— In this mode the disk deceleration state is determined by counting the EFM signal density in a single frame, and when the EFM signal count falls under four, the CLV⁻ pin is dropped to low. At the same time the WRQ signal, which functions as a brake completion monitor, goes high. When the microcontroller detects a high level on the WRQ signal, it should issue a STOP command to fully stop the disk. In internal brake continuous mode ($CB), the CLV⁻ pin high-level output braking operation continues even after the WRQ brake completion monitor goes high.

Note that if errors occur in deceleration state determination due to noise in the EFM signal, the problem may be rectified by changing the EFM signal count from four to eight with the internal brake control command ($A3).

— In TOFF output disabled mode ($CD), the TOFF pin is held low during internal brake operations. We recommend using this feature, since it is effective at preventing incorrect detection at the disk mirror surface.



Note: 1. If focus is lost during the execution of an internal brake command, the pickup must first be refocussed and then the internal brake command must be reissued.
2. Since incorrect deceleration state determination is possible depending on the EFM signal playback state (e.g., disk defects, access in progress), we recommend using these functions in combination with a microcontroller.

7. Track Jump Circuit; Pin 15: HFL, pin 16: TES, pin 17: TOFF, pin 18: TGL, pin 19: JP^+, pin 20: JP^-

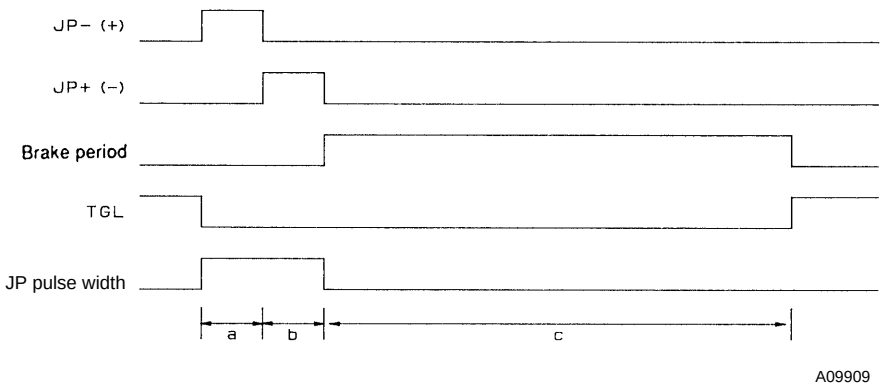
- The LC78624E supports the two track count modes listed below.

Code	Command	$\overline{RES}$ = low
$22	NEW TRACK COUNT (using the TES/HFL combination)	○
$23	STANDARD TRACK COUNT (directly counts the TES signal)	

The earlier track count function uses the TES signal directly as the internal track counter clock.
To reduce counting errors resulting from noise on the rising and falling edges of the TES signal, the new track count function prevents noise induced errors by using the combination of the TES and HFL signals, and implements a more reliable track count function. However, dirt and scratches on the disk can result in HFL signal dropouts that may result in missing track count pulses. Thus care is required when using this function.

• TJ commands

Code	Command	$\overline{RES}$ = low
$A0	STANDARD TRACK JUMP	○
$A1	NEW TRACK JUMP	
$11	1 TRACK JUMP IN #1	
$12	1 TRACK JUMP IN #2	
$31	1 TRACK JUMP IN #3	
$52	1 TRACK JUMP IN #4	
$10	2 TRACK JUMP IN	
$13	4 TRACK JUMP IN	
$14	16 TRACK JUMP IN	
$30	32 TRACK JUMP IN	
$15	64 TRACK JUMP IN	
$17	128 TRACK JUMP IN	
$19	1 TRACK JUMP OUT #1	
$1A	1 TRACK JUMP OUT #2	
$39	1 TRACK JUMP OUT #3	
$5A	1 TRACK JUMP OUT #4	
$18	2 TRACK JUMP OUT	
$1B	4 TRACK JUMP OUT	
$1C	16 TRACK JUMP OUT	
$38	32 TRACK JUMP OUT	
$1D	64 TRACK JUMP OUT	
$1F	128 TRACK JUMP OUT	
$16	256 TRACK CHECK	
$0F	TOFF	
$8F	TON	○
$8C	TRACK JUMP BRAKE	
$21	TOFF OUTPUT MODE DURING JP PULSE PERIOD	
$20	RESET TOFF OUTPUT MODE DURING JP PULSE PERIOD	○



When the LC78624E receives a track jump instruction as a servo command, it first generates accelerating pulses (period a) and next generates deceleration pulses (period b). The passage of the braking period (period c) completes the specified jump. During the braking period, the LC78624E detects the beam slip direction from the TES and HFL inputs. TOFF is used to cut the components in the TES signal that aggravate slip. The jump destination track is captured by increasing the servo gain with TGL. In during TOFF output mode JP pulse period the TOFF signal is held high during the JP pulse generation period.

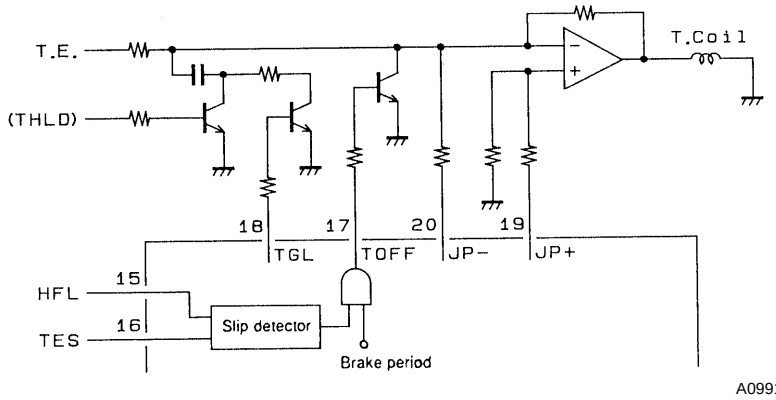
Note: Of the modes related to disk motor control, the TOFF pin only goes low in CLV mode, and will be high during accelerate, stop, and decelerate modes.Note that the TOFF pin can be turned on and off independently by microcontroller issued commands. However, this function is valid only when disk motor control is in CLV mode.

- Track jump modes

  The table lists the relationships between acceleration pulses (the a period) , deceleration pulses (the b period), and the braking period (the c period).

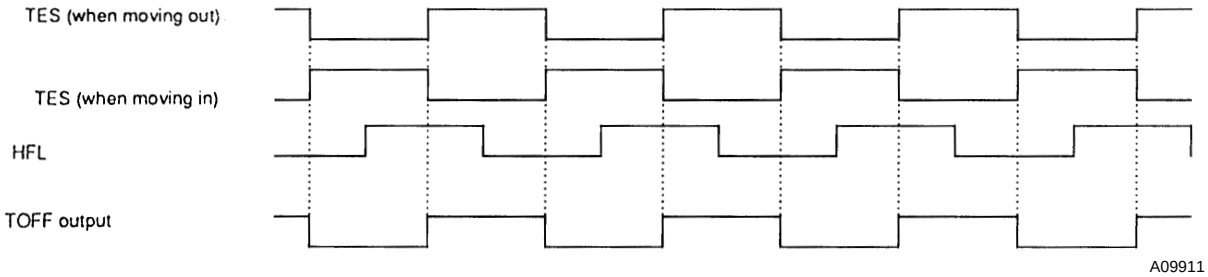
Command	Standard track jump mode			New track jump mode		
	a	b	c	a	b	c
1 TRACK JUMP IN (OUT) #1	233 µs	233 µs	60 ms	233 µs	233 µs	60 ms
1 TRACK JUMP IN (OUT) #2	0.5 track jump period	233 µs	60 ms	0.5 track jump period	The same time as “a”	60 ms
1 TRACK JUMP IN (OUT) #3	0.5 track jump period	233 µs	This period does not exist.	0.5 track jump period	The same time as “a”	This period does not exist.
1 TRACK JUMP IN (OUT) #4	0.5 track jump period	233 µs	60 ms; TOFF is low during the C period.	0.5 track jump period	The same time as “a”	60 ms; TOFF is low during the C period.
2 TRACK JUMP IN (OUT)	None	None	None	1 track jump period	The same time as “a”	60 ms
4 TRACK JUMP IN (OUT)	2 track jump period	466 µs	60 ms	2 track jump period	The same time as “a”	60 ms
16 TRACK JUMP IN (OUT)	9 track jump period	7 track jump period	60 ms	9 track jump period	The same time as “a”	60 ms
32 TRACK JUMP IN (OUT)	18 track jump period	14 track jump period	60 ms	18 track jump period	14 track jump period	60 ms
64 TRACK JUMP IN (OUT)	36 track jump period	28 track jump period	60 ms	36 track jump period	28 track jump period	60 ms
128 TRACK JUMP IN (OUT)	72 track jump period	56 track jump period	60 ms	72 track jump period	56 track jump period	60 ms
256 TRACK CHECK	TOFF goes high during the period when 256 tracks are passed over. The a and b pulses are not output.		60 ms	TOFF goes high during the period when 256 tracks are passed over. The a and b pulses are not output.		60 ms
TRACK JUMP BRAKE	There are no a or b periods.		60ms	There are no a and b periods.		60 ms

Note: 1. As indicated in the table, actuator signals are not output during the 256 TRACK CHECK function. This is a mode in which the TES signal is counted in the tracking loop off state. Therefore, feed motor forwarding is required.
2. The servo command register is automatically reset after one cycle of the track jump sequence (a, b, c) completes.
3. If another track jump command is issued during a track jump operation, the content of that new command will be executed starting immediately.
4. The 1 TRACK JUMP #3 mode does not have a braking period (the C period). Since brake mode must be generated by an external circuit, care is required when using this mode.
5. While there was no braking period (the C period) in the LC78620E/21E for the new track jump command “2 TRACK JUMP IN (OUT)”, this has been changed in this LSI, which has a C period of 60 ms.



The THLD signal is generated by the LA9230M, or LA9240M, and the tracking signal is held during the JP pulse period.

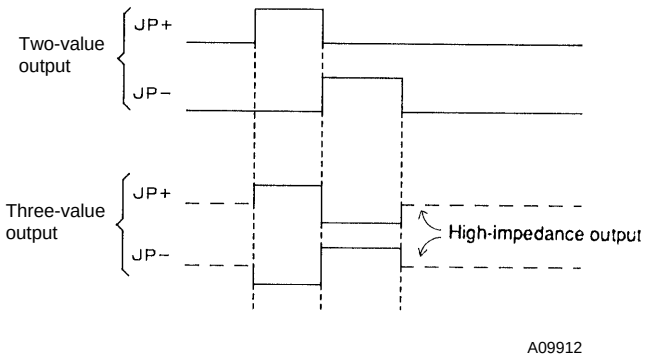
6. Tracking brake
   The chart shows the relationships between the TES, HFL, and TOFF signals during the track jump C period. The TOFF signal is extracted from the HFL signal by TES signal edges. When the HFL signal is high, the pickup is over the mirror surface, and when low, the pickup is over data bits. Thus braking is applied based on the TOFF signal being high when the pickup is moving from a mirror region to a data region and being low when the pickup is moving from a data region to a mirror region.



- JP three-value output

Code	Command	$\overline{\text{RES}}$ = low
$B6	JP THREE-VALUE OUTPUT	
$B7	JP TWO-VALUE OUTPUT (earlier scheme)	○

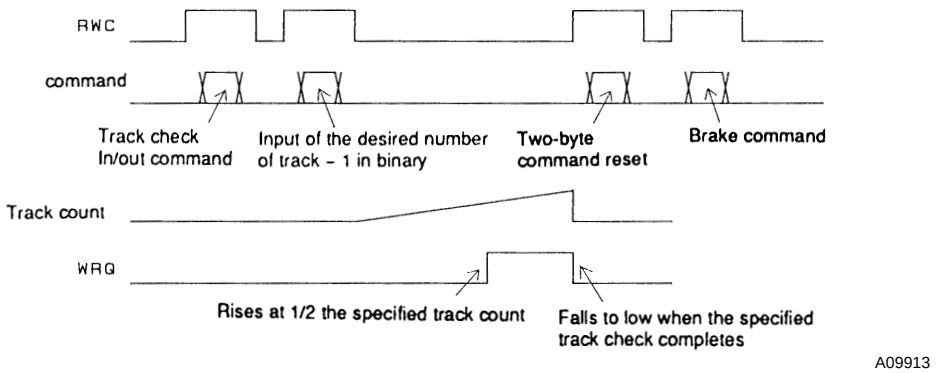
The JP three-value output command allows the track jump operation to be controlled from a single pin.



- Track check mode

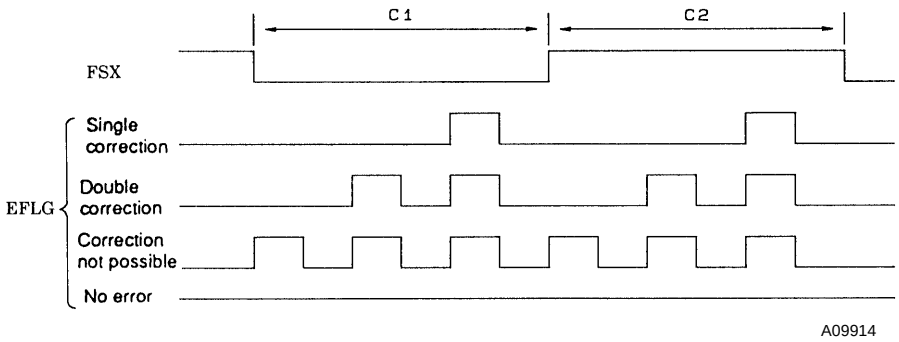
Code	Command	$\overline{\text{RES}}$ = low
$F0	TRACK CHECK IN	
$F8	TRACK CHECK OUT	
$FF	TWO-BYTE COMMAND RESET	○

The LC78624E will count the specified number of tracks plus one when the microcontroller sends an arbitrary binary value in the range 8 to 254 after issuing either a track check in or a track check out command.



Note: 1. When the desired track count has been input in binary, the track check operation is started by the fall of RWC.
2. During a track check operation the TOFF pin goes high and the tracking loop is turned off. Therefore, feed motor forwarding is required.
3. When a track check in/out command is issued the function of the WRQ signal switches from the normal mode subcode Q standby monitor function to the track check monitor function. This signal goes high when the track check is half completed, and goes low when the check finishes. The microcontroller should monitor this signal for a low level to determine when the track check completes.
4. If a two-byte reset command is not issued, the track check operation will repeat. That is, to skip over 20,000 tracks, issue a track check 201 command once, and then count the WRQ signal 100 times. This will check 20,000 tracks.
5. After performing a track check operation, use the brake command to have the pickup lock onto the track.

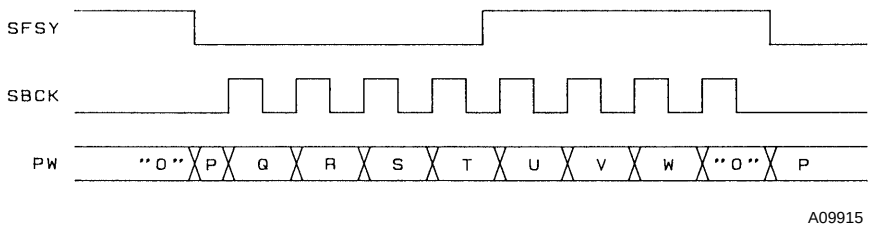
8. Error Flag Output; Pin 48: EFLG, pin 52: FSX



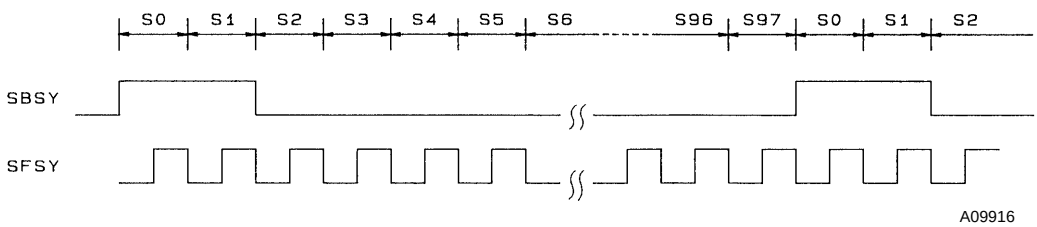
The FSX signal is generated by dividing the crystal oscillator clock, and is a 7.35 kHz frame synchronization signal. The error correction state for each frame is output from EFLG. The FSX low-level period indicates the C1 correction state, and the high-level period indicates the C2 correction state. The playback OK/NG state can be easily determined from the extent of the high level that appears here.

9. Subcodes P, Q and R to W Output Circuit; Pin 49: PW, pin 47: SBSY, pin 50: SFSY, pin 51: SBCK
PW is the subcode signal output pin, and all the codes, P, Q, and R to W can be read out by sending eight clocks to the SBCK pin within 136 μs after the fall of SFSY. The signal that appears on the PW pin changes on the rising edge of SBCK. SFSY is a signal that is output for each subcode frame cycle, and the falling edge of this signal indicates standby for the output of the subcode symbol (P to W). Subcode data P is output on the fall of this signal. However, when the text data is read or reset, subcodes cannot be read because the LC78624E is in the text mode. The subcodes can be read by inputting the SW1P ON command.

Code	Command	$\overline{\text{RES}}$ = low
$4E	SW1P OFF	○
$4F	SW1P ON	



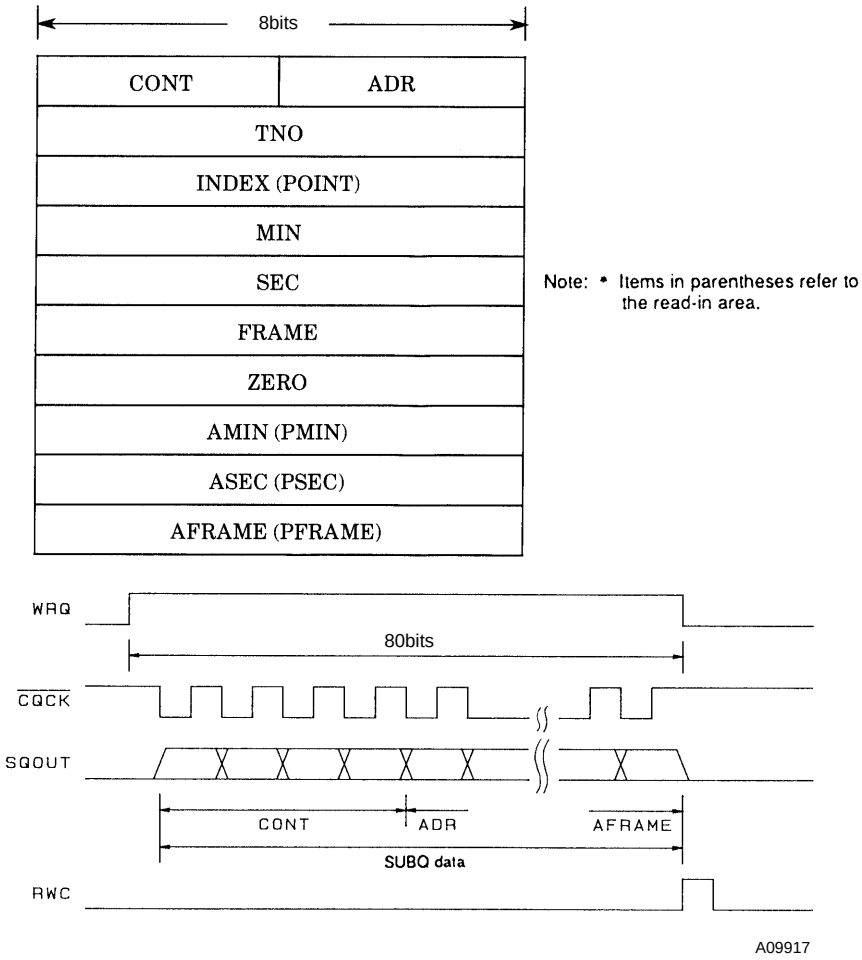
SBSY is a signal output for each subcode block. This signal goes high for the S0 and S1 synchronization signals. The fall of this signal indicates the end of the subcode synchronization signals and the start of the data in the subcode block. (EIAJ format)



10. Subcode Q Output Circuit; Pin 53: WRQ, pin 54: RWC, pin 55: SQOUT, pin 57: $\overline{\text{CQCK}}$, pin 63: $\overline{\text{CS}}$

Code	Command	$\overline{\text{RES}}$ = low
$09	ADDRESS FREE	
$89	ADDRESS 1	○

Subcode Q can be read from the SQOUT pin by applying a clock to the $\overline{\text{CQCK}}$ pin.
Of the eight bits in the subcode, the Q signal is used for song (track) access and display. The WRQ will be high only if the data passed the CRC error check and the subcode Q format internal address is 1*. The microcontroller can read out data from SQOUT in the order shown below by detecting this high level and applying $\overline{\text{CQCK}}$. When $\overline{\text{CQCK}}$ is applied the DSP disables register update internally. The microcontroller should give update permission by setting RWC high briefly after reading has completed. WRQ will fall to low at this time. Since WRQ falls to low 11.2 ms after going high, $\overline{\text{CQCK}}$ must be applied during the high period. Note that data is read out in an LSB first format.
Note: * That state will be ignored if an address free command is input. This is provided to handle CDV applications.



Note: 1. Normally, the WRQ pin indicates the subcode Q standby state. However, it is used for a different monitoring purpose in track check mode and during internal braking. (See the items on track counting and internal braking for details.)
2. The LC78624E becomes active when the $\overline{\text{CS}}$ pin is low, and subcode Q data is output from the SQOUT pin. When the $\overline{\text{CS}}$ pin is high, the SQOUT pin goes to the high-impedance state.

11. Bilingual Function

Code	Command	$\overline{RES}$ = low
$28	STO CONT	○
$29	Lch CONT	
$2A	Rch CONT	

- Following a reset or when a stereo ($28) command has been issued, the left and right channel data is output to the left and right channels respectively.
- When an Lch set ($29) command is issued, the left and right channels both output the left channel data.
- When an Rch set ($2A) command is issued, the left and right channels both output the right channel data.

12. De-Emphasis; Pin 29: EMPH

The preemphasis on/off bit in the subcode Q control information is output from the EMPH pin. When this pin is high, the LC78624E internal de-emphasis circuit operates.

13. C2 Flag Output; Pin 30: C2F

C2F output flag information in 8-bit units to indicate data error.

14. Digital Output Circuit; Pin 31: DOUT

This is an output pin for use with a digital audio interface. Data is output in the EIAJ format. This signal has been processed by the interpolation and muting circuits. This pin has a built-in driver circuit and can directly drive a transformer.

Code	Command	$\overline{RES}$ = low
$42	DOUT ON	○
$43	DOUT OFF	
$40	UBIT ON	○
$41	UBIT OFF	
$88	CDROM-XA	
$8B	ROMXA-RST	○

- The DOUT pin can be locked at the low level by issuing a DOUT OFF command.
- The UBIT information in the DOUT data can be locked at zero by issuing a UBIT OFF command.
- The DOUT data can be switched to data for which interpolation and muting processing have not been performed by issuing a CD-ROM XA command. (At this time, the audio output (the ROMXA pin) enters the mute mode.) While a ROMXA-RST command is used to switch to the audio output for which interpolation and muting have been performed. (At this time, audio output (the ROMXA pin) is released from the mute mode.)

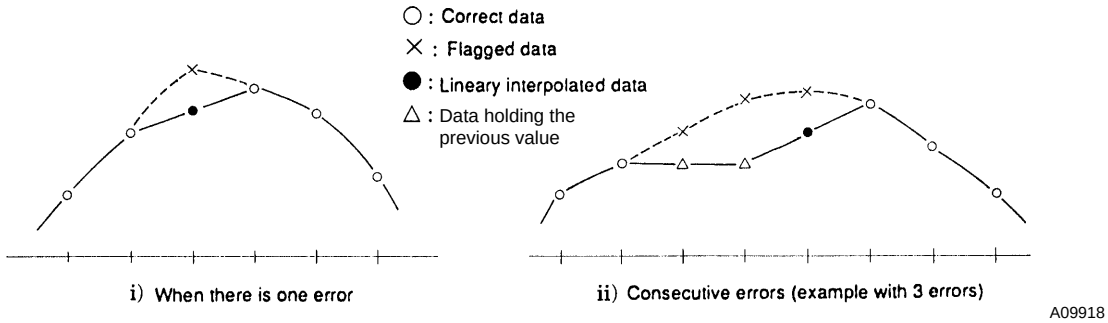
15. Mute Control Circuit

Code	Command	$\overline{RES}$ = low
$01	MUTE: 0 dB	
$03	MUTE: –∞ dB	○

Inputting the above command mutes the audio level (MUTE -∞ dB). Since zero-cross muting is used, there is very little noise associated with this operation. The IC defines zero cross to be the ranges where the upper 7 bits of the data are all zeros or all ones.

16. Interpolation Circuit

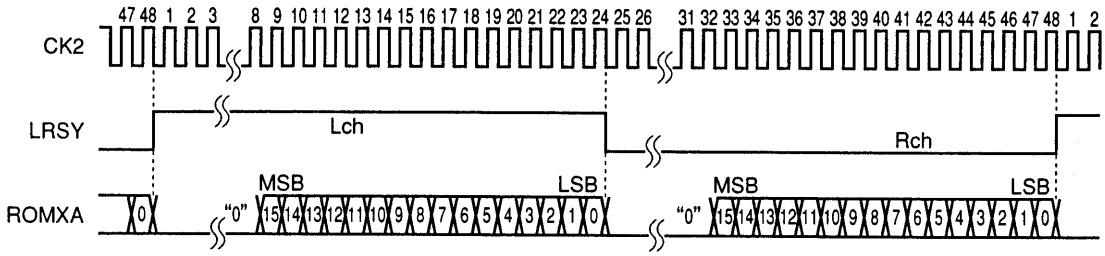
Outputting incorrect audio data that could not be corrected by the error detection and correction circuit would result in loud noises being output. To minimize this noise, the LC78624E replaces the incorrect data with linearly interpolated data based on the correct data on either side of the incorrect data. If one set of C2 flags indicate errors, the above replacement is performed, and if two or more sets of C2 flags indicate errors, the IC holds the previous value. However, when correct data is output following two or more consecutive C2 flags indicating errors, the data point between the correct data and the data output two points previously (the held value) is replaced with a value computed by linearly interpolating those two values.



A09918

17. Audio Data Output; Pin 42: LRSY, Pin 43: CK2, Pin 44: ROMXA

The ROMXA pin provides the interpolated audio data, MSB first, synchronized with the edges of the LRSY signal using the following timing.

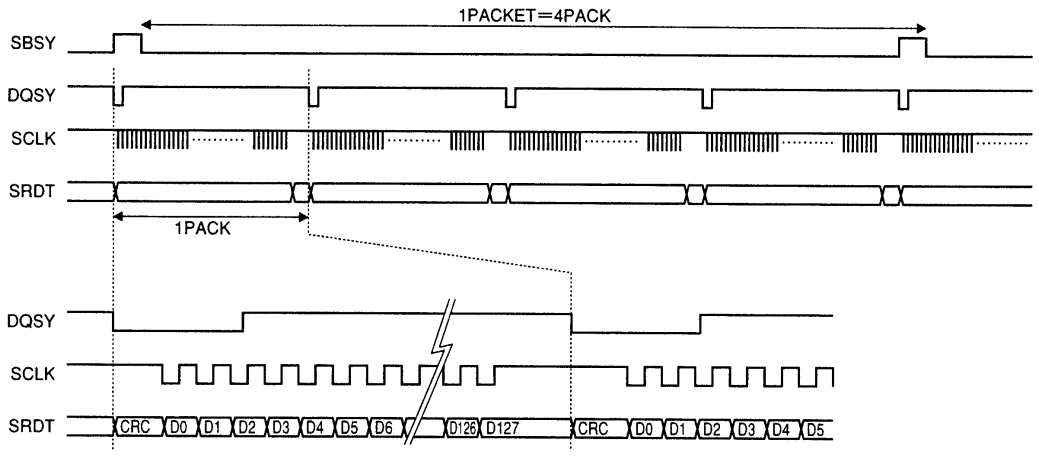


A09919

18. Text Block

The text block decodes the song titles and other text data stored in the Subcode R through W channels of the compact disc's read-in area.

A data pack consists of 24 symbols (24 × 6 = 144 bits) or 18 bytes (18 × 8 = 144 bits). These 18 bytes consist of a 4-byte ID field, 12 bytes of text data, and a 2-byte CRC. The 1-bit result of the CRC check ("H" for OK, "L" of NG) for the pack plus the 16 bytes of ID and text data are available to the microcontroller. The chip indicates the availability of this data with a "L" level pulse (min. 60 μs, max. 150 μs) from the DQSY pin. When the DQSY pin goes to "L" level, the microcontroller reads this data by supplying 128 clock pulses to the SCLK pin. The time limit for reading this data is 3.3 ms for normal playback and 1.5 ms for double-speed playback. The ID bits tell the microcontroller how to interpret the text data that follows.

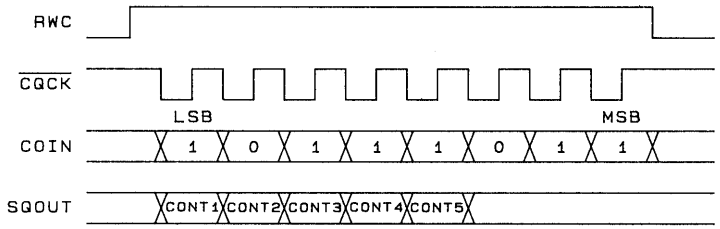


A09920

19. General-Purpose I/O Ports; Pin 24: CONT1, Pin 25: CONT2, Pin 26: CONT3, Pin 27: CONT4, Pin 28: CONT5
The LC78624E provides the five CONT1 to CONT5 I/O ports. These are all set to function as input pins after a reset. Unused port pins should be either connected to ground or set to the output port function.

Code	Command	$\overline{RES}$ = low
$DD	PORT READ	
$DB	PORT I/O SET	PORT I SET
$DC	PORT OUTPUT SET	

Port data is read in by the PORT READ command in synchronization with the falling edge of the $\overline{CQCK}$ by the SQOUT pin in the order CONT1 to CONT5. This command is a single-byte command.



A09921

Additionally, these ports can be set up individually to function as control output pins with the PORT I/O SET command. The ports are selected using the lower 5 bits of the 1Byte data. The bits in the data correspond to CONT1 to CONT5 in order starting with the LSB of the 1Byte data. This command is a Two- byte command. (RWC set once)

1 Byte data + $DB	PORT I/O SET

dn = 1 ··· Sets CONTn to be an output pin
dn = 0 ··· Sets CONTn to be an input pin
n = 0 to 5

Ports set to be output pins can output high or low levels independently. The lower 5 bits of the 1 Byte data correspond to those ports. The bits in the data correspond to CONT1 to CONT5 in order starting with the LSB of the 1 Byte data. This command is a two-byte command. (RWC set once)

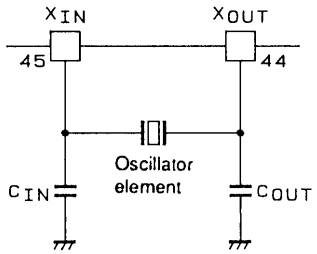
1 Byte data + $DC	PORT OUTPUT SET

dn = 1 ··· Outputs high level signal from the CONTn pin set to output
dn = 0 ··· Outputs low level signal from the CONTn pin set to output

20. Clock Oscillator; Pin 45: X_{IN}, pin 44: X_{OUT}

Code	Command	$\overline{RES}$ = low
$8E	OSC ON	○
$8D	OSC OFF	
$CE	XTAL 16M	○
$C2	NORMAL-SPEED PLAYBACK	○
$C1	DOUBLE-SPEED PLAYBACK	

The clock that is used as the time base is generated by connecting a 16.9344 MHz oscillator element between these pins. The OSC OFF command turns off both the VCO and crystal oscillators. The system microcontroller can issue double-speed or normal-speed playback command to specify the playback speed when the application implements double-speed playback system.
Recommended oscillators
CSA-309 (C = 8 pF) from Citizen Watch
CSA16.93MXZ040 (C = 15 pF) from Toyama Murata Seisakusho
CSA16.93MXW0C3 (with built-in capacitor) from Toyama Murata Seisakusho



A09922

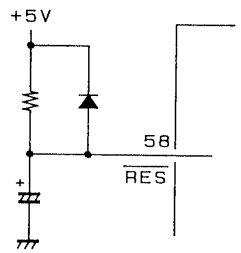
21. 16M and 4.2M Pins; Pin 60: 16M, pin 61: 4.2M
The 16M pin outputs the 16.9344 MHz external crystal oscillator 16.9344 MHz buffer signal. The 4.2M pin supplies the LA9230M, or LA9240M system clock, normally outputting a 4.2336 MHz signal. When the oscillator is turned off both these pins will be fixed at either high or low.

22. Reset Circuit; Pin 58: $\overline{\text{RES}}$

When power is first applied, this pin should be briefly set low and then set high. This will set the muting to –∞ dB and stop the disk motor.

Constant linear velocity servo	START	[STOP]	BRAKE	CLV
Muting control	0 dB	[–∞]		
Q subcode address conditions	[Address 1]	Address free		
Track jump mode	[Standard]	New		
Track count mode	Standard	[New]		
OSC	[ON]	OFF		
Playback speed	[Normal speed]	Double speed		

Setting the $\overline{\text{RES}}$ pin low sets the LC78624E to the settings enclosed in boxes in the table.



A09923

23. Other Pins; Pin 2:TAI, pin 64: TEST1, pin 11: TEST2, pin 32: TEST3, pin 33: TEST4, pin 62: TEST5, pin 59: TST11

These pins are used for testing the LSI's internal circuits. Even though pull-down resistors are built into the TAI and TEST2 to TEST5 input pin circuits, these pins must be connected to 0 V during normal operation. TST11 is an output pin and should normally be left open.

24. Circuit Block Operating Descriptions

- RAM address control

  The LC78624E incorporates an 8-bit × 2k-word RAM on chip. This RAM has an EFM demodulated data jitter handling capacity of ±4 frames implemented using address control. The LC78624E continuously checks the remaining buffer capacity and controls the data write address to fall in the center of the buffer capacity by making fine adjustments to the frequency divisor in the PCK side of the CLV servo circuit. If the ±4 frame buffer capacity is exceeded, the LC78624E forcibly sets the write address to the ±0 position. However, since the errors that occur due to this operation cannot be handled with error flag processing, the IC applies muting to the output for a 128 frame period.

Position	Division ratio or processing	
–4 or less	Force to ±0	
–3	589	Increase ratio
–2	589	
–1	589	
±0	588	Standard ratio
+1	587	Decrease ratio
+2	587	
+3	587	
+4 or more	Force to ±0	

- C1 and C2 Error Correction

  The LC78624E writes EFM demodulated data to internal RAM to compensate for jitter and then performs the following processing with uniform timing based on the crystal oscillator clock. First, the LC78624E performs C1 error checking and correction in the C1 block, determines the C1 flags, and writes data to the C1 flag register. Next, the LC78624E performs C2 error checking and correction in the C2 block, determines the C2 flags, and writes data to internal RAM.

C1 flag	Error correction and flag processing
No errors	No correction required · Flag reset
1 error	Correction · Flag reset
2 errors	Correction · Flag set
3 errors or more	Correction not possible · Flag set

C2 flag	Error correction and flag processing
No errors	No correction required · Flag reset
1 error	Correction · Flag reset
2 errors	Depends on C1 flags*1
3 errors or more	Depends on C1 flags*2

Note: 1. If the positions of the errors determined by the C2 check agree with the C1 flags, the correction is performed and the flags are cleared. However, if the number of C1 flags is 7 or higher, C2 correction may fail. In this case correction is not performed and the C1 flags are taken as the C2 flags without change. Error correction is not possible if one error position agrees and the other does not. Furthermore, if the number of C1 flags is 5 or under, the C1 check result can be seen as unreliable. Accordingly, the flags will be set in this case. Cases where the number of C1 flags is 6 or more are handled in the same way, and the C1 flags are taken as the C2 flags without change. When there is not even one agreement between the error positions, error correction is, of course, impossible. Here, if the number of C1 flags was 2 or under, data that was seen as correct after C1 correction is now seen as incorrect data. The flags are set in this case. In other cases, the C1 flags are taken as the C2 flags without change.

2. When data is determined to have three or more errors and be uncorrectable, correction is, of course, impossible. Here, if the number of C1 flags was 2 or under, data that was seen as correct after C1 correction is now seen as incorrect data. The flags are set in this case. In other cases the C1 flags are taken as the C2 flags without change

25. Command Summary Table

Blank entry: Illegal command, #: Changed or added command, *: Latching commands (mode setting commands), ○: Commands shared with an ASP (LA9220M/30M/31M or other processor), Items in parentheses are ASP commands (provided for reference purposes)

$00	(ADJ.reset)	$20	* TOFF low in TJ mode	$40	* UBIT ON	$60	
$01	* MUTE 0 dB	$21	* TOFF high in TJ mode	$41	* UBIT OFF	$61	
$02	#	$22	* New TRACK COUNT	$42	* DOUT ON	$62	
$03	* MUTE –∞ dB	$23	* Old TRACK COUNT	$43	* DOUT OFF	$63	
$04	* DISC MTR START	$24		$44		$64	
$05	* DISC MTR CLV	$25		$45		$65	
$06	* DISC MTR BRAKE	$26		$46		$66	
$07	* DISC MTR STOP	$27		$47		$67	
$08	○ FOCUS START #1	$28	* STO CONT	$48		$68	
$09	* ADDRESS FREE	$29	* LCH CONT	$49		$69	
$0A	#	$2A	* RCH CONT	$4A		$6A	
$0B		$2B	#	$4B		$6B	#
$0C		$2C	#	$4C		$6C	#
$0D		$2D	#	$4D		$6D	
$0E	#	$2E	#	$4E	SW1P OFF	$6E	#
$0F	* TRACKING OFF	$2F		$4F	SW1P ON	$6F	#
$10	2TJ IN	$30	32TJ IN	$50		$70	
$11	1TJ IN #1	$31	1TJ IN #3	$51		$71	
$12	1TJ IN #2	$32		$52	1TJ IN #4	$72	
$13	4TJ IN	$33		$53		$73	
$14	16TJ IN	$34		$54		$74	
$15	64TJ IN	$35		$55		$75	
$16	256TC	$36		$56		$76	
$17	128TJ IN	$37		$57		$77	
$18	2TJ OUT	$38	32TJ OUT	$58		$78	
$19	1TJ OUT #1	$39	1TJ OUT #3	$59		$79	
$1A	1TJ OUT #2	$3A		$5A	1TJ OUT #4	$7A	
$1B	4TJ OUT	$3B		$5B		$7B	
$1C	16TJ OUT	$3C		$5C		$7C	
$1D	64TJ OUT	$3D		$5D		$7D	
$1E		$3E		$5E		$7E	
$1F	128TJ OUT	$3F		$5F		$7F	

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Blank entry: Illegal command, #: Changed or added command, *: Latching commands (mode setting commands), ○: Commands shared with an ASP (LA9220M/30M/31M or other processor), Items in parentheses are ASP commands (provided for reference purposes)

$80		$A0	* Old TRK JMP	$C0		$E0	
$81		$A1	* New TRK JMP	$C1	* Double-speed playback	$E1	
$82		$A2	FOCUS START #2	$C2	* Normal-speed playback	$E2	
$83		$A3	* Internal BRAKE CONT	$C3		$E3	
$84		$A4		$C4	* Internal BRK OFF	$E4	
$85		$A5		$C5	* Internal BRK ON	$E5	
$86		$A6		$C6		$E6	
$87		$A7		$C7		$E7	
$88	* #CDROMXA	$A8	* DISC 8 SET	$C8	#	$E8	
$89	* ADDRESS 1	$A9	* DISC 12 SET	$C9	#	$E9	
$8A	#	$AA		$CA	* Internal BRK-DMC low	$EA	
$8B	* #ROMXA RST	$AB		$CB	* Internal BRK-DMC high	$EB	
$8C	TRACK JMP BRK	$AC	#VCO X2 SET	$CC	* TOFF during internal BRAKE	$EC	
$8D	* OSC OFF	$AD	#VCO X1 SET	$CD	* TON during internal BRAKE	$ED	
$8E	* OSC ON	$AE		$CE	* Xtal 16M	$EE	* Command noise rejecter OFF
$8F	* TRACKING ON	$AF		$CF		$EF	* Command noise rejecter ON
$90	(* F.OFF.ADJ.ST)	$B0	* CLV-PH 1/1 mode	$D0		$F0	* ○ TRCK CHECK IN (2BYTE DETECT)
$91	(* F.OFF.ADJ.OFF)	$B1	* CLV-PH 1/2 mode	$D1		$F1	
$92	(* T.OFF.ADJ.ST)	$B2	* CLV-PH 1/4 mode	$D2		$F2	
$93	(* T.OFF.ADJ.OFF)	$B3	* CLV-PH 1/8 mode	$D3		$F3	
$94	(* LSR.ON)	$B4	* CLV3ST output ON	$D4		$F4	
$95	(* LSR.OF/F.SV.ON)	$B5	* CLV3ST output OFF	$D5		$F5	
$96	(* LSR.OF/F.SV.OF)	$B6	* JP3ST output ON	$D6		$F6	
$97	(* SP.8CM)	$B7	* JP3ST output OFF	$D7		$F7	
$98	(* SP.12CM)	$B8		$D8		$F8	* ○ TRCK CHECK OUT (2BYTE DETECT)
$99	(* SP.OFF)	$B9		$D9		$F9	
$9A	(* SLED.ON)	$BA		$DA		$FA	
$9B	(* SLED.OFF)	$BB		$DB	#PORT I/O SET	$FB	
$9C	(* EF.BAL.START)	$BC		$DC	#PORT OUTPUT SET	$FC	
$9D	(* T.SERVO.OFF)	$BD		$DD	#PORT READ	$FD	
$9E	(* T.SERVO.ON)	$BE		$DE		$FE	○ NOTHING
$9F		$BF		$DF		$FF	* ○ 2BYTE CMD RST

Note: VCO × 2 SET command should be issued in case of low voltage power supply application.

27. CD-DSP Functional Comparison

Function \ Product		LC7861NE→ LC7861KE	LC78621E	LC78622E	LC78624E	LC78625E	LC78626E	LC78630E
EFM-PLL		When paired with an analog ASP	Built-in VCO FR = 1.2 kΩ	Built-in VCO FR = 1.2 kΩ	Built-in VCO FR = 1.2 kΩ	Built-in VCO FR = 1.2 kΩ	Built-in VCO FR = 5.1 kΩ	Built-in VCO FR = 1.2 kΩ
RAM		16 K	16 K	16 K	16 K	16 K	16 K	18 K
Speed		2×/4×	2×	2×	2×	2×	2×	4×
Digital output		○	○	○	○	○	○	○
Interpolation		4	4	2	2	4	2	2
Zero-cross muting		○ –12 dB, –∞	○ –12 dB, –∞	○ –∞	○ –∞	○ –12 dB, –∞	○ –∞	○ –∞
Level meter peak search		×	○	×	×	○	×	×
Bilingual		×	○	○	○	○	○	○
Digital attenuator		×	○	○	×	○	○	○
Digital filters		2fs	8fs	4fs	×	8fs	4fs	2fs
Digital de-emphasis		×	○	○	×	○	○	○
General-purpose port	Output	2	2	×	×	2	×	2
	Input/ output	×	×	5	5	(4)	1 + (3)	2 + (4)
VCD support		×	×	×	×	○	×	○
Antishock interface		×	○	×	×	○	No need	○
Antishock controller		×	×	×	×	×	○	×
CD text support		×	×	×	○	×	×	×
CD-ROM interface		○	○	×	×	○	×	○
1 bit D/A converter		×	○	○	×	○	○	○
Lowpass filter		×	×	○	×	×	○	×
Power supply voltage		4.5 to 5.5 V	3.6 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	3.0 to 5.5 V	3.6 to 5.5 V
Package		QFP64E	QFP80E	QFP64E	QFP64E	QFP80E	QFP100E	QFP80E