Ordering number:ENN1374E

CMOS IC

LC7533

3V Electronic Volume Control

Use

•Attenuation of signal.

Features

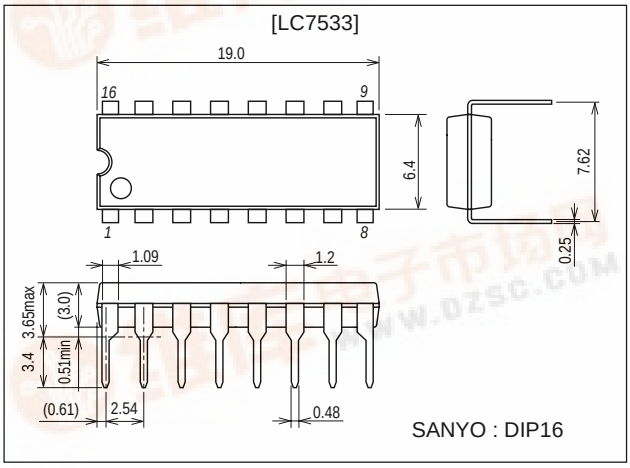
- CMOS process 3V typ. operation.
- Up/down operation is performed with SW input.
- 4-bit, 16-step counter. Step 6* is set with initial input($\overline{\text{INIT}}$).
- Center tap provided.
- Maximum attenuation : –60dB or less.
- Attenuation curve : Pseudo curve A. Left/right simultaneous setting.

*: Step 6 means mode 6.

Package Dimensions

(unit:mm)

3006C-DIP16



Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{SS} to 6	V
Supply voltage	V_I		V_{SS} to V_{DD}	V
Allowable power dissipation	Pd max		100	mW
Operating temperature	Topr		–30 to +75	˚C
Storage temperature	Tstg		–40 to +125	˚C

Allowable Operating Conditions at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		2.1 to 5.0	V
Input high-level voltage	V_{IH1}	$\overline{\text{INIT}}$, CE pin	0.7V_{DD} to V_{DD}	V
	V_{IH2}	$\overline{\text{UP}}$, $\overline{\text{DN}}$, CR pin	0.9V_{DD} to V_{DD}	V
Input low-level voltage	V_{IL1}	$\overline{\text{INIT}}$, CE	0 to 0.3V_{DD}	V
	V_{IL2}	$\overline{\text{UP}}$, $\overline{\text{DN}}$, CR	V_{SS} to 0.1V_{DD}	V

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

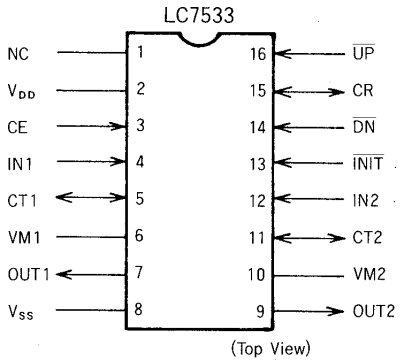
Electrical Characteristics at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Signal distortion	THD_1	V_{DD}=3V, R_L=50kΩ, f=1kHz			0.5	%
	THD_2	V_{DD}=2.1V, R_L=50kΩ, f=1kHz		1		%
Output at attenuation mode	X_{OUT}	0dBm input, 1kHz, 51kΩ load			–60	dB
Signal transmit delay time	td	Between IN and OUT, no load		1		µs
Input impedance	r_i	$\overline{UP}$, $\overline{DN}$, CE only	100		400	kΩ
Output noise voltage	V_{NO}	V_{DD}=3V, R_L=50kΩ, STEP“ 0”			8	µV
Input high-level current	I_{IH}	CE pin, V_{DD}=3V, V_I=3V			40	µA
Input low-level current	I_{IL}	$\overline{UP}$, $\overline{DN}$ pin, V_{DD}=3V, V_I=0V	–55			µA
Attenuation balance	ΔV	Pins OUT1, 2, other than STEP“ 0” (Note1)	–2	0	+2	dB
Channel balance	ΔV_O	Between pins OUT1, 2, other than STEP“ 0” (Note2)	–2		+2	dB
Current drain	I_{DD}	V_{DD}=3V, CE=V_{DD}, $\overline{INIT}$=V_{DD}, other pins:OPEN			1	mA
	I_{DD} BACK UP	V_{DD}=3V, CE=V_{SS}, $\overline{INIT}$=V_{DD}, other pins:OPEN			1	µA
Crosstalk between channels	CT	V_{DD}=1.5V, V_{SS}=–1.5V, V_M=0V, f=1kΩ, 1Vrms input, test side input : 1kΩ short		85		dB
Minimum pulse width	$T_{UP/DN}$	T=(CR oscillation cycle) $\overline{UP}$, $\overline{DN}$ pin		1.5T		ms
	T_{INIT}	$\overline{INIT}$ pin	2			µs

Note 1 (1) $\Delta V=20\log 10\ V_{OUT}/V_{TYP}$
V_{OUT} : OUT1(OUT2) output level
V_{TYP} : Standard output level
(2) Satisfy V_{OUT}(STEP N) < V_{OUT} (STEP N + 1)

Note 2 (1) $\Delta V_O=20\log 10\ V_{OUT1}/V_{OUT2}$

Pin Assignment



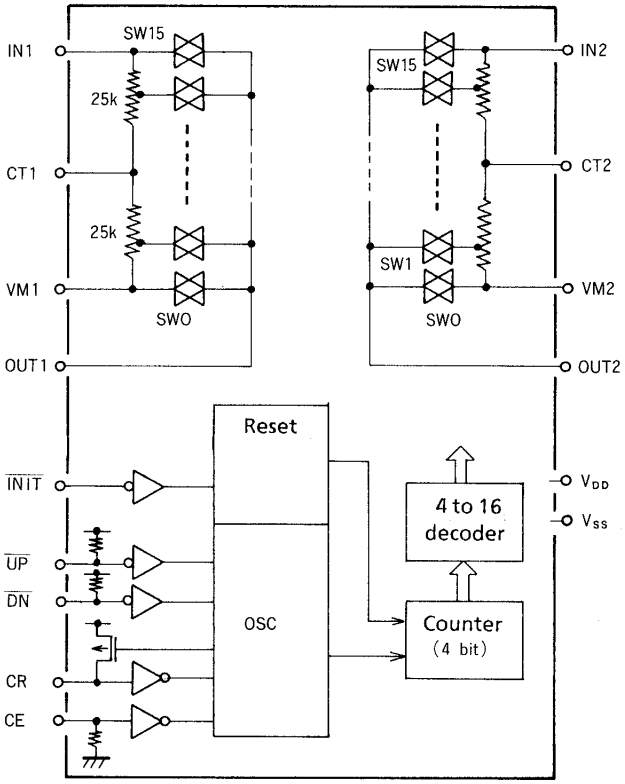
Note 1 : No bonding exists on the inside of NC pin. It is recommended that the outside should be shorted to V_{DD}, V_{SS}, etc. on the printed circuti board.

Pin Description

Pin Name	Pin Number	Description
IN1, IN2	4, 12	Input pin for volume control
OUT1, OUT2	7, 9	Output pin for volume control
V_{M1}, V_{M2}	6, 10	Bias pin. When operated from single supply, 1/2V_{DD} is applied to this pin.
C_{T1}, C_{T2}	5, 11	Tap pin provided at the center of volume control. By connecting C and R to this pin, the loudness can be controlled.
CE	3	When this pin is set to “ L” , the current drain is reduced. This pin must be “ L” at backup mode.
$\overline{INIT}$	13	Initial pin. When set to “ L” , the 6th step is reached.
$\overline{UP}$	16	When the level on this pin is made to fall, the step rises and the volume goes up. When held at “ L” , the volume goes up; if set to “ H” , the volume stops going up at a step reached at that moment. The step stops at the MSB position.
$\overline{DN}$	14	The $\overline{DN}$ operation is the reverse of $\overline{UP}$. when the $\overline{UP}$, $\overline{DN}$ are set to “ L” at the same time, the $\overline{UP}$ is given priority.The step stops at the LSB position.
CR	15	Pin for connecting R, C on which the rate of step depends.
V_{DD}	2	Power supply pin (+)
V_{SS}	8	Ground
NC	1	No bonding exists on the inside of NC pin. Connected to V_{DD} or V_{SS} is recommended.

Equivalent Circuit Block Diagram

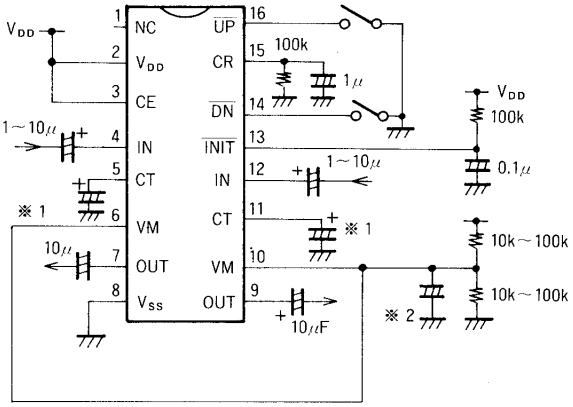
[Common to LC7533]



Note 1 : The TEST pin is bonded only when the MFP20 is used.

Sample Application Circuit

[LC7533 DIP16]



For V_M, $1/2V_{DD}$ bias is recommended.

※1 For low-band boost (appro. 1μF)

※2 The larger the capacity is (appro. 100μF), the better the characteristics of attenuation and closstalk.

Unit (resistance: Ω, capacitance: F)