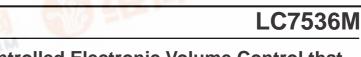
Ordering number : EN6089

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CMOS IC



Serially Controlled Electronic Volume Control that Handles High Voltages

CCB

Overview

The LC7536M is an electronic volume control that implements volume, balance, and loudness functions with a minimum number of external components, and can be controlled electronically with serial data.

Functions

- Volume: 81 positions from 0 to −79 dB (in 1-dB steps) and −∞. Since the left and right channels can be controlled separately, a balance function can be implemented easily.
- Loudness: A tap is output from the -20 dB position of a 5 dB step volume control resistor ladder. A loudness function can be implemented by connecting an external RC circuit.
- S (select): Up to two LC7536M ICs can be used on the same bus.
- Serial data input: The LC7536M supports control and communication in the CCB format.

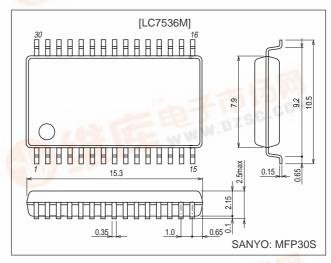
Features

• High voltage handling capability: ±16 V.

Package Dimensions

unit: mm

3216A-MFP30S



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- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.
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Specifications Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
	V _{DD} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V _{SS} to V _{SS} + 18	V
Maximum supply voltage	V _{EE} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V_{SS} – 18 to V_{SS}	V
	V _{CC} max	$V_{EE} \le V_{SS} < V_{CC} < V_{DD}$	V _{SS} to V _{SS} + 7	V
Maximum input voltage	V _{IN} max1	CL, DI, CE	0 to V _{CC} + 0.3	V
	V _{IN} max2	L5dBIN, R5dBIN, L1dBIN, R1dBIN	V _{EE} – 0.3 to V _{DD} + 0.3	V
	V _{IN} max3	S	V _{CC} – 0.3 to V _{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	250	mW
Operating temperature	Topr		-30 to +75	°C
Storage temperature	Tstg		-40 to +125	°C

Allowable Operating Ranges at Ta=-30 to $+75^{\circ}C,\,V_{SS}$ = 0 V

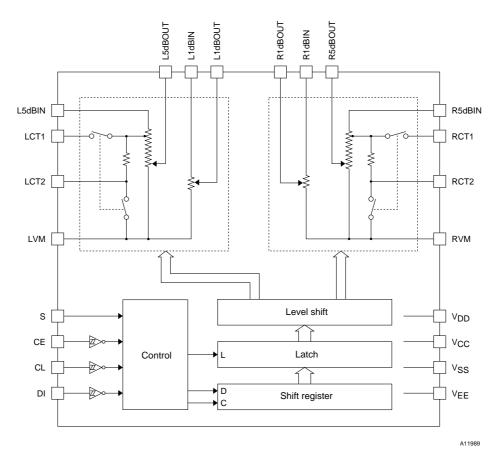
Parameter	Cumhal	Conditions	Ratings				
Parameter	Symbol	Conditions	min	typ	max	Unit	
	V _{DD}	V _{DD}	V _{CC} + 4.5		16	V	
Supply voltage	V _{EE}	V _{EE}	-16		0	V	
	V _{CC}	V _{CC}	4.5	5	5.5	V	
	V _{IH} 1	CL, DI, CE	0.8 V _{CC}		V _{CC}	V	
High-level input voltage	V _{IH} 2	S	$0.8 \times (V_{DD} - V_{CC}) + V_{CC}$		V _{DD}	V	
Low-level input voltage	V _{IL} 1	CL, DI, CE	V _{SS}		0.2 V _{CC}	V	
	V _{IL} 2	S	V _{CC}		$0.2 \times (V_{DD} - V_{CC}) + V_{CC}$	V	
Input voltage amplitude	V _{IN}	L5dBIN, R5dBIN, L1dBIN, R1dBIN	V _{EE}		V _{DD}	Vp-p	
Input pulse width	tøW	CL	1			μs	
Setup time	t _{setup}	CL, DI, CE	1			μs	
Hold time	t _{hold}	CL, DI, CE	1			μs	
Operating frequency	fopg	CL			500	kHz	

Electrical Characteristics at $Ta=25^{\circ}C,\,V_{SS}=0$ V

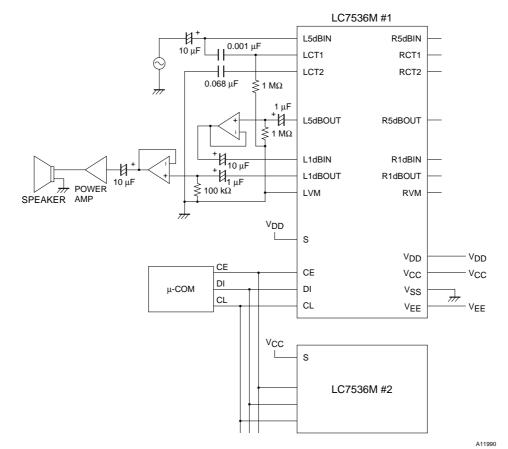
Parameter	Symbol	Conditions	Ratings			Unit
Falameter	Symbol	Conditions	min	typ	max	
Total harmonic distortion	THD1	V_{IN} = 1 Vrms, f = 1 kHz, all controls flat overall, $V_{DD}-V_{EE}$ = 32 V		0.004		%
	THD2	V_{IN} = 0.1 Vrms, f = 1 kHz, all controls flat overall, $V_{DD}-V_{EE}$ = 32 V		0.02		%
Crosstalk	CT	$V_{\text{IN}} = 1 \text{ Vrms}, \text{ f} = 1 \text{ kHz}, \text{ V}_{\text{DD}} - \text{V}_{\text{EE}} = 32 \text{ V},$ All controls flat overall, Rg = 1 kΩ		-75	-60	dB
Output at maximum attenuation	Vo min	V_{IN} = 1 V rms, f = 20 kHz, volume control set at –∞, $V_{DD} - V_{EE}$ = 32 V		-98		dB
Output noise voltage	V _N	All controls flat overall, Rg = 1 kΩ, IHF–A, $V_{DD} - V_{EE} = 32$ V		2	10	μV
Tatal as sisters as	Rvol1	The 5-dB step volume block		75		kΩ
Total resistance	Rvol2	The 1-dB step volume block		20		kΩ
Output off leakage current	I _{OFF}	L5dBIN, R5dBIN, LCT1, RCT1, LCT2, RCT2, L5dBOUT, R5dBOUT, L1dBIN, R1dBIN, L1dBOUT, R1dBOUT, LVM, RVM	-10		+10	μΑ
High-level input current	IIH	CL, DI, CE, $V_{IN} = V_{CC}$			+10	μA
Low-level input current	IIL	CL, DI, CE, V _{IN} = V _{SS}	-10			μA
Current drain	I _{DD}	V _{DD} = 16 V			1	mA
	I _{CC}	V _{DD} = 5.5 V			1	mA



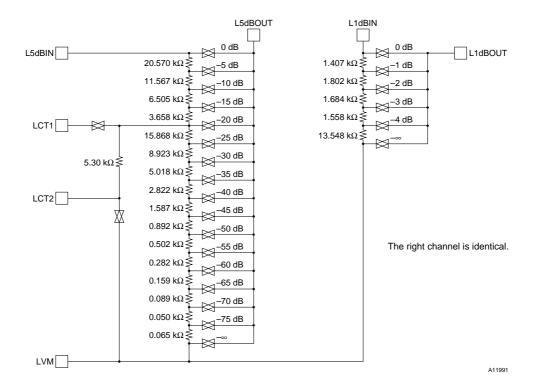
Equivalent Circuit



Sample Application Circuit

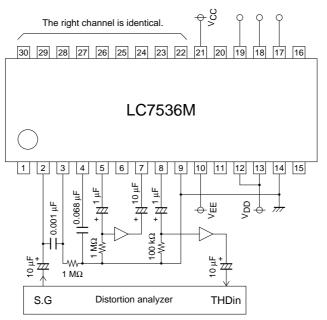


Internal Resistor Equivalent Circuit

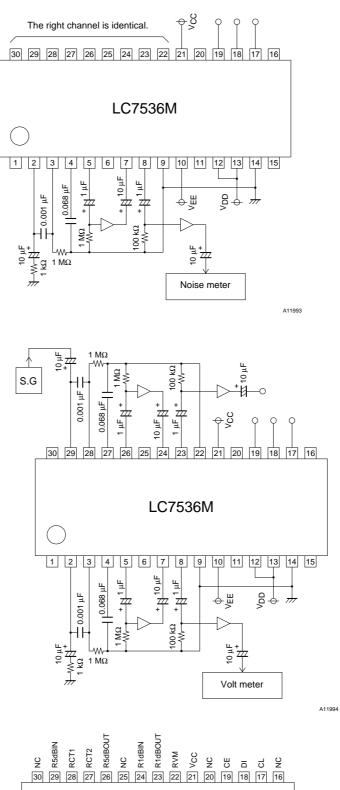


Test Circuit

• Total harmonic distortion

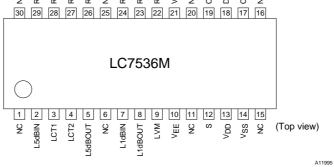


• Output noise voltage



Crosstalk



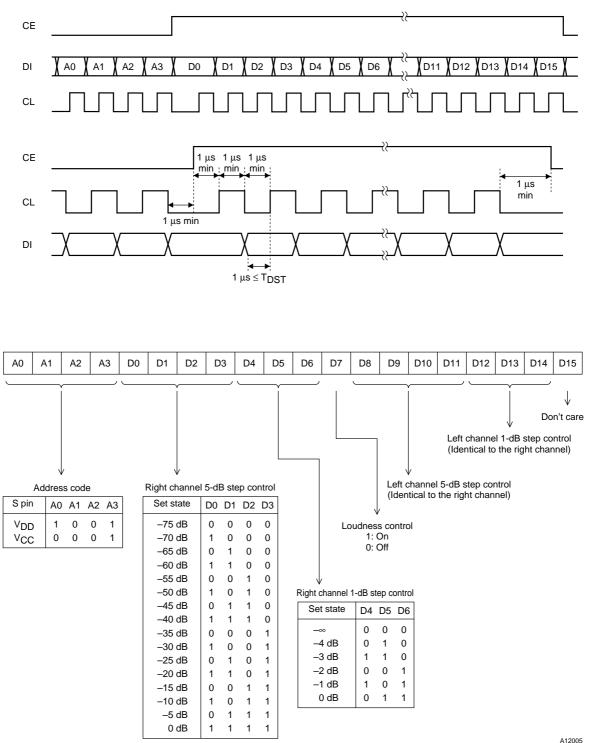


Pin Functions

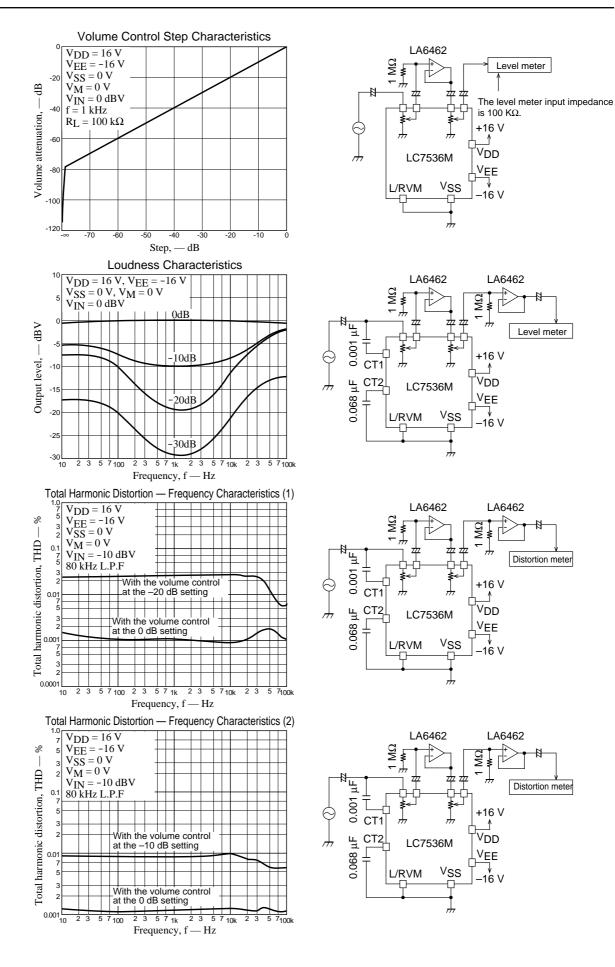
Pin No.	Pin	Function	Equivalent circuit
2	L5dBIN		° ∧DD
2	LOUDIN	5-dB step attenuator inputs	
		These inputs must be driven by low-impedance circuits.	
29	R5dBIN		
			A11996
3	LCT1		
-	-		
28	RCT1	Loudness circuit connections	CT2 7
		Connect high-band compensation capacitors between the CT1 and 5dBIN pins, and connect low-band compensation	° V _{DD}
4	LCT2	capacitors between the CT2 and VM pins.	
27	RCT2		
21	NO12		CT1 • K + 777 A11998
			° V _{DD}
5	L5dBOUT	5-dB step attenuator outputs	▲
		These signals should be received by loads of about 47 k Ω	
26	R5dBOUT	to 1 MΩ.	卒 卒 🏛
			A11999
7	L1dBIN		° V _{DD}
'	LIUDIN	1-dB step attenuator inputs	
		These inputs must be driven by low-impedance circuits.	
24	R1dBIN		
			A12000
8	L1dBOUT	1-dB step attenuator outputs	<u>↓</u> VDD
		These signals should be received by loads of about 47 k Ω	
22		to 1 M Ω .	🗴 🗴 🏂
23	R1dBOUT		A12001
		Common pins for the volume controls. The printed circuit	
		board pattern for these pins should be designed to have as	5dBIN
9	LVM	low an impedance as possible. Since LVM, RVM, and V _{SS} are not connected internally in the IC, they may be	~~
		connected to separate external circuits that meet their	
		individual specifications.	
		Since the capacitors between the VM pins and the power supply when a single power supply is used become the	× 777 ℃M (V)
22	RVM	residual resistance components at maximum attenuation,	
		care is required in determining the values of these	A12002
		capacitors.	
			↓ V _{DD}
		• Selects the address code of data during formatted.	
12	S	When this pin is connected to V_{DD} , the IC accepts data when the address code is 9, and when connected to V_{CC} ,	
		it accepts data when the address code is 8.	
			7 77 A12003
			A12000
17	CL		γVDD
18	DI	• Inputs for the serial data that controls the IC. The input	
-		signals must have an amplitude of 0 to 5 V.	
10			777
19	CE		A12004
10	V _{EE}		
13	V _{DD}	Power supply connections. These pins must be connected to the corresponding power supply. Applications must be	
14	V _{SS}	designed so that V_{CC} is not applied before V_{DD} .	
21	V _{CC}		
1, 6, 11,			
15, 16,	NC	Unused pins. These pins must be left open.	
20, 25, 30			
50			

Control System Timing and Data Format

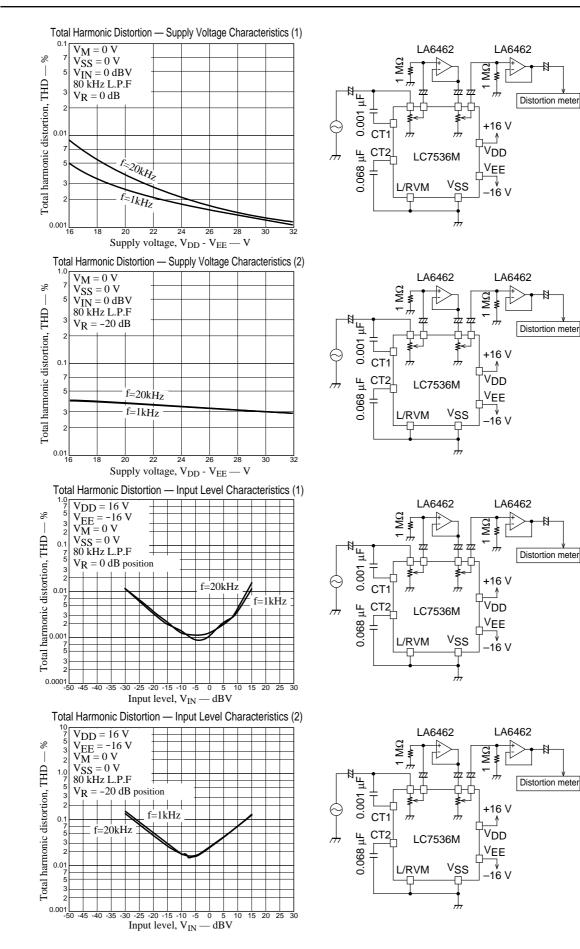
To control the LC7536M, apply the stipulated data signals to the CL, DI, and CE pins. The data consists of 20 bits, of which 4 bits are the address and 16 bits are the data.



LC7536M



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Usage Notes

- The states of the internal analog switches are undefined when power is first applied. Applications should apply muting to the analog signal system externally until control data has been transferred to the IC.
- To prevent noise from the high-frequency digital signals on the CL, DI, and CE pin lines from entering the analog signal system, either shielded lines should be used for these lines, or they should be covered by the ground pattern.

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