CMOS LSI

SANYO

No. ※4278

LC89560

Error Correction and ADPCM Decoder for CD-I and CD-ROM XA Applications

Preliminary

OVERVIEW

The LC89560 is an error-correction and ADPCM decoder for CD-I and CD-ROM applications. It combines the functionality of the earlier LC8951 and LC8955 devices into one chip. It also includes on-board erasure correction RAM, and support for connection to 64 to 512 Kbits of external RAM. (The ADPCM decoder function is not supported with 64 Kbits of external RAM option.)

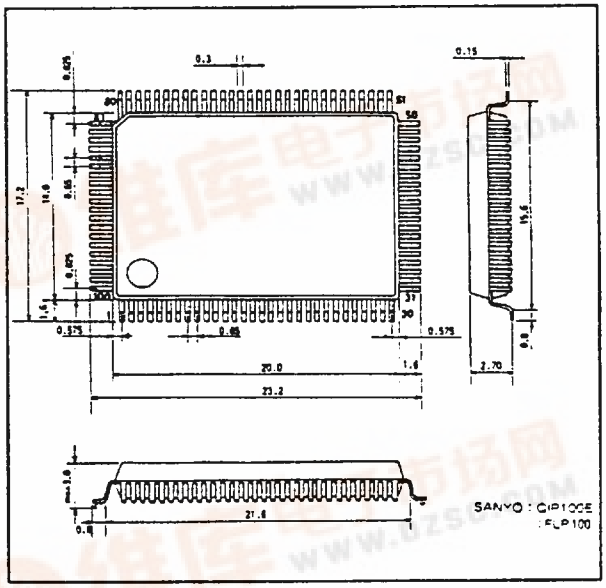
FEATURES

- Support for CD-ROM (Mode 1), CD-I and CD-ROM XA (Mode 2, Forms 1 and 2)
- Incorporates circuitry required for CD-I and CD-ROM onto a single chip
- Error-detection and correction implemented in hardware
- Real-time error correction that does not require communications over a host interface bus
- High transfer rate of up to 2.3 Mbytes/s (18.4 Mbits/s)
- Multiple block buffering allows operation even with slow hosts
- Erasure correction gives twice the error-correction capability
- Command status FIFO on the host interface
- Status FIFO on the host interface
- ADPCM decoder circuits on-chip
- Sub-code interface on-chip
- External SRAM can be accessed directly from a SUB-CPU
- On-chip 8 Kbit RAM for erasure correction
- CMOS process, single 5 V supply
- 100-pin flat package (SQFP100, QIP100E)

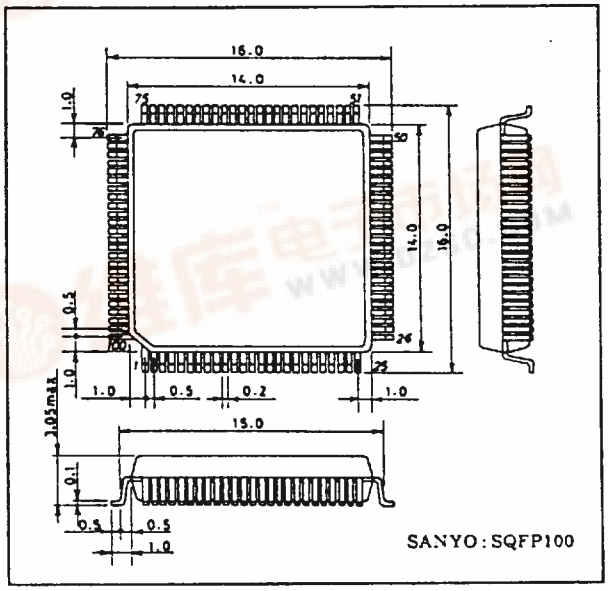
PACKAGE DIMENSIONS

Unit: mm

3151-QFP100E

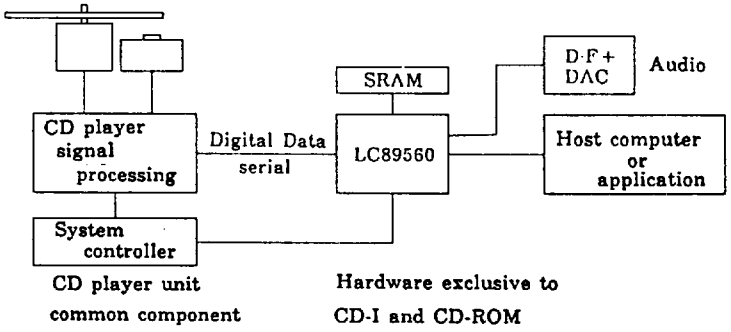


3181-SQFP100

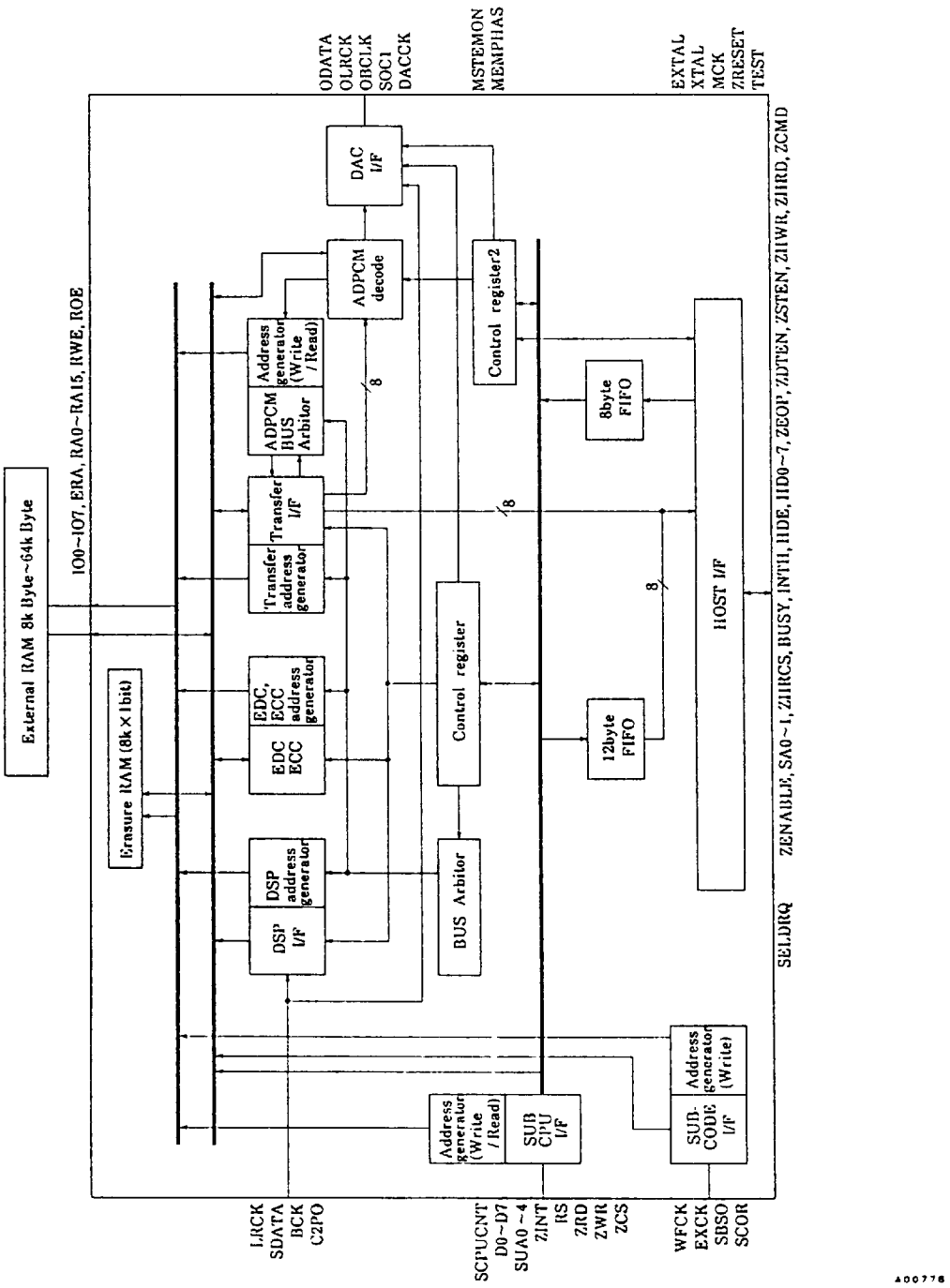


Specifications and information herein are subject to change without notice.

CD-I/CD-ROM SYSTEM BLOCK DIAGRAM



BLOCK DIAGRAM



PIN DESCRIPTION (QIP100E)

The letter 'Z' as the first character of a name indicates negative logic.

Number	Name	I/O	Description
1	SA0	I	Host register select
2	ZAPCS	I	Host register chip select
3	BUSY	O	Busy signal. This signal is active when the host writes ADPCM data.
4	INTH	O	Interrupt to host
5	HDE	O	Erasure flag output. This pin has an internal pull-up resistor.
6	HD7	I/O	Host interface data. These pins have internal pull-up resistors.
7	HD6	I/O	
8	HD5	I/O	
9	HD4	I/O	
10	HD3	I/O	
11	HD2	I/O	
12	HD1	I/O	
13	HD0	I/O	
14	Vss	–	Ground
15	ZEOP	O	End-of-process signal. This signal is used during DMA data transfer.
16	MSTEMON	O	Audio block monitor pin
17	MEMPHAS	O	
18	OLRCK	O	D/A converter outputs
19	ODATA	O	
20	OBCLK	O	
21	SOC1	O	Output pin for LC7883K
22	DACCK	O	Clock output. 16.9344 MHz for levels A and B, 8.4672 MHz for level C.
23	Vss	–	Ground
24	RA0	O	RAM address lines
25	RA1	O	
26	RA2	O	
27	RA3	O	
28	RA4	O	
29	RA5	O	
30	RA6	O	
31	RA7	O	
32	RA8	O	
33	RA9	O	
34	RA10	O	
35	RA11	O	
36	RA12	O	

Number	Name	I/O	Description
37	RA13	O	RAM address lines
38	RA14	O	
39	RA15	O	
40	V_{SS}	–	Ground
41	V_{DD}	–	5 V supply
42	ZRWE	O	RAM write pin
43	ZROE	O	RAM read pin
44	ERA	I/O	Erasure flag RAM data input/output
45	IO0	I/O	Data buffer RAM input/output. These pins have internal pull-up resistors.
46	IO1	I/O	
47	IO2	I/O	
48	IO3	I/O	
49	IO4	I/O	
50	IO5	I/O	
51	IO6	I/O	
52	IO7	I/O	
53	V_{SS}	–	Ground
54	EXTAL	I	Crystal oscillator
55	XTAL	O	
56	TEST	I	Test pin. Connect to V_{SS}.
57	V_{SS}	–	Ground
58	MCK	O	Connections to CD-DSP
59	LRCK	I	
60	SDATA	I	
61	BCK	I	
62	C2PO	I	
63	WFCK	I	Sub-code inputs and outputs
64	EXCK	O	
65	SBSO	I	
66	SCOR	I	
67	CEMPHAS	O	Connect to CD-DSP emphasis pin.
68	ZRESET	I	Reset pin. Hold LOW for 1 µs.
69	SCPUCNT	I	SUB-PCU interface select
70	D0	I/O	SUB-CPU data signal pins. These pins have internal pull-up resistors.
71	D1	I/O	
72	D2	I/O	
73	D3	I/O	
74	D4	I/O	

Number	Name	I/O	Description
75	D5	I/O	SUB-CPU data signal pins. These pins have internal pull-up resistors.
76	D6	I/O	
77	D7	I/O	
78	V_{SS}	–	Ground
79	SUA0	I	SUB-CPU register select address
80	SUA1	I	
81	SUA2	I	
82	SUA3	I	
83	SUA4	I	
84	NC	–	No connection
85	ZINT	O	SUB-CPU interrupt signal. This is an open-drain output, with an internal pull-up resistor.
86	RS (ALE)	I	Internal register set pin
87	ZRD	I	SUB-CPU read signal
88	ZWR	I	SUB-CPU write signal
89	V_{DD}	–	5 V supply
90	V_{SS}	–	Ground
91	ZCS	O	SUB-CPU chip select signal
92	ZENABLE	I	Chip select from host
93	SELDRQ	I	DRQ/WAIT select
94	ZWAIT/DRQ	O	DRQ/ZWAIT output
95	ZDTEN	O	Data enable
96	ZSTEN	O	Status enable
97	ZHWR	I	Host data write signal
98	ZHRD	I	Host data read signal
99	ZCMD	I	Host data/command signal select
100	SA1	I	Audio block register select

PIN DESCRIPTION (SQFP100)

The letter 'Z' as the first character of a name indicates negative logic.

Number	Name	I/O	Description
1	INTH	O	Interrupt to host
2	HDE	O	Erasure flag output. This pin has an internal pull-up resistor.
3	HD7	I/O	Host interface data. These pins have internal pull-up resistors.
4	HD6	I/O	
5	HD5	I/O	
6	HD4	I/O	
7	HD3	I/O	
8	HD2	I/O	

Number	Name	I/O	Description
9	HD1	I/O	Host interface data. These pins have internal pull-up resistors.
10	HD0	I/O	
11	V_{SS}	–	Ground
12	ZEOP	O	End-of-process signal. This signal is used during DMA data transfer.
13	MSTEMON	O	Audio block monitor pin
14	MEMPHAS	O	
15	OLRCK	O	D/A converter outputs
16	ODATA	O	
17	OBCLK	O	
18	SOCI	O	Output pin for LC7883K
19	DACCK	O	Clock output. 16.9344 MHz for levels A and B, 8.4672 MHz for level C.
20	V_{SS}	–	Ground
21	RA0	O	RAM address lines
22	RA1	O	
23	RA2	O	
24	RA3	O	
25	RA4	O	
26	RA5	O	
27	RA6	O	
28	RA7	O	
29	RA8	O	
30	RA9	O	
31	RA10	O	
32	RA11	O	
33	RA12	O	
34	RA13	O	
35	RA14	O	
36	RA15	O	
37	ZRWE	O	RAM write pin
38	ZROE	O	RAM read pin
39	ERA	I/O	Erasure flag RAM data input/output
40	V_{SS}	–	Ground
41	V_{DD}	–	5 V supply
42	IO0	I/O	Data buffer RAM input/output. These pins have internal pull-up resistors.
43	IO1	I/O	
44	IO2	I/O	
45	IO3	I/O	
46	IO4	I/O	

Number	Name	I/O	Description
47	IO5	I/O	Data buffer RAM input/output. These pins have internal pull-up resistors.
48	IO6	I/O	
49	IO7	I/O	
50	V_{SS}	–	Ground
51	EXTAL	I	Crystal oscillator
52	XTAL	O	
53	TEST	I	Test pin. Connect to V_{SS}.
54	V_{SS}	–	Ground
55	MCK	O	Connections to CD-DSP
56	LRCK	I	
57	SDATA	I	
58	BCK	I	
59	C2PO	I	
60	WFCK	I	Sub-code inputs and outputs
61	EXCK	O	
62	SBSO	I	
63	SCOR	I	
64	CEMPHAS	O	Connect to CD-DSP emphasis pin
65	ZRESET	I	Reset pin. Hold LOW for 1 μs.
66	SCPUCNT	I	SUB-CPU interface select
67	D0	I/O	SUB-CPU data signal pins. These pins have internal pull-up resistors.
68	D1	I/O	
69	D2	I/O	
70	D3	I/O	
71	D4	I/O	
72	D5	I/O	
73	D6	I/O	
74	D7	I/O	
75	V_{SS}	–	Ground
76	SUA0	I	SUB-CPU register select address
77	SUA1	I	
78	SUA2	1	
79	SUA3	I	
80	SUA4	I	
81	ZSWAIT	O	WAIT signal to SUB-CPU
82	ZINT	O	SUB-CPU interrupt signal. This is an open-drain output, with an internal pull-up resistor.
83	RS (ALE)	I	Internal register set pin
84	ZRD	I	SUB-CPU read signal

Number	Name	I/O	Description
85	ZWR	I	SUB-CPU write signal
86	ZCS	O	SUB-CPU chip select seignal
87	ZENABLE	I	Chip select from host
88	SELDRQ	I	DRQ/WAIT select
89	V_{DD}	–	5 V supply
90	V_{SS}	–	Ground
91	ZWAIT/DRQ	O	DRQ/ZWAIT output
92	ZDTEN	O	Data enable
93	ZSTEN	O	Status enable
94	ZHWR	I	Host data write signal
95	ZHRD	I	Host data read signal
96	ZCMD	1	Host data/command signal select
97	SA1	I	Audio block register select
98	SA0	I	Host register select
99	ZAPCS	I	Host register chip select
100	BUSY	O	Busy signal. This signal is active when the host writes ADPCM data.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	T_a = 25 °C	–0.3 to 7.0	V
Input/output voltage	V_I, V_O	T_a = 25 °C	–0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	$T_a \leq$ 70 °C	350	mW
Operating temperature	T_{opg}		–30 to 70	°C
Storage temperature	T_{stg}		–55 to 125	°C
Soldering temperature		10 s	260	°C

Recommended Operating Conditions

T_a = –30 to +70 °C, V_{SS} = 0 V

Parameter	Symbol	Rating			Unit
		min	typ	max	
Supply voltage	V_{DD}	4.5	5.0	5.5	V
Input voltage range	V_{IN}	0	–	V_{DD}	V

DC Electrical Characteristics

V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_a = −30 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level input voltage	V_{IH1}	All input pins except XTALCK and those in the note.	2.2	–	–	V
LOW-level input voltage	V_{IL1}		–	–	0.8	V
HIGH-level input voltage	V_{IH2}	See note.	2.5	–	–	V
LOW-level input voltage	V_{IL2}		–	–	0.6	V
HIGH-level output voltage	V_{OH1}	I_{OH1} = −3 mA, all output pins excepting ZTAL and ZINT	2.4	–	–	V
LOW-level output voltage	V_{OL1}	I_{OL1} = 3 mA, all output pins excepting ZTAL and ZINT	–	–	0.4	V
LOW-level output voltage	V_{OL2}	I_{OL2} = 3 mA, ZINT (open-drain with pull-up)	–	–	0.4	V
Input leakage current	I_L	V_I = V_{SS} or V_{DD}, all input pins	−25	–	25	μA
Pull-up resistance	R_{UP}	All bus pins, ZINT	10	20	40	kΩ

Note
RESET (Schmitt trigger) and all bus pins (ZHRD, ZHWR, ZENABLE, ZCMD, WFCK, SBSO and SCOR)

FUNCTIONAL DESCRIPTION

The LC89560 has five main functional blocks. Each is described in the following sections.

CD Player Interface and Data Input Block

The LC89560 supports three different input data formats, selected by programming the CSEL and LMSEL internal registers.

The internal operation of the device is synchronized to the input data signal on a block-by-block (that is, sector-by-sector) basis. The sync detector circuit operates by detecting patterns in the input data. An additional sync insertion circuit can be used to preserve synchronization. These two synchronization methods can be programmed on or off.

The input data passes through the de-scrambling circuit, and is then written 8 bits at a time into buffer RAM. The C2 pointer (error flag) from the CD player is also written into RAM. If the error correction block uses 128 Kbits or more, the RAM is nine bits wide. However, the C2 pointer can also be omitted—in this case, the RAM need only be eight bits wide. Note that erasure correction cannot be performed if the C2 pointer is omitted.

Data from the CD is written to buffer RAM in its entirety, including the SYNC, header, sub-header and parity (2352 bytes per block).

The LC89560 master clock is output on MCK, thus allowing this clock to be used as the CD LSI clock.

Error Detection and Correction

Error correction is performed on each block (2352 bytes) after it has been stored in buffer RAM.

The LC89560 is able to perform error correction in real time in hardware. This allows controller software to perform other functions during this time, such as buffering data from the CD or transferring data to the host computer. This ensures that the data transfer rate from the CD is not reduced while corrected data is being sent to the host computer.

The standard error detection and correction technique is supplemented by an erasure correction method using the C2 pointer. This results in very low error rates. The standard error correction can correct one incorrect symbol whereas the erasure correction can correct two incorrect symbols.

The correction algorithm is programmable, allowing the use of a variety of techniques, including repeated correction and QP/PQ correction.

After recovery of the error correction code (ECC), a 32-bit CRC error check is performed using the error detection code (EDC). The header and sub-header are stored into internal registers at this time.

The LC89560 then generates a decoding-completed interrupt to the host microcontroller. The controller reads the header, sub-header, block header address in buffer RAM, and the decoding status from the LC89560.

Also, since the 8 Kbit erasure RAM has been integrated into the chip, the usual external 8 Kbit RAM is not needed.

Host Interface Block

The data transfer rate to the host computer has been increased to a peak rate of 2.3 Mbytes/s. Up to 60 Kbytes of external buffer RAM can now be supported, allowing up to 26 sectors of data to be buffered. This can be used to implement disk caching.

The host command interface has an 8-byte FIFO for received commands. By activating the ZHWR signal, the host can write up to eight commands at once. When the host writes to the FIFO, the LC89560 generates a command interrupt to the host microcontroller. The command written to the FIFO is not interpreted completely by the LC89560 at this time. To transfer data to the host, the host microcontroller sets the LC89560 registers with the number of bytes to be transferred and the buffer RAM address of the header of the block to be transferred. It then writes to the transfer trigger register. ZDTEN then goes LOW to indicate the start of data transfer to the host. The host repeatedly generates ZHRD pulses while ZDTEN is LOW to read the data. If the host attempts to read data faster than approximately 2.3 Mbytes/s, the LC89560 activates the ZWAIT/DRQ signal. The host must hold ZHRD HIGH while ZWAIT/DRQ is LOW. During the transfer of this block, the microcontroller waits for the next transfer-completed interrupt.

DRQ (data request) data transfer can be peformed using the SELDRQ pin. This form of data transfer operates rather like a DMA controller in that the host generates ZHRD pulses in response to the data request signal produced by the LC89560.

When the last data byte is read, ZEOP goes active while the read pulse is active. Following that, the ZDTEN signal goes inactive. The transfer-completed interrupt is then generated to inform the microcontroller that data transfer to the host has completed.

The microcontroller can transfer information such as the decoding results and CD-ROM drive status to the host computer by writing to registers in the LC89560. The status register comprises twelve bytes. The microcontroller and the host handshake using the ZSTEN signal. The LC89560 has no knowledge of the contents of these registers.

Since these command and status registers are not interpreted or executed by the LC89560, the meaning of the data passed through these registers can be defined in any way desired. Thus, CD-ROM applications can be easily designed, and the LC89560 can easily be incorporated into existing systems.

Shared Circuits

The LC89560 performs data decoding and buffering using pipeline processing. Furthermore, writing to buffer RAM, data decoding and transfer of data from buffer RAM to the host can be synchronized and performed simultaneously. As a result, the controlling microcontroller does not need to control access to the buffer RAM in any way.

ADPCM Decoder

Error-corrected ADPCM data (although in actual fact, error correction is not performed) is transferred to the ADPCM decoder under the control of the microcontroller. Transfer is essentially the same as for transfer of data to the host.

More correctly, data is transferred between the SRAM error correction area and the ADPCM data area. The ADPCM decoder then reads the data from the ADPCM data area and initiates audio replay.

The level (A, B, or C) and stereo/mono mode can be determined from the sub-header data. Also, temporarily collected ADPCM data can be replayed to the host.

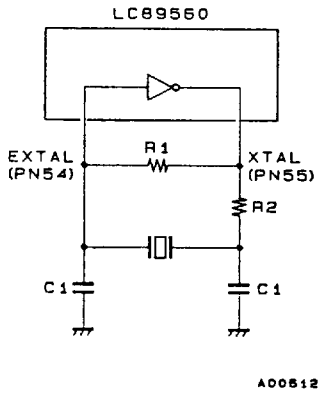
The LC89560 ADPCM decoder output can be directly connected to the LC7883K eight-times oversampling filter and D/A converter.

CD-DA data can also be specified for output on the audio output pins by programming the internal registers. Digital mute is also provided (for ADPCM replay only.)

Sub-code Data Interface

Sub-code data can be written to the external RAM by connecting to the sub-code pin of the CD-DSP, thus allowing the microcontroller to read the sub-code values. The Q code contains the CRC check information.

RECOMMENDED OSCILLATOR CIRCUIT



LC89560
R1 = 120kΩ
R2 = 47Ω
C1 = 30pF
16.9344 MHz crystal oscillator frequency