19-2730; Rev 0; 1/03

MAXIM

# 10Gbps EAM Driver with Integrated Bias Network



## General Description

The MAX3940 is designed to drive an electro-absorption modulator (EAM) at data rates up to 10.7Gbps. It incorporates the functions of a biasing circuit and a modulation circuit, with integrated control op amps externally programmed by DC voltages.

The integrated bias circuit provides a programmable biasing current up to 50mA. This bias current reflects a bias voltage of up to 1.25V on an external 50Ω load. The bias and modulation circuits are internally connected on chip, eliminating the need for an external bias inductor.

A high-bandwidth, fully differential signal path is internally implemented to minimize jitter accumulation. When a clock signal is available, the integrated data-retiming function can be selected to reject input-signal jitter.

The MAX3940 receives differential CML signals (ground referenced) with on-chip line terminations of 50Ω. The output has a 50Ω resistor for back termination and is able to deliver a modulation current of 40mA$_{P-P}$ to 120mA$_{P-P}$, with an edge speed of 23ps (typical, 20% to 80%). This modulation current reflects an EAM modulation voltage of 1.0V$_{P-P}$ to 3.0V$_{P-P}$.

The MAX3940 also includes an adjustable pulse-width control circuit to precompensate for asymmetrical EAM characteristics.

## Features

- ♦ On-Chip Bias Network
- ♦ 23ps Edge Speed
- ♦ Programmable Modulation Voltage Up to 3V$_{P-P}$
- ♦ Programmable EAM Biasing Voltage Up to 1.25V
- ♦ Selectable Data-Retiming Latch
- ♦ Up to 10.7Gbps Operation
- ♦ Integrated Modulation and Biasing Functions
- ♦ 50Ω On-Chip Input and Output Terminations
- ♦ Pulse-Width Adjustment
- ♦ Enable and Polarity Controls
- ♦ ESD Protection

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX3940E/D | -40°C to +85°C | Dice* |

*Dice are designed to operate over a -40°C to +120°C junction temperature ($T_J$) range, but are tested and guaranteed at $T_A$ = +25°C only.

## Applications

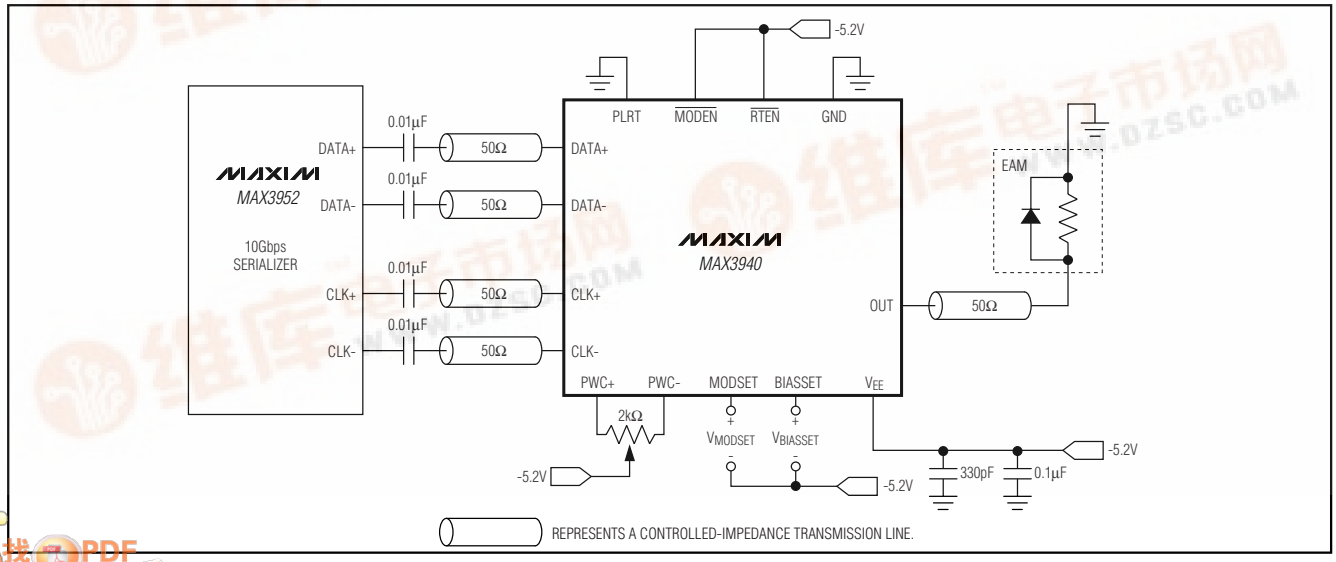
SONET OC-192 and SDH STM-64 Transmission Systems

DWDM Systems

Long/Short-Reach Optical Transmitters

10Gbps Ethernet

## Typical Application Circuit



# 10Gbps EAM Driver with Integrated Bias Network

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage $V_{EE}$ .....-6.0V to +0.5V
Voltage at $\overline{MODEN}$, $\overline{RTEN}$, PLRT, MODSET, BIASSET .....($V_{EE}$ - 0.5V) to +0.5V
Voltage at DATA+, DATA-, CLK+, and CLK-.....-1.65V to +0.5V
Voltage at OUT .....-4V to +0.5V
Voltage at PWC+, PWC- .....($V_{EE}$ - 0.5V) to ($V_{EE}$ + 1.7V)
Current into or out of OUT.....80mA
Storage Temperature Range .....-55°C to +150°C
Operating Junction Temperature Range.....-55°C to +150°C
Processing Temperature (die).....+400°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{EE}$ = -5.5V to -4.9V, $T_A$ = -40°C to +85°C. Typical values are at $V_{EE}$ = -5.2V, $I_{BIAS}$ = 30mA, $I_{MOD}$ = 100mA, and $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Power-Supply Voltage | $V_{EE}$ | | | -5.5 | | -4.9 | V |
| Supply Current | $I_{EE}$ | Excluding $I_{BIAS}$ and $I_{MOD}$ (Note 1) | Retime disabled | | 122 | 170 | mA |
| | | | Retime enabled | | 139 | 195 | |
| Power-Supply Noise Rejection | PSNR | f ≤ 10MHz (Note 2), see Figure 4 | | | 12 | | dB |
| **SIGNAL INPUT** (Note 3) | | | | | | | |
| Input Data Rates | | NRZ | | | 10.7 | | Gbps |
| Single-Ended Input Resistance | $R_{IN}$ | Input to GND (Note 3) | | 42.5 | 50 | 58.5 | Ω |
| Single-Ended Input Voltage | $V_{IS}$ | DC-coupled, Figure 1a | | -1 | | 0 | V |
| | | AC-coupled, Figure 1b | | -0.4 | | +0.4 | |
| Differential Input Voltage | $V_{ID}$ | DC-coupled (Note 4) | | 0.2 | | 2.0 | $V_{P-P}$ |
| | | AC-coupled (Note 4) | | 0.2 | | 1.6 | |
| Differential Input Return Loss | $RL_{IN}$ | (Note 3) | ≤ 10GHz | | 17 | | dB |
| | | | 10GHz < f ≤ 15GHz | | 10 | | |
| **EAM BIAS** | | | | | | | |
| Maximum Bias Current | | $V_{BIASSET}$ = $V_{EE}$ + 2V | | 50 | 55 | | mA |
| Minimum Bias Current | | $V_{BIASSET}$ = $V_{EE}$ | | | 0.3 | 1 | mA |
| BIASSET Voltage Range | $V_{BIASSET}$ | | | $V_{EE}$ | | $V_{EE}$ + 2 | V |
| Equivalent Bias Resistance | $R_{BSEQV}$ | (Note 5) | | | 36.4 | | Ω |
| Bias-Current-Setting Accuracy | | $T_A$ = +25°C | $V_{BIASSET}$ = $V_{EE}$ + 0.11V | 2.1 | | 3.9 | mA |
| | | | $V_{BIASSET}$ = $V_{EE}$ + 0.36V | 8.8 | | 11.2 | |
| | | | $V_{BIASSET}$ = $V_{EE}$ + 2.0V | 52 | | 58 | |
| Bias-Current Temperature Stability | | (Note 6) | $V_{BIASSET}$ < $V_{EE}$ + 0.36V | -1300 | | +1300 | ppm/°C |
| | | | $V_{BIASSET}$ ≥ $V_{EE}$ + 0.36V | -480 | | +480 | |
| BIASSET Input Resistance | | | | | 20 | | kΩ |
| BIASSET Bandwidth | | 50Ω driver load, $V_{BIASSET}$ = $V_{EE}$ + 0.55V, Figure 2 | | | 5 | | MHz |
| **EAM MODULATION** | | | | | | | |
| Maximum Modulation Current | | $V_{MODSET}$ = $V_{EE}$ + 1V | | 120 | 127 | | $mA_{P-P}$ |
| Minimum Modulation Current | | $V_{MODSET}$ = $V_{EE}$ | | | 38 | 40 | $mA_{P-P}$ |
| MODSET Voltage Range | $V_{MODSET}$ | | | $V_{EE}$ | | $V_{EE}$ + 1 | V |
| Equivalent Modulation Resistance | $R_{MODEQV}$ | (Note 7) | | | 11.1 | | Ω |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{EE}$ = -5.5V to -4.9V, $T_A$ = -40°C to +85°C. Typical values are at $V_{EE}$ = -5.2V, $I_{BIAS}$ = 30mA, $I_{MOD}$ = 100mA, and $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Modulation Set Bandwidth | | Modulation depth 10%, 50Ω driver load, see Figure 2 | | 5 | | MHz |
| MODSET Input Resistance | | | | 20 | | kΩ |
| Modulation-Current Temperature Stability | | (Note 6) | -480 | | +480 | ppm/°C |
| Modulation-Current Setting Error | | 50Ω driver load, $T_A$ = +25°C | -5 | | +5 | % |
| Output Resistance | $R_{OUT}$ | OUT to GND | 42.5 | 50 | 58.5 | Ω |
| Total Off Current | | BIASSET = $V_{EE}$, $\overline{MODEN}$ = $V_{EE}$, MODSET = $V_{EE}$, DATA+ = high, DATA- = low | | | 1 | mA |
| Output Return Loss | $RL_{OUT}$ | $I_{BIAS}$ = 30mA, $I_{MOD}$ = 50mA, ≤ 5GHz | | 8 | | dB |
| Output Edge Speed | | 20% to 80% (Notes 6, 8) | | 23 | 32 | ps |
| Setup/Hold Time | $t_{SU}$, $t_{HD}$ | Figure 3 (Note 6) | 25 | | | ps |
| Pulse-Width Adjustment Range | | (Notes 6, 8) | ±20 | ±50 | | ps |
| Pulse-Width Control Input Range (Single Ended) | | For PWC+ and PWC- | $V_{EE}$ + 0.5 | | $V_{EE}$ + 1.5 | V |
| Pulse-Width Control Input Range (Differential) | | (PWC+) - (PWC-) | -0.5 | | +0.5 | V |
| Output Overshoot | δ | (Notes 6, 8) | -10 | | +10 | % |
| Driver Random Jitter | $RJ_{DR}$ | (Note 6) | | 0.3 | 1.1 | $ps_{RMS}$ |
| Driver Deterministic Jitter | $DJ_{DR}$ | PWC- = GND (Notes 6, 9) | | 6.8 | 14 | $ps_{P-P}$ |
| **CONTROL INPUTS** | | | | | | |
| Input High Voltage | $V_{IH}$ | (Note 10) | $V_{EE}$ + 2.0 | | | V |
| Input Low Voltage | $V_{IL}$ | (Note 10) | | | $V_{EE}$ + 0.8 | V |
| Input Current | | (Note 10) | -80 | | +80 | µA |

**Note 1:** Supply current remains elevated once the retiming function has been enabled. Power must be cycled to reduce supply current after the retiming function has been disabled.

**Note 2:** Power-supply noise rejection is specified as PSNR = 20Log($V_{noise\ (on\ Vcc)}$ / $\Delta V_{OUT}$). $V_{OUT}$ is the voltage across a 50Ω load. $V_{noise\ (on\ Vcc)}$ = $100mV_{P-P}$.

**Note 3:** For DATA+, DATA-, CLK+, and CLK-.

**Note 4:** CLK input characterized at 10.7Gbps

**Note 5:** $R_{BSEQV}$ = ($V_{BIASSET}$ - $V_{EE}$) / $I_{OUT}$ with $\overline{MODEN}$ = $V_{EE}$, DATA+ = high, and DATA- = low.

**Note 6:** Guaranteed by design and characterization using the circuit shown in Figure 4.

**Note 7:** $R_{MODEQV}$ = ($V_{MODSET}$ - $V_{EE}$) / ($I_{OUT}$ - 37mA) with BIASSET = $V_{EE}$.

**Note 8:** 50Ω load, characterized at 10.7Gbps with a 1111 1111 0000 0000 pattern.

**Note 9:** Deterministic jitter is defined as the arithmetic sum of PWD (pulse-width distortion) and PDJ (pattern-dependent jitter). Measured with a 10.7Gbps $2^7$ - 1 PRBS pattern with eighty 0s and eighty 1s inserted in the data pattern.

**Note 10:** For $\overline{MODEN}$ and PLRT.

# 10Gbps EAM Driver with Integrated Bias Network

## Test Circuits and Timing Diagrams

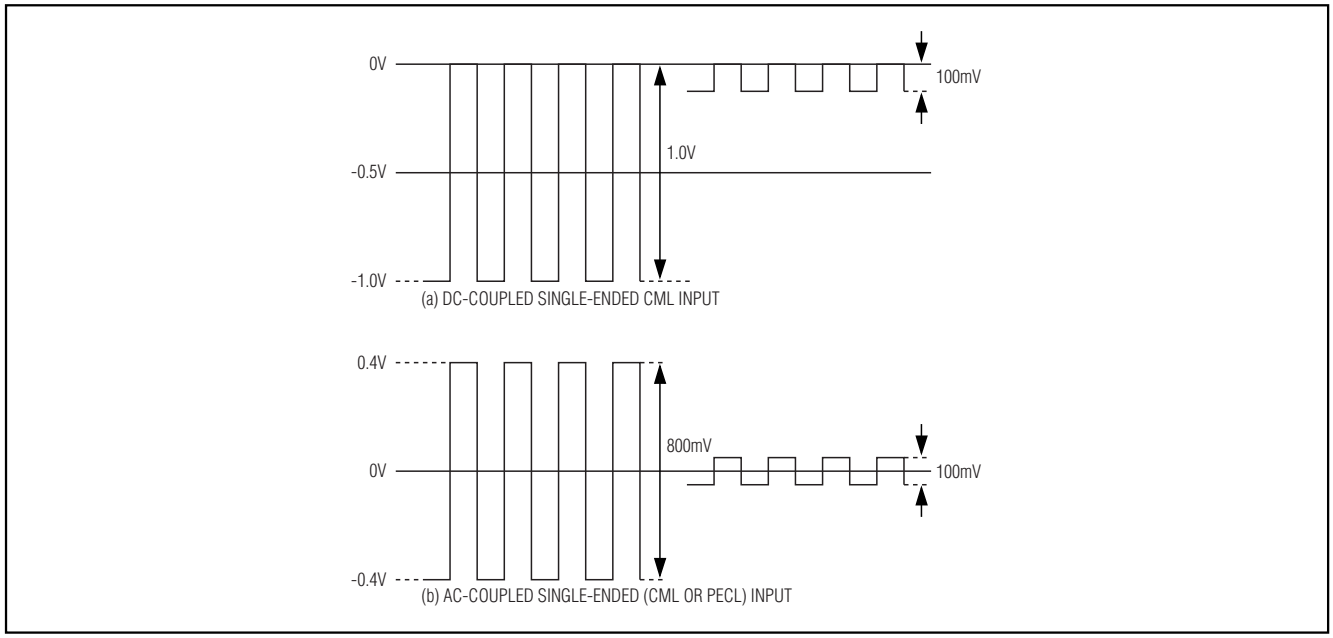



*Figure 1. Definition of Single-Ended Input Voltage Range*

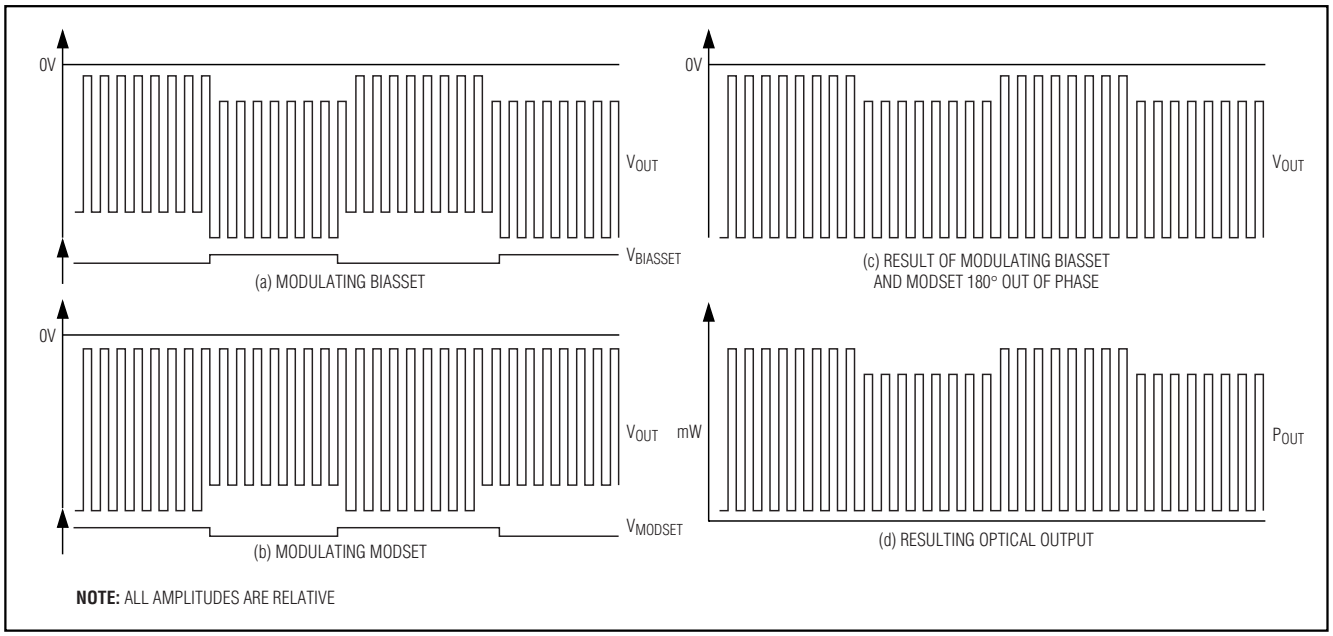



*Figure 2. Modulating BIASSET and MODSET pads*

## Test Circuits and Timing Diagrams (continued)

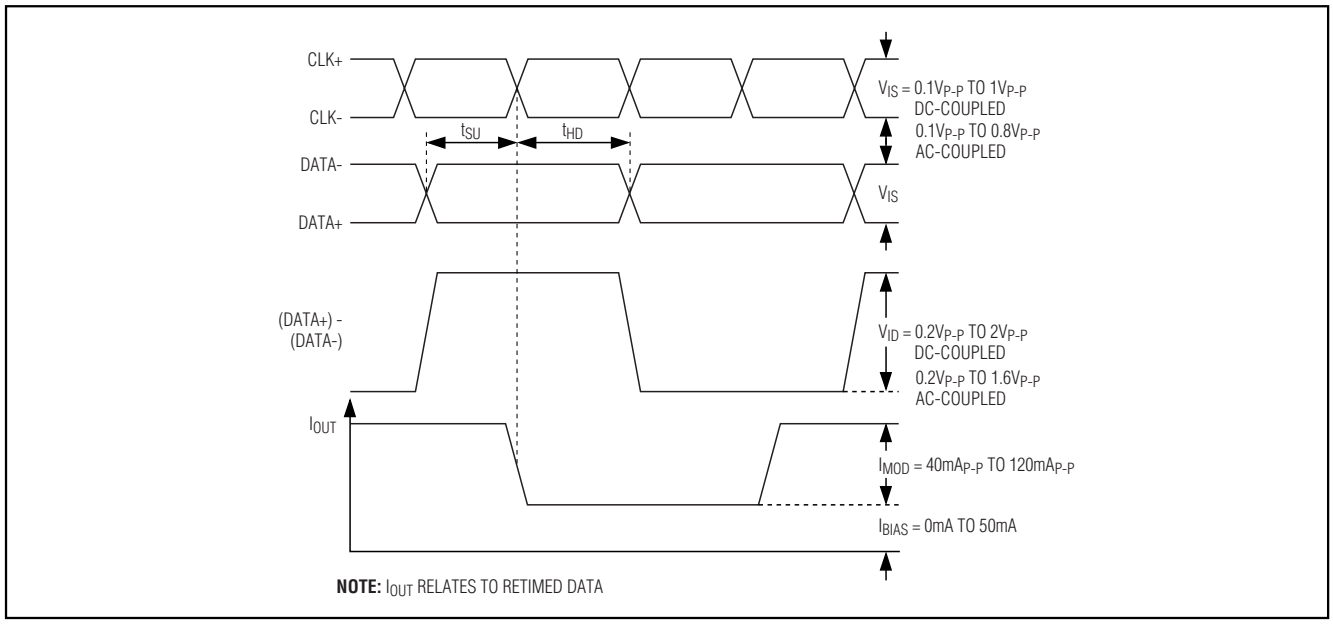



*Figure 3. Setup and Hold Timing Definition*

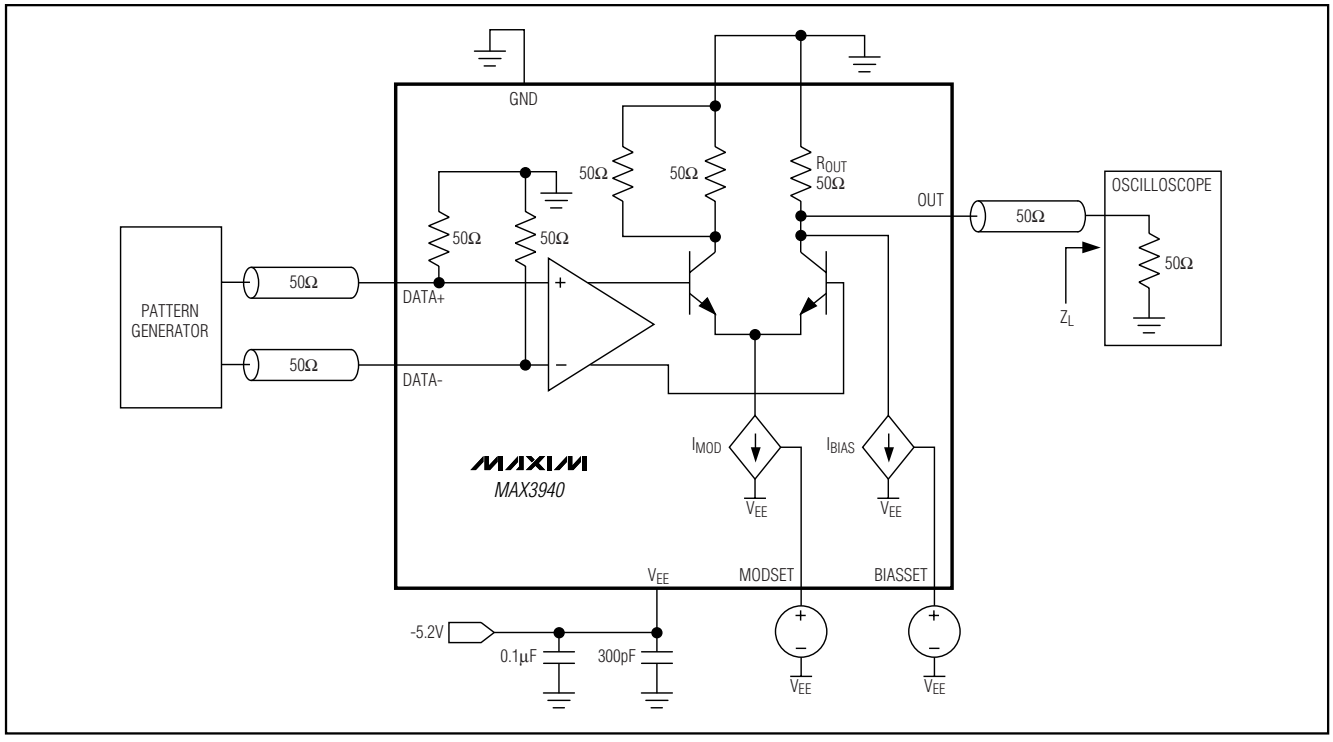



*Figure 4. AC Characterization Circuit*

# 10Gbps EAM Driver with Integrated Bias Network

## Test Circuits and Timing Diagrams (continued)

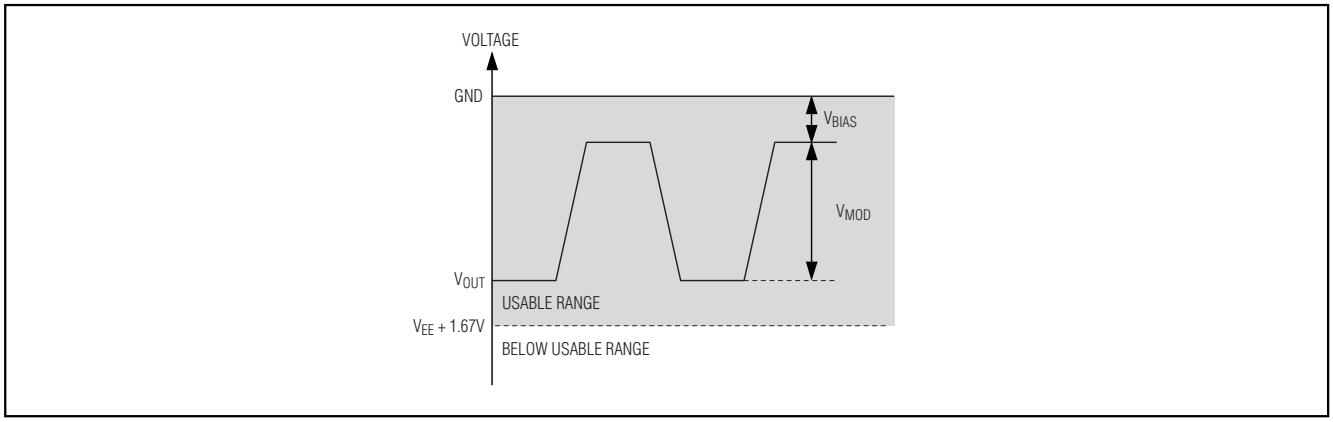
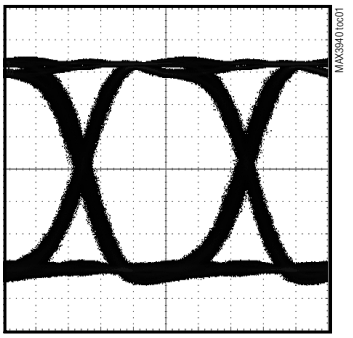



*Figure 5. Bias and Modulation Relationship to EAM Voltage*

## Typical Operating Characteristics

(Typical values are at $V_{EE}$ = -5.2V, $I_{BIAS}$ = 30mA, $I_{MOD}$ = 100mA, $T_A$ = +25°C, unless otherwise noted.)

**10Gbps ELECTRICAL EYE DIAGRAM ($V_{MOD}$ = 1$V_{P-P}$, $2^{31}$ - 1 PRBS)**

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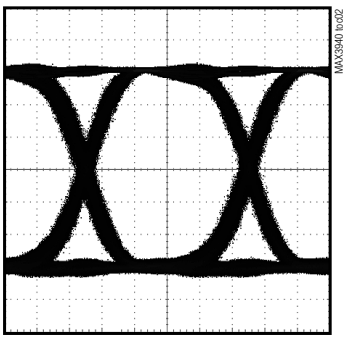
**10Gbps ELECTRICAL EYE DIAGRAM ($V_{MOD}$ = 3$V_{P-P}$, $2^{31}$ - 1 PRBS)**

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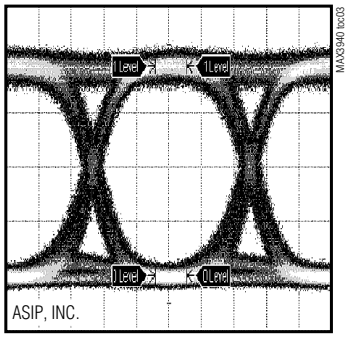
**10.3Gbps OPTICAL EYE DIAGRAM**

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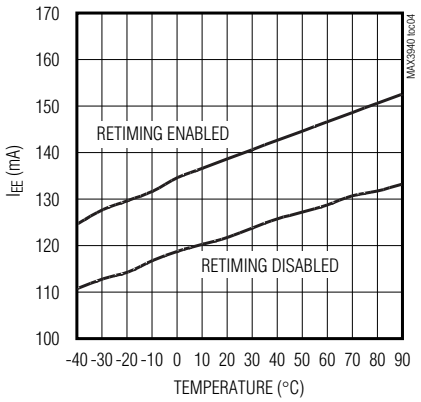
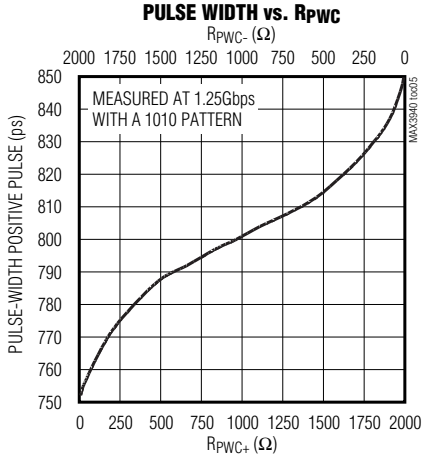
**SUPPLY CURRENT vs. TEMPERATURE (50Ω LOAD, EXCLUDES $I_{BIAS}$, $I_{MOD}$)**



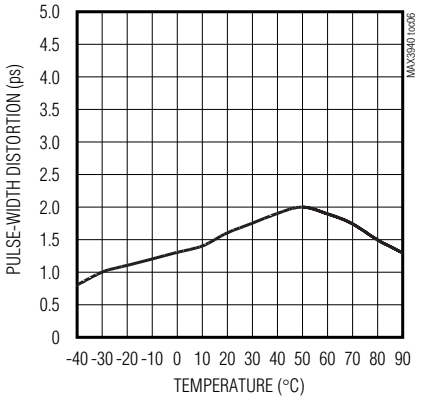

**PULSE WIDTH vs. $R_{PWC}$**



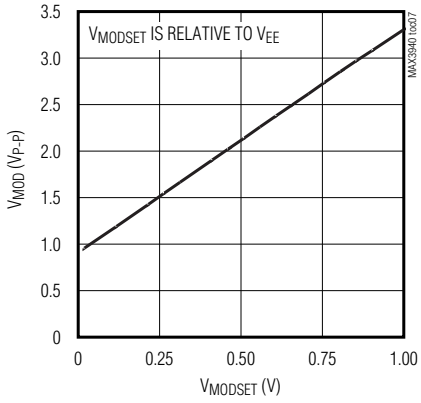
## Typical Operating Characteristics (continued)

(Typical values are at $V_{EE}$ = -5.2V, $I_{BIAS}$ = 30mA, $I_{MOD}$ = 100mA, $T_A$ = +25°C, unless otherwise noted.)

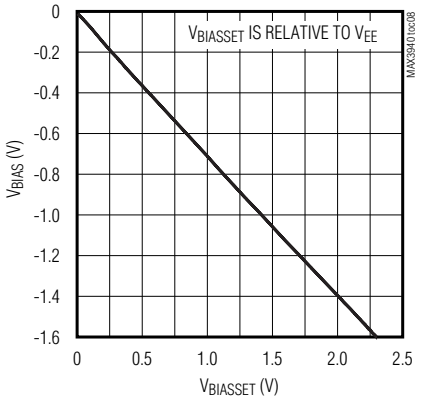
**PULSE-WIDTH DISTORTION vs. TEMPERATURE**



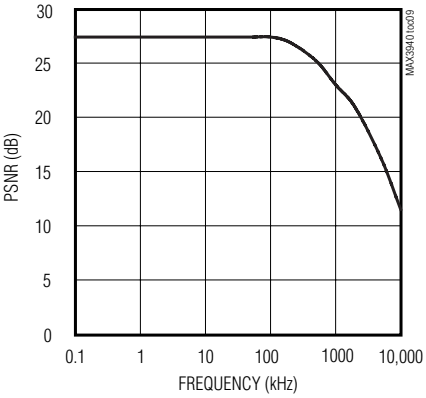

**$V_{MOD}$ vs. $V_{MODSET}$ ($Z_L$ = 50Ω)**



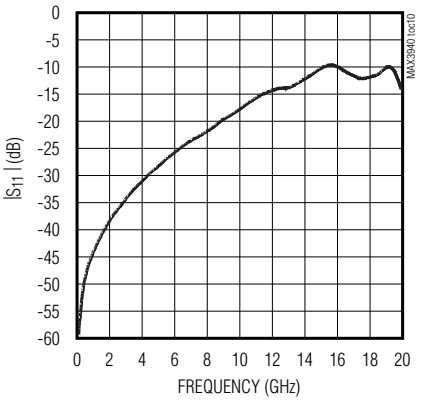

**$V_{BIAS}$ vs. $V_{BIASSET}$ ($Z_L$ = 50Ω)**



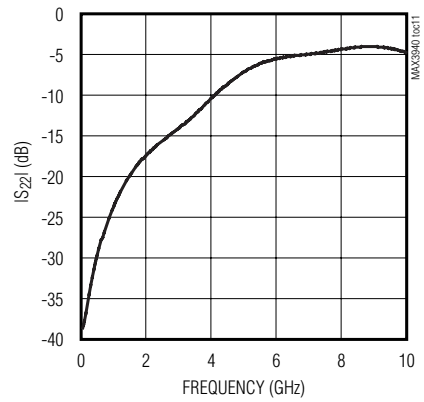

**POWER-SUPPLY NOISE REJECTION vs. FREQUENCY**




**DIFFERENTIAL $S_{11}$ vs. FREQUENCY**




**$S_{22}$ vs. FREQUENCY (DEVICE POWERED)**



# 10Gbps EAM Driver with Integrated Bias Network

## Pad Description

| PAD | NAME | FUNCTION |
|---|---|---|
| BP1, BP2, BP4, BP5, BP7–BP12, BP14, BP15, BP17–BP24, BP26, BP27, BP28 | GND | Ground. All pads must be connected to board ground. |
| BP3 | DATA+ | Noninverting Data Input, with 50Ω On-Chip Termination |
| BP6 | DATA- | Inverting Data Input, with 50Ω On-Chip Termination |
| BP13 | CLK+ | Noninverting Clock Input for Data Retiming, with 50Ω On-Chip Termination |
| BP16 | CLK- | Inverting Clock Input for Data Retiming, with 50Ω On-Chip Termination |
| BP25 | OUT | Driver Output. Provides both modulation and bias output. DC-couple to EAM. |
| BP29 | $\overline{\text{MODEN}}$ | TTL/CMOS Modulation Enable Input. Set low or float for normal operation. Set high to put the EAM in the absorption (logic 0) state. Contains an internal 100kΩ pulldown to $V_{EE}$. |
| BP30 | $\overline{\text{RTEN}}$ | Data-Retiming Input. Connect to $V_{EE}$ for retimed data. Connect to GND to bypass retiming latch. |
| BP31 | BIASSET | Bias Current Set. Apply a voltage to set the bias current of the driver output. |
| BP32 | MODSET | Modulation Current Set. Apply a voltage to set the modulation current of the driver output. |
| BP33–BP41 | $V_{EE}$ | Negative Supply Voltage. All pads must be connected to $V_{EE}$. |
| BP42 | PWC+ | Positive Input for Modulation Pulse-Width Adjustment (see the *Design Procedure* section). |
| BP43 | PWC- | Negative Input for Modulation Pulse-Width Adjustment. Ground to disable the pulse-width adjustment feature (see the *Design Procedure* section). |
| BP44 | PLRT | Differential Data Polarity Swap Input. Set high or float for normal operation. Set low to invert the differential signal polarity. Contains an internal 100kΩ pullup to GND. |

## Detailed Description

The MAX3940 EAM driver consists of two main parts: a high-speed modulation driver and an EAM-biasing block. The clock and data inputs to the driver are compatible with PECL and CML logic levels. The modulation and bias current are output through the OUT pad.

The modulation output stage is composed of a high-speed differential pair and a programmable current source with a maximum modulation current of 120mA. The rise and fall times are typically 23ps. The modulation current is designed to produce an EAM voltage up to $3.0V_{P-P}$ when driving a 50Ω module. The $3.0V_{P-P}$ results from $120mA_{P-P}$ through the parallel combination of the 50Ω EAM load and the internal 50Ω back termination.

### Polarity Switch

The MAX3940 includes a polarity switch. When the PLRT pad is high or left floating, the output maintains the polarity of the input data. When the PLRT pad is low, the output is inverted relative to the input data.

### Clock/Data Input Logic Levels

The MAX3940 is directly compatible with ground-reference CML. Either DC- or AC-coupling may be used for CML referenced to ground. For all other logic types, AC-coupling should be used.

### Optional Data Input Latch

To reject pattern-dependent jitter in the input data, a synchronous differential clock signal should be connected to the CLK+ and CLK- inputs, and the $\overline{\text{RTEN}}$ control input should be connected to $V_{EE}$.

The input data is retimed on the rising edge of CLK+. If $\overline{RTEN}$ is connected to ground, the retiming function is disabled and the input data is directly connected to the output stage. Leave CLK+ and CLK- open when retiming is disabled.

### Pulse-Width Control

The pulse-width control circuit can be used to compensate for pulse-width distortion introduced by the EAM. The differential voltage between PWC+ and PWC- adjusts the pulse-width compensation. The adjustment range is typically ±50ps. Optional single-ended operation is possible by forcing a voltage on the PWC+ pad while leaving the PWC- pad unconnected. When PWC- is connected to ground, the pulse-width control circuit is automatically disabled.

### Modulation Output Enable

The MAX3940 incorporates a modulation current-enable input. When $\overline{MODEN}$ is low or floating, the modulation/bias output (OUT) is enabled. When $\overline{MODEN}$ is high, the output is switched to the logic 0 state. The typical enable time is 2ns and the typical disable time is 2ns.

## Design Procedure

### Programming the Modulation Voltage

The EAM modulation voltage results from $I_{MOD}$ passing through the EAM impedance ($Z_L$) in parallel with the internal 50Ω termination resistor ($R_{OUT}$).

$$V_{MOD} \approx I_{MOD} \times \frac{Z_L \times R_{OUT}}{Z_L + R_{OUT}}$$

To program the desired modulation current, force a voltage at the MODSET pad (see the *Typical Application Circuit*). The resulting $I_{MOD}$ current can be calculated by the following equation:

$$I_{MOD} \approx \frac{V_{MODSET}}{11.1\Omega} + 37mA$$

An internal, independent current source drives a constant 37mA to the modulation circuitry and any voltage above $V_{EE}$ on the MODSET pad adds to this. The input impedance of the MODSET pad is typically 20kΩ. Note that the minimum output voltage is $V_{EE}$ + 1.67V (see Figure 5).

### Programming the Bias Voltage

As in the case of modulation, the EAM bias voltage results from $I_{BIAS}$ passing through the EAM impedance ($Z_L$) in parallel with the internal 50Ω termination resistor ($R_{OUT}$).

$$V_{BIAS} \approx I_{BIAS} \times \frac{Z_L \times R_{OUT}}{Z_L + R_{OUT}}$$

To program the desired bias current, force a voltage at the BIASSET pad (see the *Typical Application Circuit*). The resulting $I_{BIAS}$ current can be calculated by the following equation:

$$I_{BIAS} \approx \frac{V_{BIASSET}}{36.4\Omega}$$

The input impedance of the BIASSET pad is typically 20kΩ. Note that the minimum output voltage is $V_{EE}$ + 1.67V (see Figure 5).

### Programming the Pulse-Width Control

Three methods of control are possible when pulse predistortion is desired to minimize distortion at the receiver. The pulse width may be set with a 2kΩ potentiometer with the center tapped to $V_{EE}$ (or equivalent fixed resistors), or by applying a voltage to the PWC+ pad, or by applying a differential voltage across the PWC+ and PWC- pads. See Table 1 for the desired effect of the pulse-width setting. Pulse width is defined as (positive pulse width)/((positive pulse width + negative pulse width)/2).

### Input Termination Requirement

The MAX3940 data and clock inputs are CML compatible. However, it is not necessary to drive the IC with a standard CML signal. As long as the specified input voltage swings are met, the MAX3940 will operate properly.

## Applications Information

### Layout Considerations

To minimize loss and crosstalk, keep the connections between the MAX3940 output and the EAM module as short as possible. Use good high-frequency layout techniques and multilayer boards with an uninterrupted ground plane to minimize EMI and crosstalk. Circuit boards should be made using low-loss dielectrics. Use controlled-impedance lines for the clock and data inputs as well as for the data output. Wafer capacitors are required to filter the $V_{EE}$ supply. Connect the backside of the die to GND.

**Table 1. Pulse-Width Control**

| PULSE WIDTH | $R_{PWC+}$, $R_{PWC-}$ FOR $R_{PWC+} + R_{PWC-} = 2k\Omega$ | $V_{PWC+}$ (PWC- OPEN) | $V_{PWC+} - V_{PWC-}$ |
|---|---|---|---|
| 100% | $R_{PWC+} = R_{PWC-}$ | $V_{EE}$ + 1V | 0V |
| >100% | $R_{PWC+} > R_{PWC-}$ | > $V_{EE}$ + 1V | >0V |
| <100% | $R_{PWC+} < R_{PWC-}$ | < $V_{EE}$ + 1V | <0V |

# 10Gbps EAM Driver with Integrated Bias Network

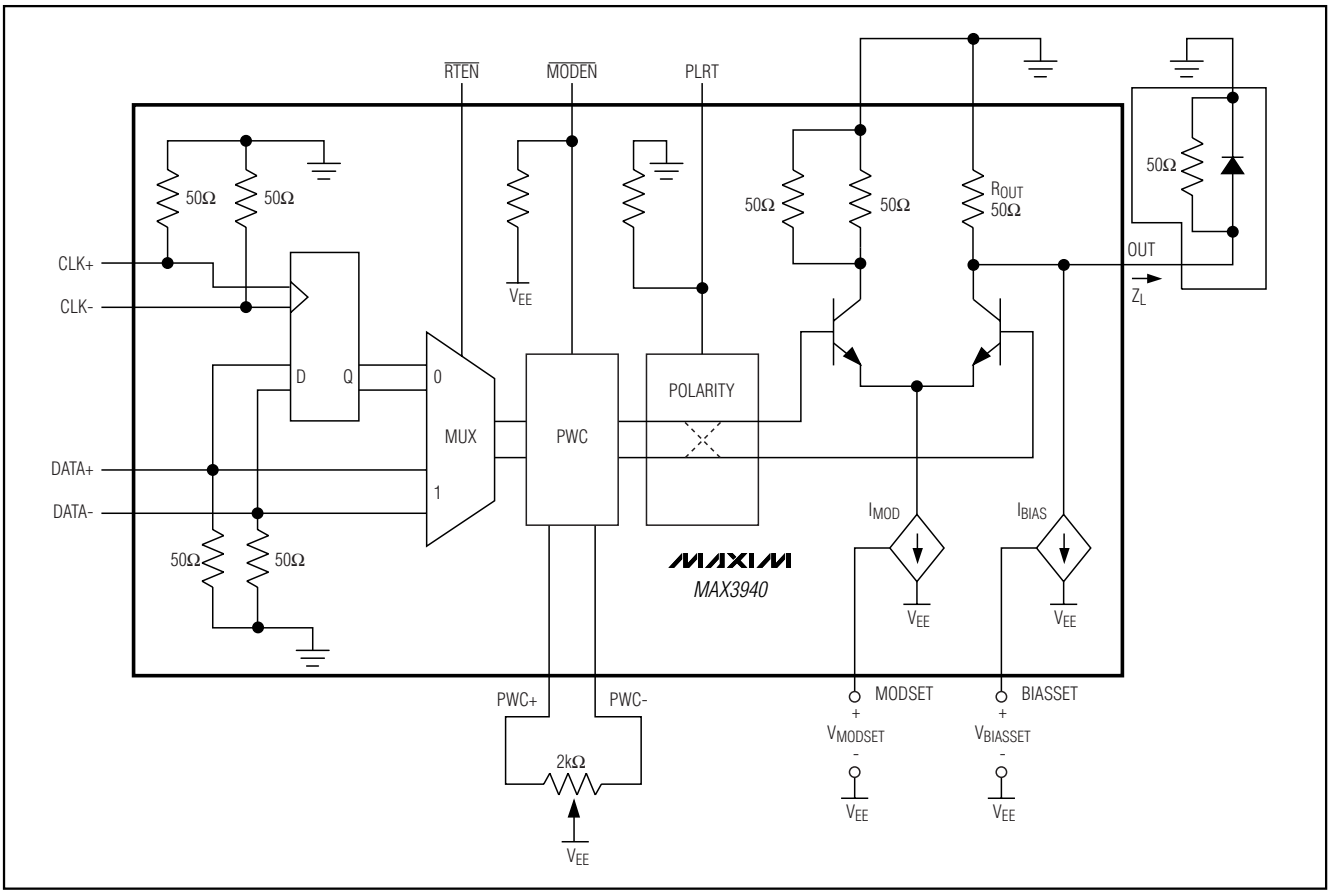



*Figure 6. Functional Diagram*

### Interface Schematics

Figures 7 and 8 show simplified input and output circuits of the MAX3940 EAM driver.

### Wire Bonding Die

For high-current density and reliable operation, the MAX3940 uses gold metalization. Make connections to the die with gold wire only, using ball-bonding techniques.

Minimize bond-wire lengths and ensure that the span between the ends of the bond wire does not come closer to the edge of the die than two times the bond-wire diameter. The minimum length of the bond wires might be constrained by the type of wire bonder used, as well as the dimensions of the die.

To minimize inductance, keep the connections from OUT, GND, and $V_{EE}$ as short as possible. This is crucial for optimal performance.

### Laser Safety and IEC 825

Using the MAX3940 EAM driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Each customer must determine the level of fault tolerance required by their application, recognizing that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

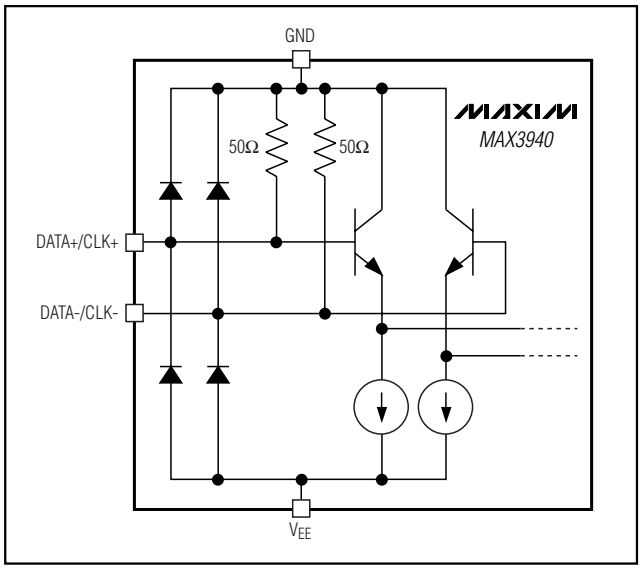



*Figure 7. Simplified Input Circuit*

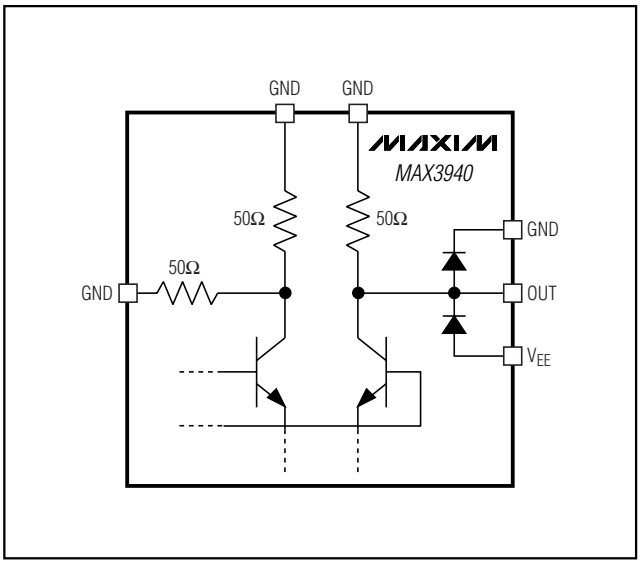



*Figure 8. Simplified Output Circuit*

## Chip Topography/ Pad Configuration

The origin for pad coordinates is defined as the bottom left corner of the bottom left pad. All pad locations are referenced from the origin and indicate the center of the pad where the bond wire should be connected. Refer to Maxim application note HFAN-08.0.1: *Understanding Bonding Coordinates and Physical Die Size* for detailed information.

Maxim characterized this circuit with gold wire (1-mil diameter wire) ball bonded to the pads. Die pad size is 4 mils (102µm) square, and die thickness is 8 mils (203µm).

## Chip Information

TRANSISTOR COUNT: 2084

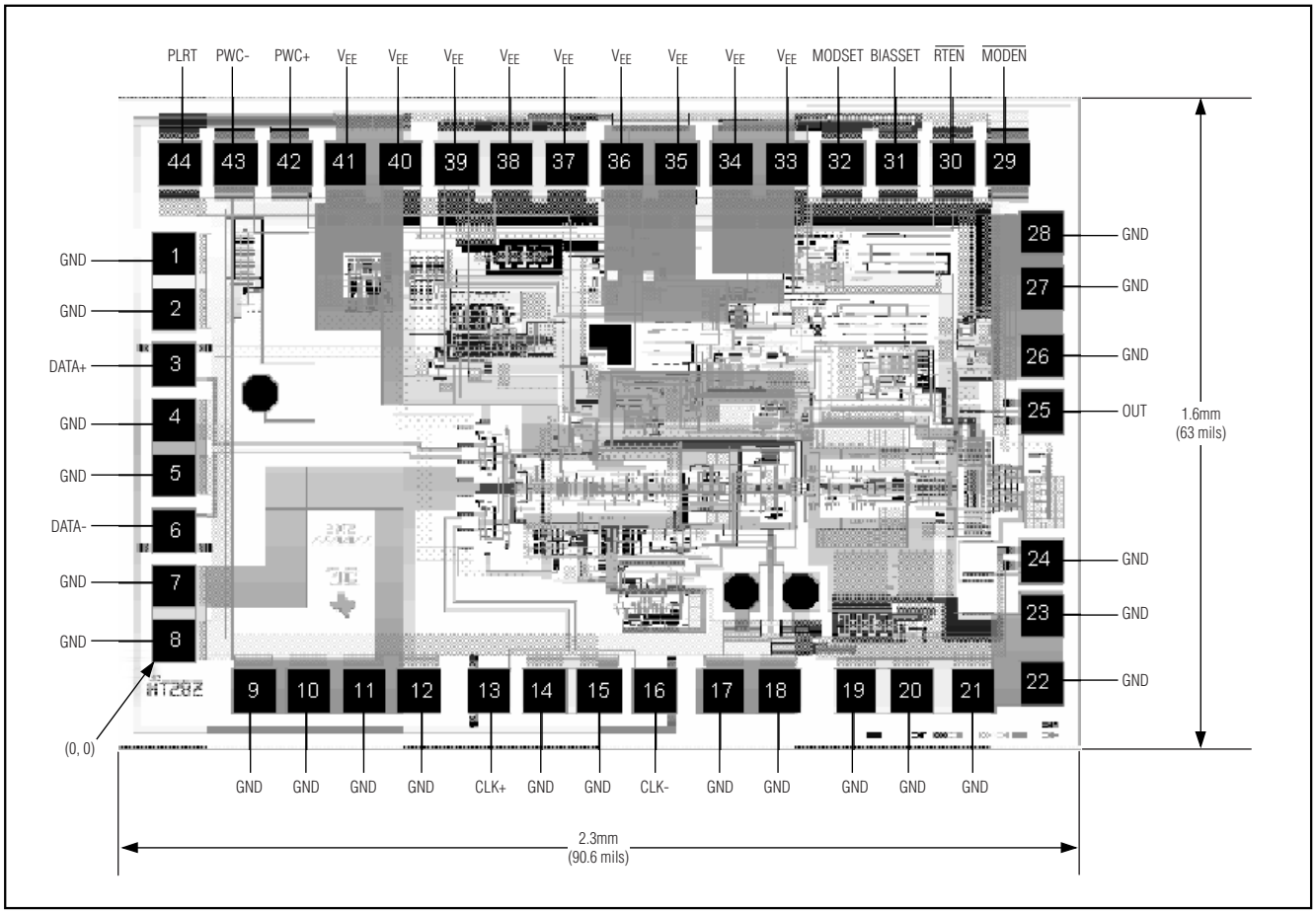
PROCESS: SiGe BIPOLAR

SUBSTRATE: SOI

DIE THICKNESS: 8 mils

# 10Gbps EAM Driver with Integrated Bias Network

## Chip Topography



## Table 2. Bondpad Locations

| PAD NUMBER | PAD NAME | COORDINATES (µm) | |
|---|---|---|---|
| | | X | Y |
| BP1 | GND | 51.2 | 933.2 |
| BP2 | GND | 51.2 | 807.2 |
| BP3 | DATA+ | 51.2 | 681.2 |
| BP4 | GND | 51.2 | 555.2 |
| BP5 | GND | 51.2 | 429.2 |
| BP6 | DATA- | 51.2 | 303.2 |
| BP7 | GND | 51.2 | 177.2 |
| BP8 | GND | 51.2 | 51.2 |
| BP9 | GND | 231.8 | -63.6 |
| BP10 | GND | 357.8 | -63.6 |
| BP11 | GND | 483.8 | -63.6 |
| BP12 | GND | 609.8 | -63.6 |
| BP13 | CLK+ | 769.4 | -63.6 |
| BP14 | GND | 895.4 | -63.6 |
| BP15 | GND | 1021.4 | -63.6 |
| BP16 | CLK- | 1147.4 | -63.6 |
| BP17 | GND | 1305.2 | -63.6 |
| BP18 | GND | 1431.2 | -63.6 |
| BP19 | GND | 1606.2 | -63.6 |
| BP20 | GND | 1732.2 | -63.6 |
| BP21 | GND | 1874 | -63.2 |
| BP22 | GND | 2028 | -43.8 |
| BP23 | GND | 2028 | 108.6 |
| BP24 | GND | 2028 | 234.6 |
| BP25 | OUT | 2028 | 574.8 |
| BP26 | GND | 2028 | 700.8 |
| BP27 | GND | 2028 | 856.2 |
| BP28 | GND | 2028 | 982.2 |
| BP29 | $\overline{\text{MODEN}}$ | 1953.8 | 1140.4 |
| BP30 | $\overline{\text{RTEN}}$ | 1827.8 | 1140.4 |
| BP31 | BIASSET | 1701.8 | 1140.4 |
| BP32 | MODSET | 1575.8 | 1140.4 |
| BP33 | $V_{EE}$ | 1449.8 | 1140.4 |
| BP34 | $V_{EE}$ | 1323.8 | 1140.4 |
| BP35 | $V_{EE}$ | 1197.8 | 1140.4 |
| BP36 | $V_{EE}$ | 1071.8 | 1140.4 |
| BP37 | $V_{EE}$ | 945.8 | 1140.4 |
| BP38 | $V_{EE}$ | 819.8 | 1140.4 |
| BP39 | $V_{EE}$ | 693.8 | 1140.4 |
| BP40 | $V_{EE}$ | 567.8 | 1140.4 |
| BP41 | $V_{EE}$ | 441.8 | 1140.4 |
| BP42 | PWC+ | 315.8 | 1140.4 |
| BP43 | PWC- | 189.8 | 1140.4 |
| BP44 | PLRT | 63.8 | 1140.4 |

## Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.