

## **10Gbps 1:16 Deserializer with Clock Recovery**

### ***General Description***

The MAX3953 is a 9.953Gbps/10.3125Gbps 1:16 deserializer with clock recovery for 10Gbps Ethernet and OC192 SONET applications. The integrated phase-locked loop (PLL) recovers a clock from the serial data input, and the data is then retimed and demultiplexed into 16 parallel LVDS outputs. Using Maxim's SiGe bipolar process, the MAX3953 can achieve 0.75UI of high-frequency jitter tolerance comprised of 0.50UI of deterministic jitter and 0.25UI of random jitter.

The MAX3953 includes TTL-compatible loss-of-lock (LOL) and sync-error (SYNC\_ERR) indicators that allow the user to verify that the part has locked on to incoming data. In case the incoming data becomes invalid, a clock holdover function is provided to maintain a valid reference clock to the upstream device. For proper operation, a reference clock of baud rate/64 or baud rate/16 is required.

The MAX3953 operates from a single +3.3V power supply and typically dissipates 1.5W. The operating temperature range is from 0°C to +85°C. The MAX3953 is available in a 68-pin QFN package.

## ***Applications***

10Gbps Ethernet LAN  
10Gbps Ethernet WAN  
Add/Drop Multiplexers  
Digital Cross-Connects

## Features

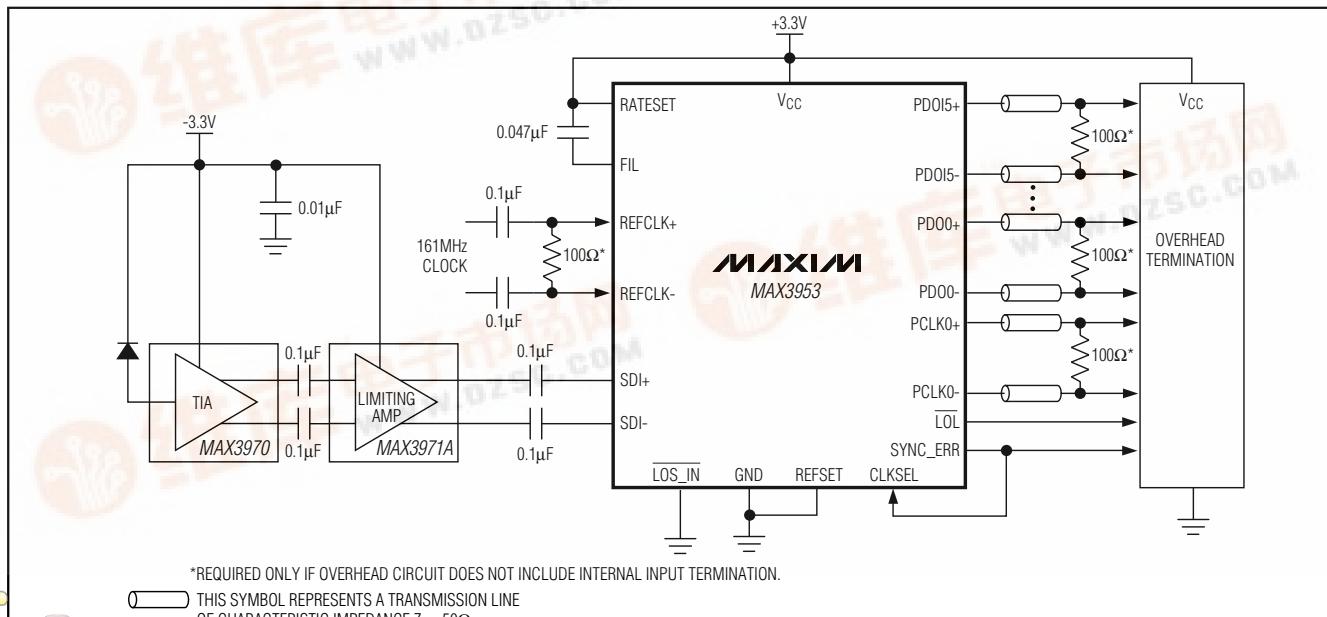
- ◆ Serial Data Rate: 9.953Gbps/10.3125Gbps
- ◆ Clock Recovery with 1:16 Demultiplexer
- ◆ 0.75UIP-P High-Frequency Jitter Tolerance
- ◆ 16-Bit Parallel LVDS Output
- ◆ OIF-Compliant Parallel Interface
- ◆ Loss-of-Lock (LOL) Indicator
- ◆ Differential Input Range: 100mVp-p to 1.2Vp-p
- ◆ Clock Holdover
- ◆ Reference Clock: Baud Rate/64 or Baud Rate/16
- ◆ Temperature Range: 0°C to +85°C
- ◆ 10mm × 10mm 68-Pin QFN Package

## **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
MAX3953UGK	0°C to +85°C	68 QFN (10mm x 10mm)

**Pin Configuration and Functional Diagram appear at end of data sheet.**

## **Typical Operating Circuit**



\*REQUIRED ONLY IF OVERHEAD CIRCUIT DOES NOT INCLUDE INTERNAL INPUT TERMINATION.

**0** THIS SYMBOL REPRESENTS A TRANSMISSION LINE  
OF CHARACTERISTIC IMPEDANCE  $Z_0 = 50\Omega$ .

# 10Gbps 1:16 Deserializer with Clock Recovery

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +5.0V  
 Input Voltage Levels  
     ( $SDI_+$ ,  $SDI_-$ ) ..... ( $V_{CC}$  - 1.0V) to ( $V_{CC}$  + 0.5V)  
 LVDS Output Voltage Levels  
     ( $PDO[15..0]^\pm$ ,  $PCLKO_+$ ,  $PCLKO_-$ ) ..... -0.5V to ( $V_{CC}$  + 0.5V)  
 Voltage at  $\overline{LOL}$ ,  $SYNC\_ERR$ ,  $RATESET$ ,  $CLKSEL$ ,  $REFCLK_+$ ,  
      $REFCLK_-$ ,  $REFSET$ ,  $LOS\_IN$ ,  $FIL$  ..... -0.5V to ( $V_{CC}$  + 0.5V)

Continuous Power Dissipation ( $T_A = 85^\circ C$ )  
     68-Lead QFN (derate 30.3mW/ $^\circ C$  above  $+85^\circ C$ ) ..... 2.5W  
 Operating Temperature Range .....  $0^\circ C$  to  $+85^\circ C$   
 Storage Temperature Range .....  $-55^\circ C$  to  $+150^\circ C$   
 Lead Temperature (soldering, 10s) .....  $+300^\circ C$   
 Processing Temperature (die) .....  $+400^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $T_A = 0^\circ C$  to  $+85^\circ C$ . Typical values are at  $+3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Supply Current	$I_{CC}$		476	580	600	mA
<b>INPUT SPECIFICATION (SDI+, SDI-) Figure 1</b>						
Differential Input Voltage	$V_{ID}$	AC-coupled or DC-coupled input	100	1200	1500	mVp-p
Common-Mode Input Range		DC-coupled	$V_{CC} - 0.3$	$V_{CC}$	$V_{CC}$	V
Input Termination to $V_{CC}$	$R_{IN}$		40	50	60	$\Omega$
<b>REFERENCE CLOCK INPUT (REFCLK+, REFCLK-) (Note 1)</b>						
Differential Input Voltage		AC-coupled or DC-coupled input	300	1600	1800	mVp-p
LVPECL Input High Voltage			$V_{CC} - 1.16$	$V_{CC} - 0.88$	$V_{CC} - 0.5$	V
LVPECL Input Low Voltage			$V_{CC} - 1.81$	$V_{CC} - 1.48$	$V_{CC} - 1.0$	V
LVPECL Input Bias Voltage			$V_{CC} - 1.3$	$V_{CC} - 0.88$	$V_{CC} - 0.5$	V
Differential Input Impedance			2.6	3.0	3.5	$k\Omega$
<b>OUTPUT SPECIFICATION (PDO[15..0]±, PCLKO±)</b>						
LVDS Output High Voltage	$V_{OHD}$			1.475	1.5	V
LVDS Output Low Voltage	$V_{OLD}$		0.925	0.9	0.85	V
LVDS Differential Output Voltage	$ V_{OD} $		250	400	500	mV
LVDS Change in Magnitude of Differential Output for Complementary States	$ \Delta V_{OD} $			25	30	mV
LVDS Offset Output Voltage	$V_{OD}$		1.125	1.275	1.4	V
LVDS Change in Magnitude of Output Offset Voltage for Complementary States	$ \Delta V_{OD} $			25	30	mV
LVDS Differential Output Impedance			80	140	200	$\Omega$
LVDS Output Current		Short together or short to GND		20	30	mA

# 10Gbps 1:16 Deserializer with Clock Recovery

## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $T_A = 0^\circ C$  to  $+85^\circ C$ . Typical values are at  $+3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LVTTL INPUT AND OUTPUT (CLKSEL, SYN_ERR, RATESET, LOS_IN, LOL, REFSET)</b>						
LVTTL Input High Voltage	$V_{IH}$		2			V
LVTTL Input Low Voltage	$V_{IL}$				0.8	V
LVTTL Input Current			-50	+6		$\mu A$
LVTTL Output High Voltage	$V_{OH}$	$I_{OH} = 20\mu A$	2.4		$V_{CC}$	V
LVTTL Output Low Voltage	$V_{OL}$	$I_{OL} = 1mA$			0.4	V

**Note 1:** Reference clock duty cycle can range from 30% to 70%.

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $T_A = 0^\circ C$  to  $+85^\circ C$ . Typical values are at  $+3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Input Data Rate		RATESET = GND	9.953			Gbps
		RATESET = $V_{CC}$	10.3125			
Sinusoidal Jitter Tolerance		$f = 400kHz$ (Notes 3, 4)	1.5			UIp-P
		$f = 4MHz$ (Note 3)	0.15			
Tolerated Consecutive Identical Digits		Bit-error ratio (BER) = $10^{-12}$	2000			Bits
Input Return Loss		$f < 10GHz$ , differential	10			dB
		$f < 15GHz$ , differential	8			
		$f < 15GHz$ , common mode	9			
Frequency Difference when PLL Indicates Out of Lock			1000			ppm
Frequency Difference when PLL Indicates In Lock			500			ppm
LOL Assert Time		No transitions at input, Figure 2	30	100		$\mu s$
PLL Acquisition Time		Valid transitions at input, Figure 2		100		$\mu s$
Maximum PCLK0 Deviation from REFCLK				2500		ppm
Output Clock to Data Delay	$t_{CLK-Q}$	Figure 3	-150	+150		ps
Output Clock Duty Cycle			45	50	55	%

# 10Gbps 1:16 Deserializer with Clock Recovery

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $T_A = 0^\circ C$  to  $+85^\circ C$ . Typical values are at  $+3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Clock and Data Rise/Fall Time	$t_R, t_F$	20% to 80%	100	250	250	ps
LVDS Differential Skew	$t_{SKW1}$	Any differential pair		50	50	ps
LVDS Channel-to-Channel Skew	$t_{SKW2}$	$PDO[15..0]\pm$		100	100	ps

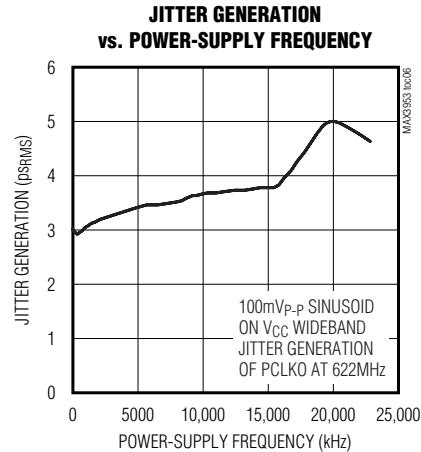
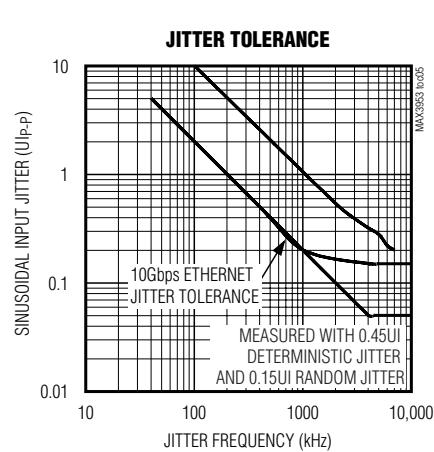
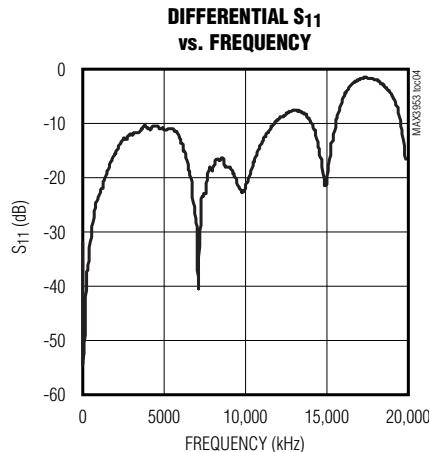
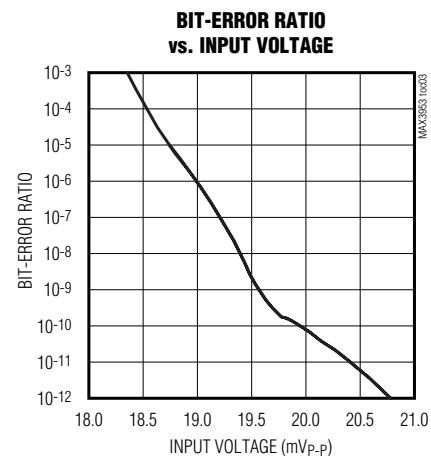
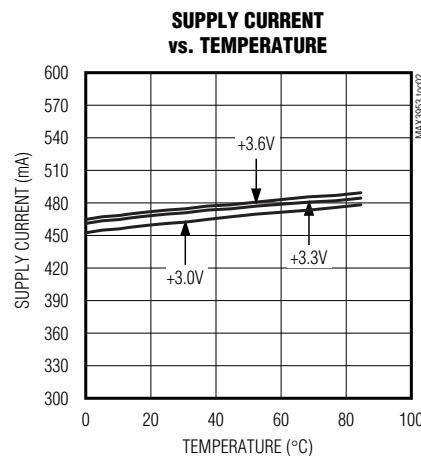
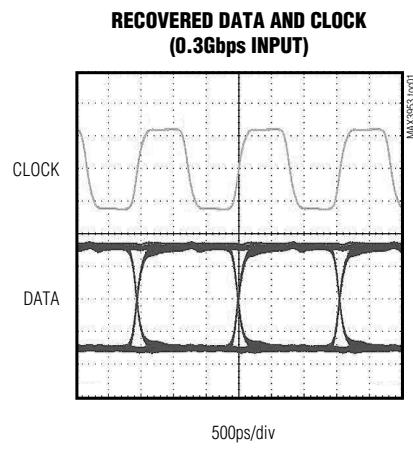
**Note 2:** Guaranteed by design and characterization for  $T_A = 0^\circ C$  to  $+85^\circ C$ .

**Note 3:** Measured with 0.45UIp-P deterministic jitter and 0.15UIp-P random jitter, on top of the specified sinusoidal jitter in a 2<sup>31</sup> - 1 PRBS pattern with a BER =  $10^{-12}$ .

**Note 4:** The jitter tolerance exceeds IEEE 802.3AE specifications. The jitter tolerance outperforms the instrument's measurement capability.

## Typical Operating Characteristics

( $T_A = +25^\circ C$ , unless otherwise noted.)



# 10Gbps 1:16 Deserializer with Clock Recovery

MAX3953

## Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 6, 14, 17, 18, 34, 35, 51, 52, 60, 68	GND	Ground
2	REFCLK+	Positive Reference Clock Input, LVPECL. Connect a baud rate/64 or baud rate/16 reference clock.
3	REFCLK-	Negative Reference Clock Input, LVPECL. Connect a baud rate/64 or baud rate/16 reference clock.
7	REFSET	Reference Clock Select Input, TTL. When the reference clock is baud rate/64, set REFSET to GND. When the reference clock is baud rate/16, set REFSET to VCC.
8, 11, 12, 13, 15, 16, 27, 42, 59, 66	VCC	+3.3V Supply Voltage
9	SDI+	Positive Serial Data Input, CML. 9.953Gbps/10.3125Gbps serial data stream.
10	SDI-	Negative Serial Data Input, CML. 9.953Gbps/10.3125Gbps serial data stream.
19	LOS_IN	Loss-of-Signal Input, TTL. The <u>LOS_IN</u> is an external input. Clock holdover is activated when <u>LOS_IN</u> is TTL low. Connect to VCC if <u>LOS</u> input is not available. See the <i>Clock Holdover Mode</i> section.
20	LOL	Loss-of-Lock Indicator Output, TTL. <u>LOL</u> signals a TTL low when the VCO frequency is more than 1000ppm from the reference clock frequency. <u>LOL</u> signals a TTL high when the VCO frequency is within 500ppm of the reference clock frequency. See the <i>Clock Holdover Mode</i> section.
21	PCLKO+	Positive Parallel Clock Output, LVDS
22	PCLKO-	Negative Parallel Clock Output, LVDS
23, 25, 28, 30, 32, 36, 38, 40, 43, 45, 47, 53, 55, 57, 61, 63	PDO15+ to PDO0+	Positive Parallel Data Outputs, LVDS
24, 26, 29, 31, 33, 37, 39, 41, 44, 46, 48, 54, 56, 58, 62, 64	PDO15- to PDO0-	Negative Parallel Data Outputs, LVDS
49	SYNC_ERR	Synchronization Error Output, TTL. SYNC_ERR is intended to drive CLKSEL for holdover mode. See the <i>Clock Holdover Mode</i> section.
50	CLKSEL	Output Clock Selector, TTL. CLKSEL is the control input for clock holdover. When CLKSEL = GND, PCLKO is derived from the input data. When CLKSEL = VCC, PCLKO is derived from the reference clock.
65	RATESET	Serial Data Rate Select Input, TTL. When the input serial data stream is 9.953Gbps, set RATESET to GND. When the input serial data stream is 10.312Gbps, set RATESET to VCC.
67	FIL	PLL Loop Filter Capacitor Input. A capacitor between this pin and VCC sets the loop to zero. A 0.047 $\mu$ F capacitor is recommended.
EP	Exposed Pad	Ground. This must be soldered to the circuit board ground for proper thermal and electrical performance. See the <i>Layout Considerations</i> section.

# 10Gbps 1:16 Deserializer with Clock Recovery

## Detailed Description

The MAX3953 deserializer with clock recovery converts 9.953Gbps/10.3125Gbps serial data into 16-bit wide, 622Mbps/644Mbps parallel data. The device combines a fully integrated phase-locked loop (PLL), TTL-compatible status monitors, input amplifier, data retiming block, 16-bit demultiplexer, clock dividers, and LVDS output buffers. The PLL consists of a phase/frequency detector (PFD), a loop filter, and voltage-controlled oscillator (VCO). The PLL recovers the serial clock from the input data stream and retimes the data. The demultiplexer generates a 16-bit-wide 622Mbps/644Mbps parallel data output. The MAX3953 is designed to deliver the best jitter performance by using differential signal architecture and low-noise design techniques.

### Input Amplifier

The serial data input (SDI) amplifier accepts differential input amplitudes from 100mVp-P to 1200mVp-P.

### Phase-Frequency Detector

The digital phase-frequency detector (PFD) aids frequency acquisition during startup conditions. Depending on the polarity of the frequency input difference between REFCLK and the VCO clock, the PFD drives the VCO until the frequency difference is reduced to zero. False locking is eliminated by this digital phase-frequency detector.

The data phase detector is optimized to achieve 0.75UI high-frequency jitter tolerance.

### Loop Filter and VCO

The phase detector and frequency detector outputs are summed into the loop filter. A  $0.047\mu\text{F}$  capacitor ( $C_F$ ) is required to set the PLL damping ratio. The loop filter output controls the on-chip VCO.

### Loss-of-Lock Monitor

A loss-of-lock (LOL) monitor is included in the MAX3953 frequency detector. A loss-of-lock condition is signaled with a TTL low. When the PLL is frequency locked, LOL switches to TTL high in approximately 56 $\mu\text{s}$ .

LOL signals a TTL low when the VCO frequency is more than 1000ppm from the reference clock frequency. LOL signals a TTL high when the VCO frequency is within 500ppm of the reference clock frequency.

### Low-Voltage Differential Signal (LVDS) Outputs

The MAX3953 features LVDS outputs for interfacing with high-speed circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 500mVp-P to 800mVp-P differential low-voltage swings to achieve fast transition times, minimize power dissipation, and improve noise immunity.

## Applications Information

### Clock Holdover Mode

The clock holdover mode is designed to provide an accurate parallel clock in the event of a loss-of-lock (LOL) or loss-of-signal (LOS) condition. The activation of the holdover mode is controlled by the SYNC\_ERR, LOS\_IN, and CLKSEL pins. CLKSEL is an input signal used to select the VCO to lock on to the incoming data (SDI) or the reference clock (REFCLK). The architecture of the holdover mode is shown in Figure 4. Holdover mode is activated by connecting SYNC\_ERR to CLKSEL.

### Consecutive Identical Digits (CIDs)

The MAX3953 has a low phase and frequency drift in the absence of data transitions. As a result, long runs of consecutive zeros and ones can be tolerated while maintaining a BER of  $1 \times 10^{-12}$ . The CID tolerance is tested using a  $2^{13} - 1$  pseudorandom bit stream (PRBS), substituting a long run of zeros to simulate worst case. A CID tolerance of greater than 2,000 bits is typical.

### Exposed-Pad Package

The exposed pad, 68-pin QFN incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The pad is electrical ground on the MAX3953 and should be soldered to the circuit board for proper thermal and electrical performance. See Maxim Application Note HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages* for further information.

### Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3953 high-speed inputs and outputs. Power-supply decoupling should be placed as close to the  $V_{CC}$  as possible. To reduce feed-through, isolate input signals from output signals.

## 10Gbps 1:16 Deserializer with Clock Recovery

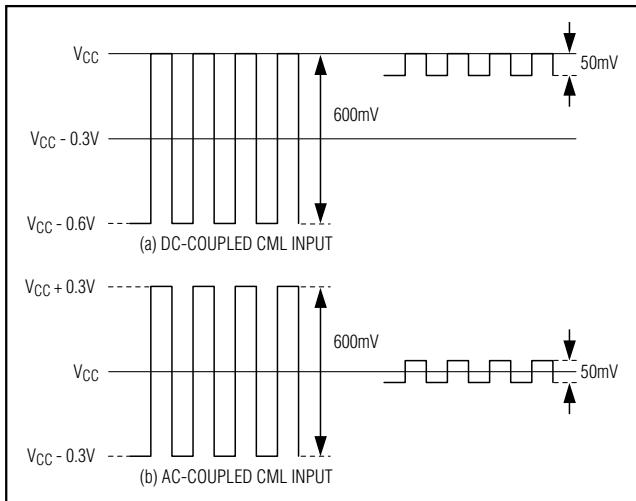


Figure 1. Input Amplitude

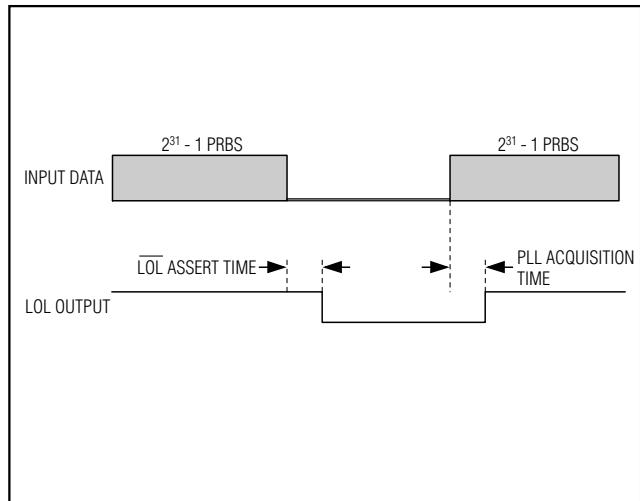


Figure 2.  $\overline{LOL}$  Assert and Acquisition Time

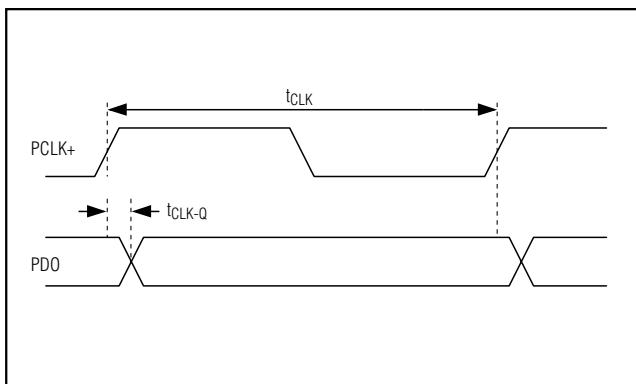


Figure 3. Timing Parameters

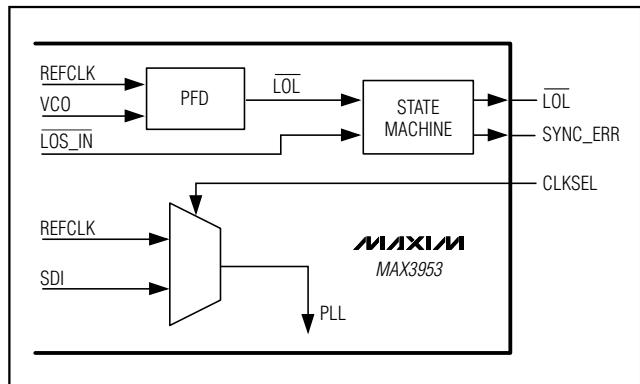
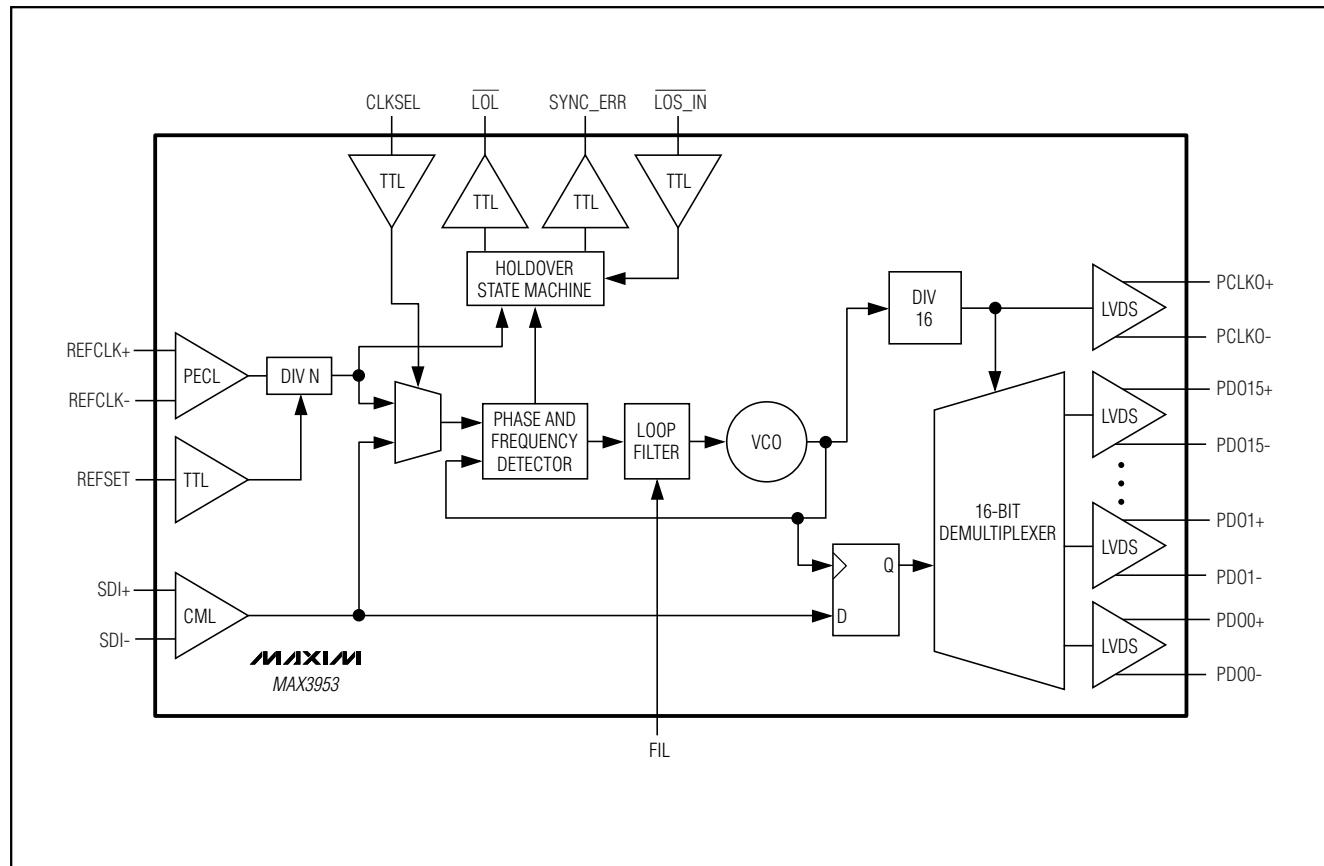


Figure 4. Clock Holdover Architecture

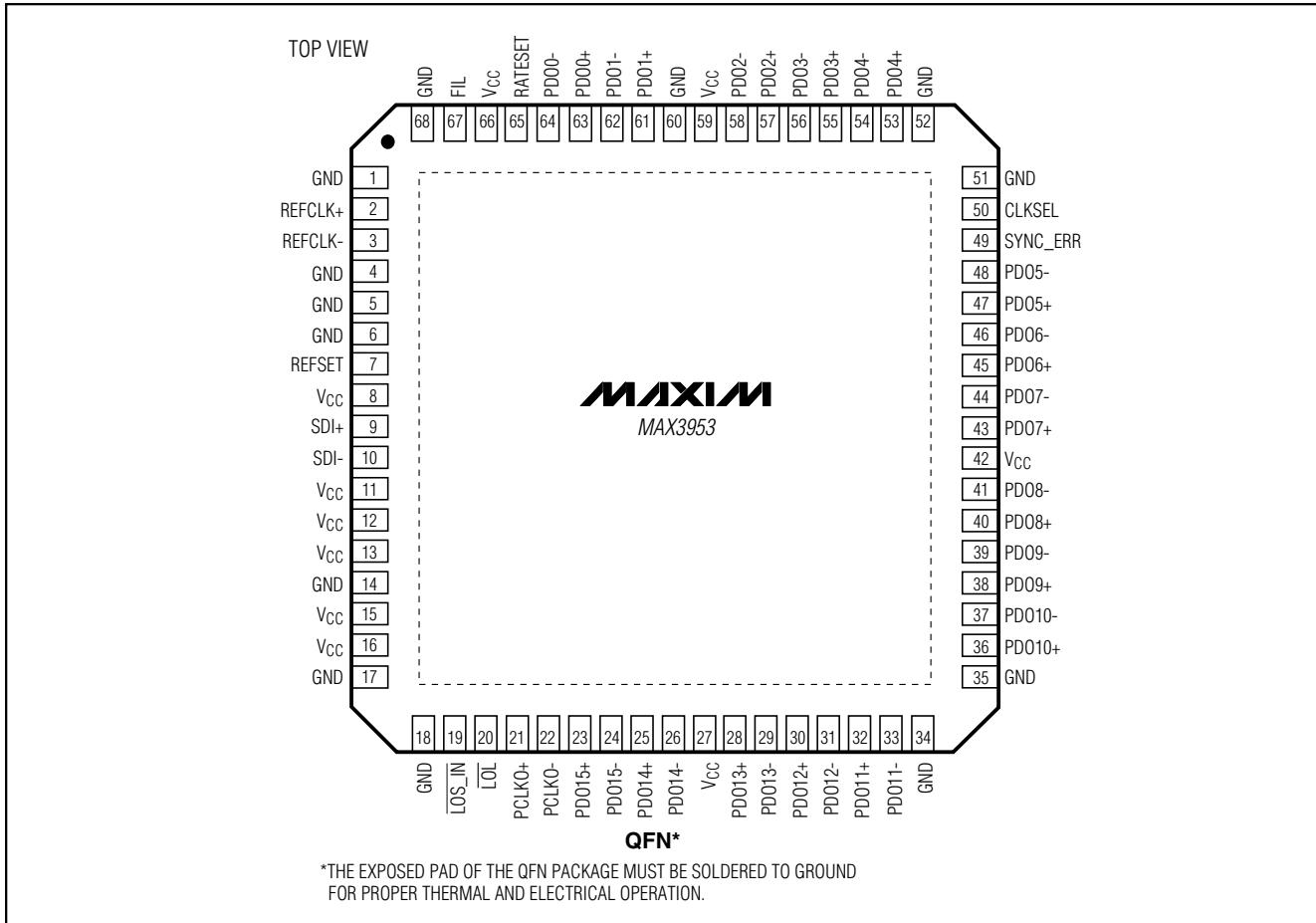
## 10Gbps 1:16 Deserializer with Clock Recovery

Functional Diagram



## **10Gbps 1:16 Deserializer with Clock Recovery**

## Pin Configuration



# MAX3953

## **Chip Information**

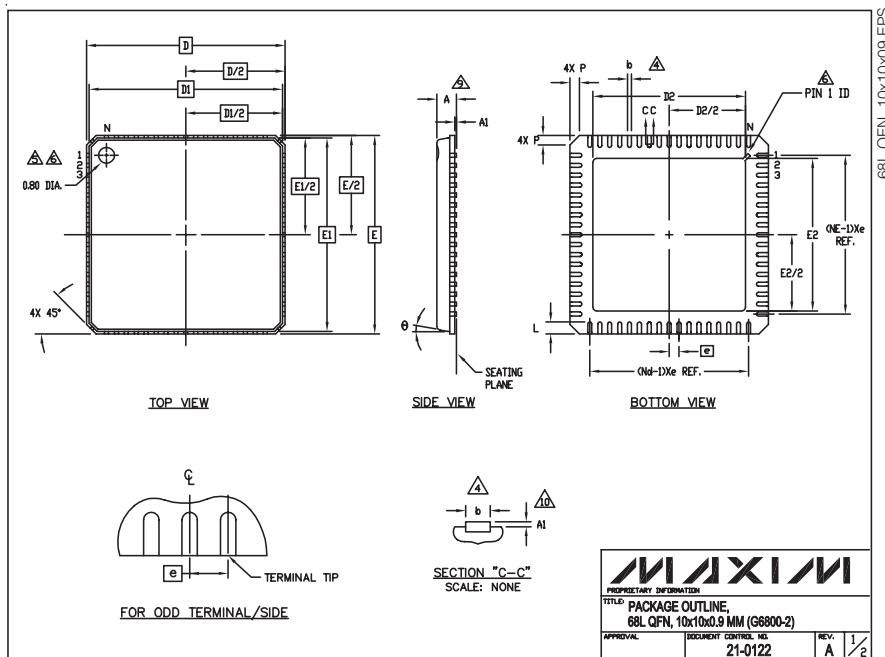
TRANSISTOR COUNT: 11,612

## PROCESS: SiGe BIPOLAR

# 10Gbps 1:16 Deserializer with Clock Recovery

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



COMMON DIMENSIONS		
	MIN.	NOM.
		MAX.
A	—	0.90
A1	0.00	0.01
b	0.18	0.23
D	10.00 BSC	
D1	9.75 BSC	
E	0.50 BSC	
E1	10.00 BSC	
L	0.50	0.60
N	68	3
Nd	17	3
Ne	17	3
θ	0	12°
P	0	0.42
D2	4.40	7.70
E2	4.40	7.70
		7.85

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
4. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
5. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. PACKAGE WARPAGE MAX 0.10mm.
10. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS.
11. APPLIES ONLY TO TERMINALS.



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

10 **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**