19-2405; Rev 0; 4/02

MAXIM

10Gbps 16:1 Serializer

General Description

The MAX3952 16:1 serializer is optimized for 10.3Gbps and 9.95Gbps Ethernet applications. A serial clock output is provided for retiming the data at the latch input of the laser driver. Both the high-speed data and clock are CML outputs. The serializer operates from a single +3.3V supply, consuming only 1.15W typical power.

The clock multiplier reference clock frequency can be either 1/16 or 1/64 the serial output clock rate. A FIFO aligns the phase between the parallel clock input and the internally synthesized clock. In addition, a 1/16 counterdirectional clock output (LVDS) is provided for use as the clock signal of the XAUI codec IC or framer.

The operating temperature range is from -40°C to +85°C. The MAX3952 is available in a 10mm × 10mm 68-pin QFN package.

Applications

10Gbps Ethernet LAN

10Gbps Ethernet WAN

Features

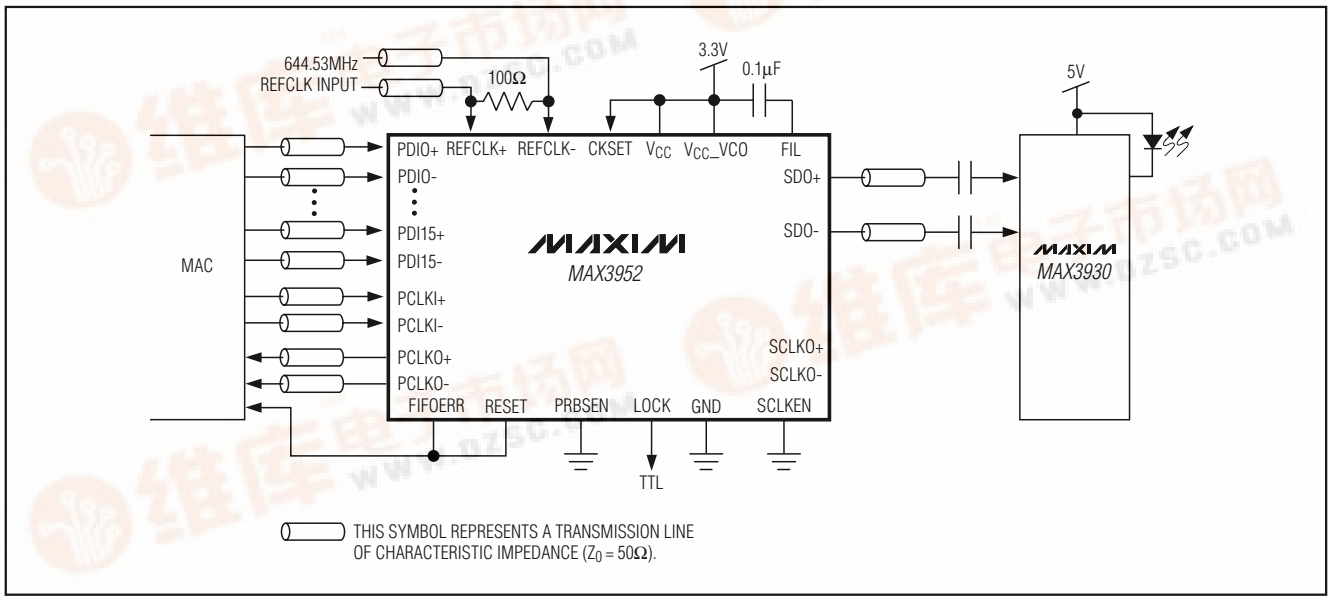
- ♦ Operates at 9.953Gbps and 10.3125Gbps
- ♦ 16-Bit LVDS Interface
- ♦ Single +3.3V Supply
- ♦ 1.15W Power Dissipation
- ♦ LVDS Source Clock Output
- ♦ Built-In 2^7 - 1 PRBS Pattern Generator
- ♦ Deterministic Jitter: 9ps (max) at 0°C to +85°C
- ♦ Operating Temperature Range: -40°C to +85°C
- ♦ 68-Pin QFN Package (10mm × 10mm)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3952EGK	-40°C to +85°C	68 QFN

Pin Configuration appears at end of data sheet.

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

Power Supply (V_{CC}).....-0.5 to +5V
CML Output Current (SDO±, SCLKO±).....22mA
LVDS Input Voltage Levels
(PDI_±, PCLKI±).....-0.5V to (V_{CC} + 0.5V)
LVDS Output Voltage (PCLKO±).....-0.5V to (V_{CC} + 0.5V)

Continuous Power Dissipation (T_A = +85°C)
QFN (derate 30.3mW/°C above 70°C).....2424mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Voltage Levels at FIL, RESET, CKSET.....-0.5V to (V_{CC} + 0.5V)
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, differential LVDS load = 100Ω, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 1)		350	500	mA
LVDS INPUT SPECIFICATIONS (PDI±[15…0], PCLKI±)						
Input Voltage Range	V_I		0		2400	mV
Differential Input Voltage	$\|V_{ID}\|$		100			mV
Input Common-Mode Current		Input, V_{OS} = 1.2V		100		µA
Threshold Hysteresis				70		mV
Differential Input Impedance	R_{IN}		85	100	115	Ω
LVDS OUTPUT SPECIFICATIONS (PCLKO±)						
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\|V_{OD}\|$		250		400	mV
Change in Magnitude of Differential Outputs for Complementary Inputs	$\Delta\|V_{OD}\|$				25	mV
Offset Output Voltage			1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\|V_{OS}\|$				25	mV
Differential Output Impedance			80		140	Ω
Output Current		Short together			12	mA
		Short to ground			40	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, differential LVDS load = 100Ω, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CML OUTPUT SPECIFICATIONS (SDO±, SCLKO±)						
Differential Output		R_L = 50Ω to V_{CC}	640	800	1000	mV_{P-P}
Differential Output Impedance			85	100	115	Ω
Output Common-Mode Voltage		R_L = 50Ω to V_{CC}		V_{CC} - 0.2		V
LVTTL SPECIFICATIONS (RESET, FIFO_ERROR, LOCK, PRBSEN)						
LVTTL Input High Voltage	V_{IH}		2.0			V
LVTTL Input Low Voltage	V_{IL}				0.8	V
LVTTL Input High Current	I_{IH}		-28		10	µA
LVTTL Input Low Current	I_{IL}		-50		10	µA
LVTTL Output High Voltage	V_{OH}	I_{OH} = 20µA	2.4		V_{CC}	V
LVTTL Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.4	V
LVPECL INPUT SPECIFICATIONS (REFCLK±)						
LVPECL Input High Voltage	V_{IH}		V_{CC} - 1.16		V_{CC} - 0.88	V
LVPECL Input Low Voltage	V_{IL}		V_{CC} - 1.81		V_{CC} - 1.48	V
LVPECL Input Bias Voltage				V_{CC} - 1.3		V
LVPECL Single-Ended Impedance				1.4		kΩ
LVPECL Differential Input Voltage Swing			300		1900	mV_{P-P}

Note 1: CML outputs AC-coupled to 100Ω differential load, PRBSEN = GND, and SCLKEN = GND.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, differential LVDS and CML load = 100Ω, T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tx DATA INPUT SPECIFICATIONS (PDI±[15…0], PCLKI±)						
Parallel Input Setup Time	t_{SU}	(Figure 1)			200	ps
Parallel Input Hold Time	t_H	(Figure 1)			200	ps
Tx SOURCE CLOCK OUTPUT SPECIFICATIONS (PCLKO±)						
Parallel Clock Output Rise/Fall Time	t_r, t_f	20% to 80%		100	250	ps
Parallel Clock Output Duty Cycle			45		55	%
SERIAL DATA OUTPUT SPECIFICATIONS (SDO±, SCLKO±)						
Bit-Error Rate				1×10^{-12}		
Serial Data Output Rise/Fall Time	t_r, t_f	20% to 80%			28	ps
Serial Output Clock-to-Data Delay	t_{CK-Q}	(Note 3)	-15		+15	ps
Serial Data or Clock Output Random Jitter	t_{RJ}				0.9	ps_{RMS}
Serial Data Output Deterministic Jitter	t_{DJ}	0°C to +85°C (Note 4)			9	ps_{P-P}
		-40°C to +85°C (Note 4)			15	
Serial Clock or Data Output Return Loss	RL = -20log|S_{22}|	100kHz to 10GHz		17		dB
		10GHz to 13GHz		10		
		13GHz to 15GHz		7		
Tx REFERENCE CLOCK INPUT SPECIFICATIONS (REFCLK±)						
Reference Clock Frequency Tolerance			-100		+100	ppm
Reference Clock Input Duty Cycle			30		70	%
RESET INPUT (RESET)						
Minimum Pulse Width of FIFO Reset		UI is PCLKO period		4		UI
Tolerated Drift Between PCLKI and PCLKO After Reset		UI is PCLKO period; drift is PCLKO crossing - PCLKI crossing	-1		+1	UI

Note 2: See Table 1 for valid operating clock frequencies. AC characteristics are guaranteed by design and characterization.

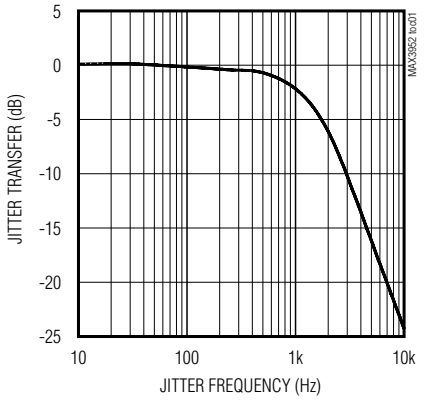
Note 3: Relative to the falling edge of the SCLKO.

Note 4: Deterministic jitter includes pattern-dependent jitter and pulse-width distortion. Measured with a pattern equivalent to 2^{23} - 1 PRBS.

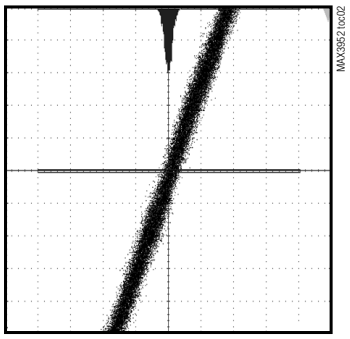
Typical Operating Characteristics

(T_A = +25°C, V_{CC} = +3.3V, unless otherwise noted.)

RCLKI TO SCLKO JITTER TRANSFER

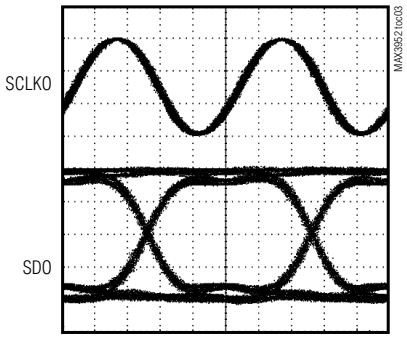


SERIAL CLOCK OUTPUT RANDOM JITTER

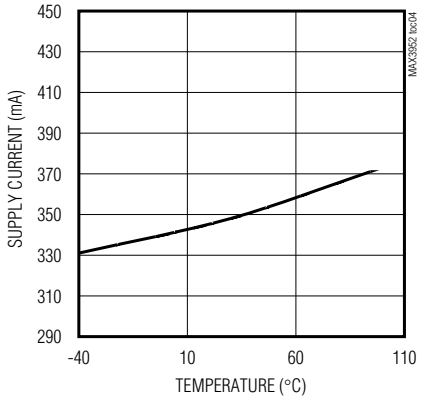


f_{REFCLK} = 155.52MHz, RANDOM JITTER = 513fs_{RMS}

SERIAL CLOCK AND DATA OUTPUTS



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 4, 5, 13, 17, 18, 26, 34, 35, 51, 52, 68	GND	Ground
2	REFCLK+	Positive Reference Clock Input, LVPECL
3	REFCLK-	Negative Reference Clock Input, LVPECL
6, 9, 12, 25, 43, 60	V_{CC}	Positive Power Supply
7	SCLKO-	Negative Serial Clock Output, CML. 9.95328GHz or 10.3125GHz
8	SCLKO+	Positive Serial Clock Output, CML. 9.95328GHz or 10.3125GHz
10	SDO-	Negative Serial Data Output, CML. 9.95328Gbps or 10.3125Gbps
11	SDO+	Positive Serial Data Output, CML. 9.95328Gbps or 10.3125Gbps
14	SCLKEN	Control Input for Disabling SCLKO Output: SCLKEN = GND ⇒ SCLKO Off SCLKEN = V_{CC} ⇒ SCLKO Active
15	PCLKO+	Positive Source Clock Output. LVDS, 622MHz or 644MHz. Clocks the MAC.
16	PCLKO-	Negative Source Clock Output. LVDS, 622MHz or 644MHz. Clocks the MAC.
19, 21, 23, 27, 29, 31, 36, 38, 40, 44, 46, 48, 54, 56, 58, 61	PDI15+ to PDI0+	Positive Parallel Data Inputs, LVDS. PDI15+ is MSB
20, 22, 24, 28, 30, 32, 37, 39, 41, 45, 47, 49, 55, 57, 59, 62	PDI15- to PDI0-	Negative Parallel Data Inputs, LVDS. PDI15- is MSB
33	RESET	16 x 4-Bit FIFO Reset Input, TTL, Active High
42	PRBSEN	PRBS Pattern Generator Enable Input, TTL, Active High
50	FIFO_ERROR	FIFO Error, TTL, Active High
53	LOCK	PLL Lock Indicator, TTL, Active High
63	PCLKI+	Positive Parallel Clock Input, LVDS
64	PCLKI-	Negative Parallel Clock Input, LVDS
65	CKSET	Reference Clock Programming Pin. Programming instructions in Table 1.
66	FIL	Filter Capacitor Input Pin
67	V_{CC}_VCO	Loop Filter and VCO Positive Power Supply

Detailed Description

The MAX3952 converts 16-bit-wide, 622Mbps/644Mbps data to 9.95Gbps/10.3Gbps serial data (Figures 3 and 4). Data is loaded into the 16:1 mux through a 16 x 4 FIFO buffer for wide tolerance to clock skew. Clock and data inputs are LVDS levels, and high-speed serial outputs are current-mode logic (CML). An internal PLL frequency synthesizer generates a serial clock from a low-speed reference clock.

Low-Voltage Differential-Signal Inputs and Outputs

The MAX3952 has LVDS inputs for interfacing with high-speed digital circuitry. This technology uses 250mV to 400mV differential low-voltage swings to achieve fast transition times, minimal power dissipation, and noise immunity. For proper operation, the parallel clock LVDS outputs (PCLKO±) require 100Ω differential DC terminations between the positive and negative outputs. Do not terminate these outputs to ground. The parallel data and parallel clock LVDS inputs (PDI_+, PDI_-, PCLKI+, PCLKI-) are internally terminated with a 100Ω differential input resistance and therefore do not require external termination.

LVPECL Inputs

The reference clock (REFCLK±) has LVPECL inputs for interfacing to a crystal oscillator using AC- or DC-coupling. The REFCLK± inputs are self-biasing to V_{CC} - 1.3V for AC-coupled inputs. Only a 100Ω differential termination resistance must be added when inputs are AC-coupled.

Current-Mode Logic Outputs

The high-speed data and clock outputs (SDO±, SCLKO±) of the MAX3952 are designed using CML. The CML outputs include internal 50Ω back termination to V_{CC}. These outputs are intended to drive a 50Ω transmission line terminated with a matched load impedance. For detailed instructions on how to interface with LVDS, PECL, and CML, refer to HFAN-01.0: *Introduction to LVDS, PECL, and CML.*

FIFO Buffer

Data is latched into the MAX3952 by the parallel input clock (PCLKI±). The parallel input clock is the FIFO write clock. The parallel output clock (PCLKO±) is the FIFO read clock that loads the 16:1 mux. The FIFO allows the read and write clock to vary by up to ±1UI (unit interval). This specification makes the MAX3952 noncompliant with the IEEE802.3ae standard, as this standard requires a tolerance of ±14UI. Conditions that result in the read and write clock accessing the same FIFO address are indicated by FIFO_ERROR. To clear this condition, assert RESET high for at least 4UI. FIFO_ERROR can be connected directly to the RESET input to clear timing errors. After reset, the full elastic range of the FIFO is available again.

Frequency Synthesizer

The PLL synthesizes a 9.95GHz/10.31GHz clock from an external reference clock. The PLL reference clock (REFCLK±) can be programmed as 622MHz/644MHz or 155MHz/161MHz using the CKSET pin. See Table 1 for CKSET settings. The parallel output clock (PCLKO±) is derived from the synthesizer and is SCLKO ÷ 16. A TTL-compatible loss-of-lock indicator (LOCK), asserts low when the VCO is unable to lock to the reference frequency. This pin can be used to directly drive an LED. If jitter on the REFCLK± input is present, an error with respect to the divided down SCLKO frequency of 500ppm will be indicated by a low state on LOCK.

Table 1. Setting REFCLK Frequency

REFERENCE CLOCK FREQUENCY (MHz)	CKSET PIN SETTING	SERIAL CLOCK FREQUENCY (GHz)
622.08	OPEN	9.95
644.53	V_{CC}	10.3
155.52	GND	9.95
161.13	30kΩ to GND	10.3

Internal Pattern Generator

The MAX3952 includes a SONET-compliant internal pattern generator capable of a 2^7 - 1 PRBS pattern. Connecting the PRBSEN pin to V_{CC} enables the pattern generator.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Use controlled impedance transmission lines to interface with the MAX3952 clock and data inputs and outputs. Give special consideration to filtering the V_{CC}_VCO pin; all other power supplies can be connected through a common filter.

Exposed Pad (EP) Package

The EP 68-pin QFN incorporates features that provide a very low thermal resistance path for heat removal from the IC to a PC board. The MAX3952's exposed paddle must be soldered directly to a ground plane with good thermal conductance. Refer to HFAN-08.1: *Thermal Considerations of QFN and Other Exposed-Paddle Packages.*

10Gbps 16:1 Serializer

Chip Information

TRANSISTOR COUNT:8400

PROCESS: SiGe bipolar

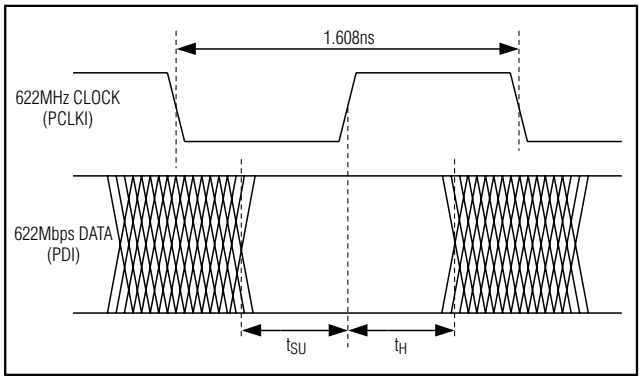


Figure 1. Setup and Hold Time

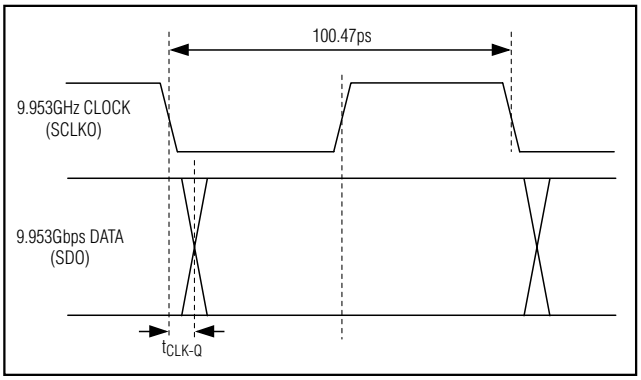


Figure 2. Definition of Clock to Q

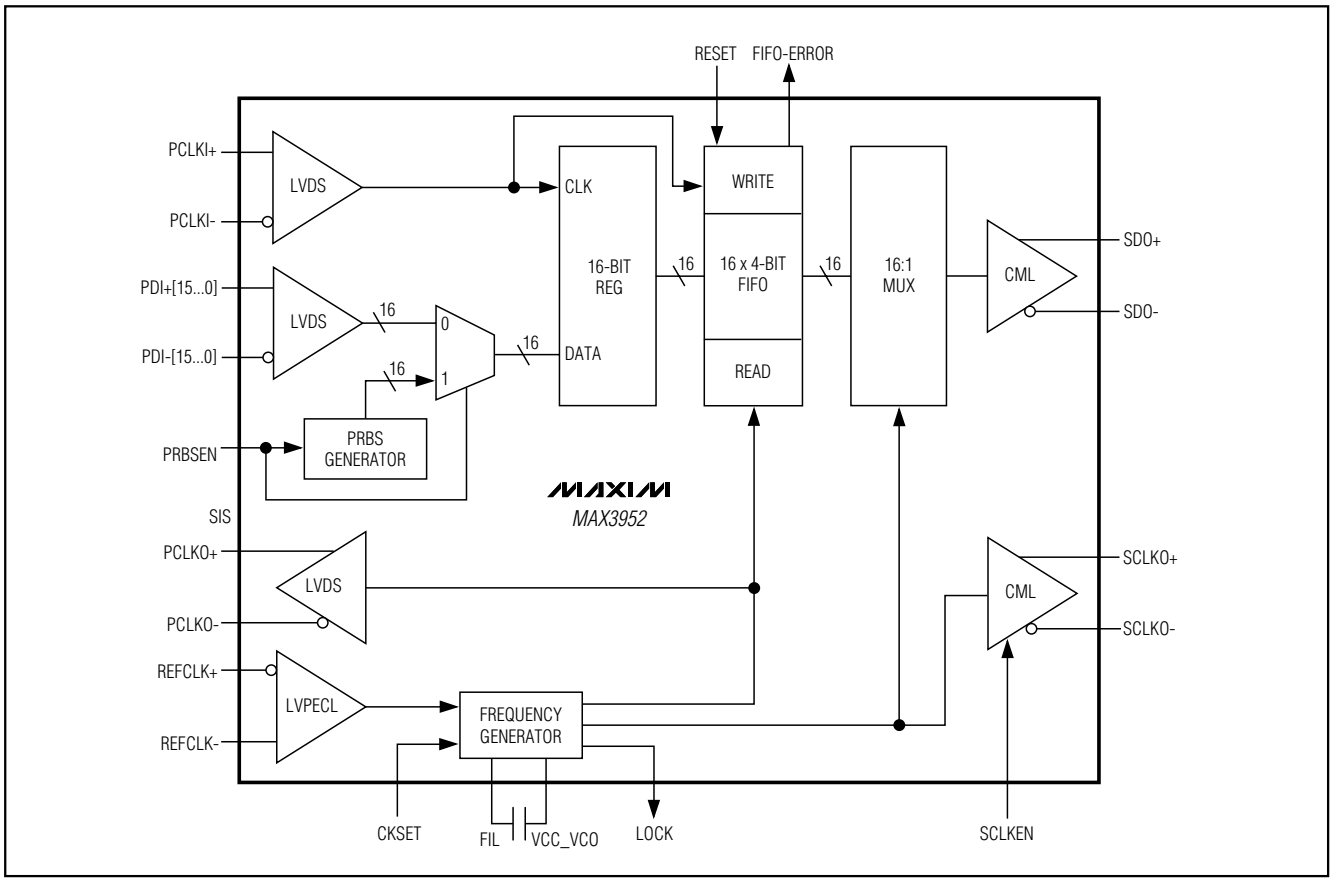
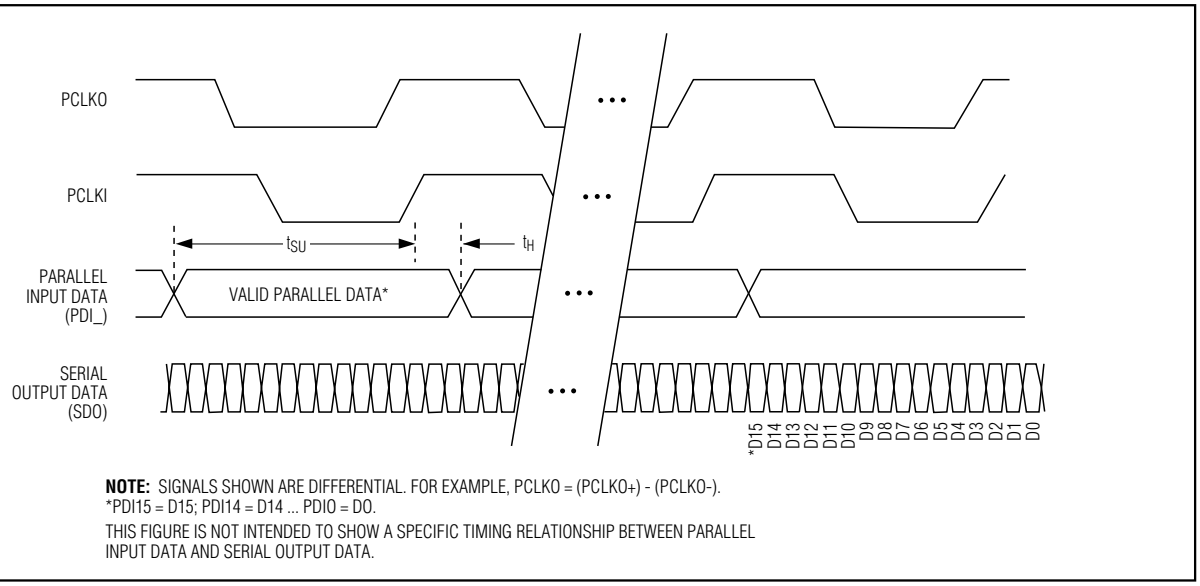


Figure 3. Functional Diagram

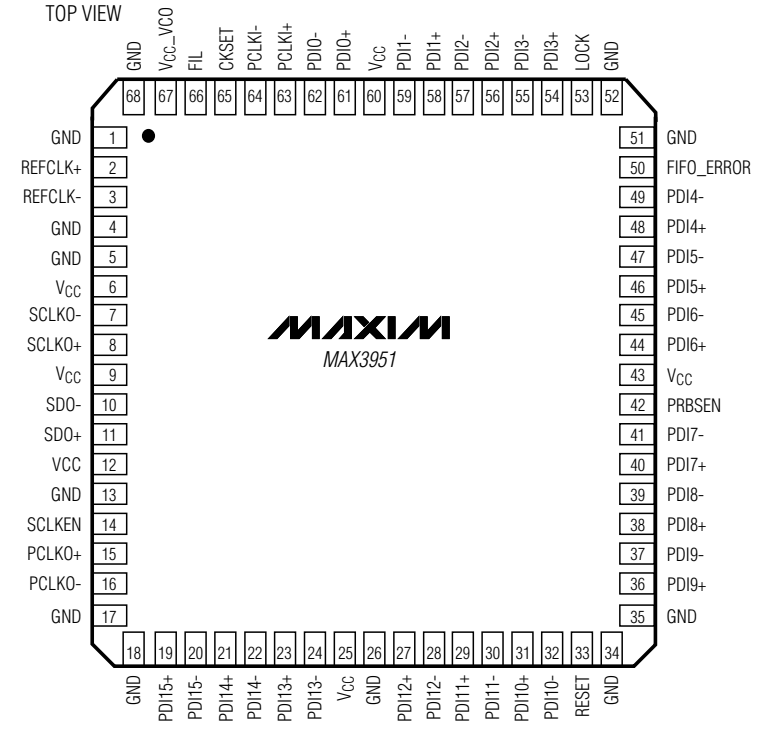


NOTE: SIGNALS SHOWN ARE DIFFERENTIAL. FOR EXAMPLE, PCLKO = (PCLKO+) - (PCLKO-).
*PDI15 = D15; PDI14 = D14 ... PDI0 = D0.

THIS FIGURE IS NOT INTENDED TO SHOW A SPECIFIC TIMING RELATIONSHIP BETWEEN PARALLEL INPUT DATA AND SERIAL OUTPUT DATA.

Figure 4. Parallel and Serial Data Timing

Pin Configuration

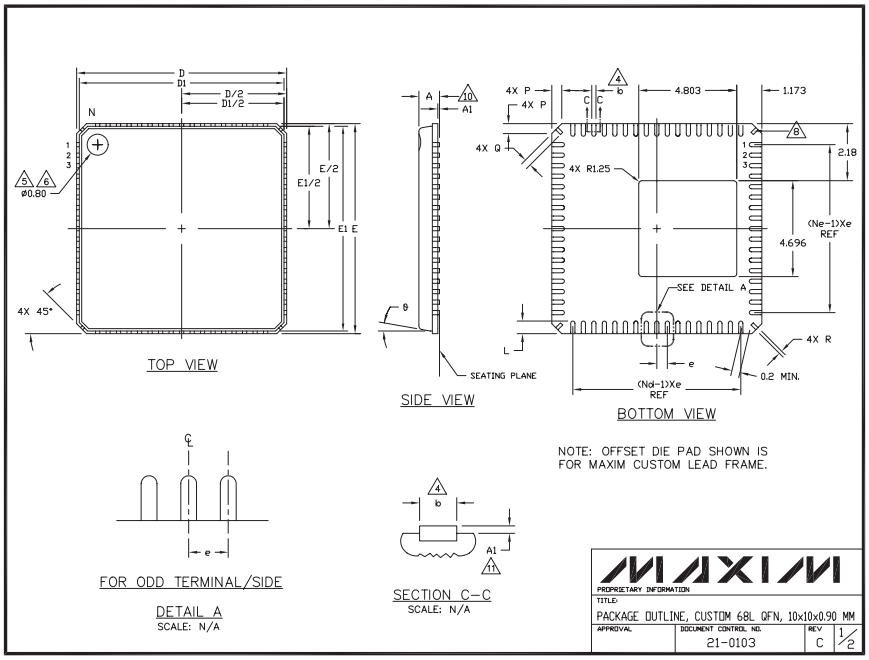


*EXPOSED PAD IS CONNECTED TO GND.

10Gbps 16:1 Serializer

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TERMINAL.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPES SHOWN AT FOUR CORNERS ARE CONNECTED TO DIE PAD.
9. PACKAGE WARPAGE MAX 0.10mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
11. APPLIED ONLY FOR TERMINALS.
12. CUSTOM LEAD FRAME WITH OFFSET DIE PAD: REFER TO MAXIM 24-0718 (G6800-1F).

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00BSC		
D1		9.75BSC		
E		10.00BSC		
E1		9.75BSC		
N		68		3
Nd		17		3
Ne		17		3
e		0.50 BSC		
L	0.50	0.60	0.75	
θ			12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	
R	0.13	0.17	0.23	

PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, CUSTOM 68L QFN, 10x10x0.90 MM
APPROVAL
DOCUMENT CONTROL NO.
21-0103
REV
C
2/2