19-2269; Rev 2; 6/03

EVALUATION KIT AVAILABLE

+3.3V, 2.5Gbps Low-Power Limiting Amplifiers

General Description

The MAX3272/MAX3272A 2.5Gbps limiting amplifiers accept a wide range of input voltages and provide a constant-level output voltage with controlled edge speeds. Additional features include power detectors with programmable loss-of-signal (LOS) indication, an optional squelch function that mutes the data output signal when the input voltage falls below a programmable threshold, and an output polarity selector. These parts exhibit excellent jitter performance and have low power dissipation.

The MAX3272/MAX3272A feature current-mode logic (CML) data outputs that are tolerant of inductive connectors, and are available in a 4mm × 4mm QFN package or in die form (MAX3272 only). Along with the MAX3271, the MAX3272/MAX3272A are ideal for low-power, compact optical receivers.

Applications

Gigabit Ethernet Optical Receivers
Fibre Channel Optical Receivers
System Interconnects
2.5Gbps Optical Receivers
SONET/SDH Receivers

Features

- Single +3.3V Power Supply
- 33mA Supply Current
- 5ps Deterministic Jitter
- 90ps Edge Speed
- Output Squelch Function
- Programmable Loss-of-Signal Function
- CML Output Interface
- 20-Pin 4mm × 4mm QFN Package
- Selectable Output Polarity

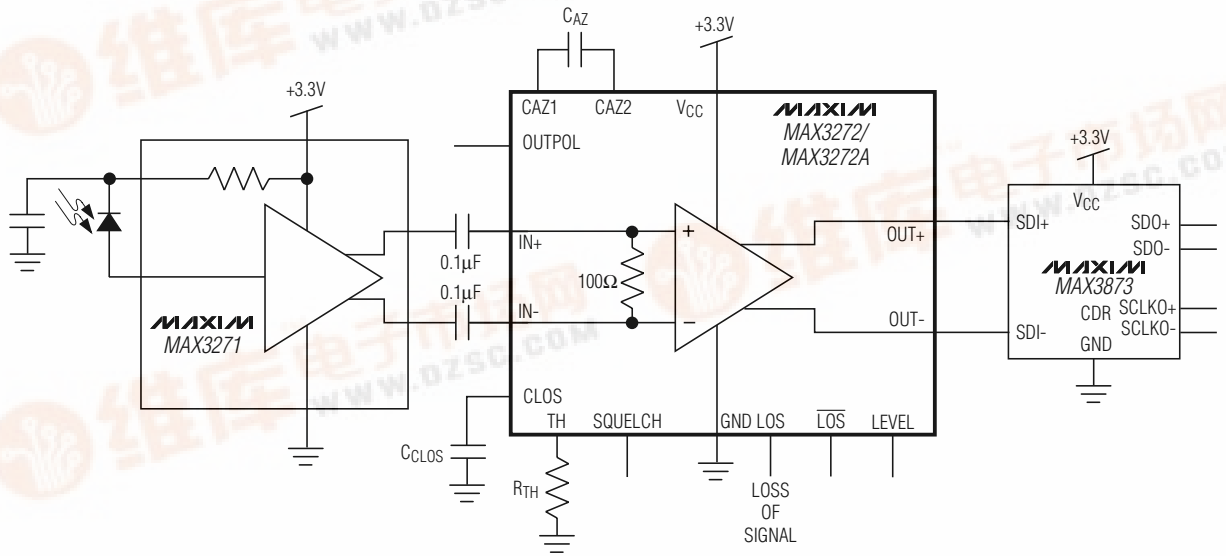
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PACKAGE CODE
MAX3272EGP	-40°C to +85°C	20 QFN	G2044-3
MAX3272E/D	-40°C to +85°C	20 QFN	Dice*
MAX3272AEGP	-40°C to +85°C	20 QFN	G2044-3

*Dice are designed and guaranteed to operate from -40°C to +85°C, but are tested only at T_A = +25°C.

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



Typical Operating Circuits continue at end of data sheet.

+3.3V, 2.5Gbps Low-Power Limiting Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) .....-0.5V to +6.0V
Voltage at IN+, IN- .....(V_{CC} - 2.4V) to (V_{CC} + 0.5V)
Voltage at SQUELCH, CAZ1, CAZ2, TH, CLOS .....-0.5V to (V_{CC} + 0.5V)
Voltage at LOS, $\overline{LOS}$ (MAX3272).....-0.5V to +6.0V
Voltage at LOS, $\overline{LOS}$ (MAX3272A) .....-0.5V to (V_{CC} + 0.5V)
Voltage at LEVEL.....-0.5V to +2.0V
Voltage at OUTPOL.....-0.5V to +6.0V
Current into LOS, $\overline{LOS}$ .....-1mA to +9mA
Differential Input Voltage (IN+ - IN-).....2.5V_{P-P}
Continuous Current at IN+, IN- 50mA
Continuous Current at CML Outputs (OUT+, OUT-) .....-25mA to +25mA
Continuous Power Dissipation 1600mW
Storage Ambient Temperature Range (T_{STG}).....-55°C to +150°C
Operating Junction Temperature Range (T_J) .....-55°C to +150°C
Die Attach Temperature.....+400°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 2)			33	44	mA
Input Data Rate					2.5		Gbps
Input Voltage Range	V_{IN}	Differential		15		1200	mV_{P-P}
Output Deterministic Jitter		(Notes 3, 4, 5)			5	27	ps_{P-P}
Random Jitter		(Notes 4, 6)			3		ps_{RMS}
Data Output Edge Speed (20% to 80%)		(Notes 3, 4)	$15mV_{P-P} < V_{IN} \le 30mV_{P-P}$		90	130	ps
			$30mV_{P-P} \le V_{IN} \le 1200mV_{P-P}$		90	115	
Differential Input Resistance	R_{IN}	IN+ to IN-		95	100	105	Ω
Input-Referred Noise					220		μV_{RMS}
CML Output Voltage	V_{OUT}	LEVEL open, R_{LOAD} = 50Ω		550	750	1200	mV_{P-P}
Output Signal when Squelched		Outputs AC-coupled			2.2		mV_{P-P}
Power-Supply Noise Rejection	PSNR	f ≤ 2MHz (Note 7)			30		dB
Low Frequency Cutoff	f_{OC}	C_{AZ} = open			0.9		MHz
		C_{AZ} = 0.1µF			1.5		kHz
Output Resistance	R_{OUT}	Single ended to V_{CC}		42.5	50	57.5	Ω
Single-Ended Output Return Loss		≤ 2.5GHz			10		dB
		2.5GHz to 4.0GHz			9		
Differential Input Return Loss		4.0GHz			10		dB
OUTPOL Input Limits	V_{IL}					0.8	V
	V_{IH}			2.4			
LOS Hysteresis		(Notes 3, 4, 8)		2	3.3		dB
LOS Assert/Deassert Time		C_{CLOS} = open (Notes 3, 9, 10)			1		µs
		C_{CLOS} = 0.01µF (Notes 3, 9, 10)		2.3	50	100	
Low LOS Assert Level		R_{TH} = 20kΩ (Notes 3, 10)		4.5	6.5		mV_{P-P}
Low LOS Deassert Level		R_{TH} = 20kΩ (Notes 3, 10)			9.5	12.7	mV_{P-P}
Medium LOS Assert Level		R_{TH} = 1kΩ (Notes 3, 10)		7.8	12.9		mV_{P-P}
Medium LOS Deassert Level		R_{TH} = 1kΩ (Notes 3, 10)			17.4	22.4	mV_{P-P}
High LOS Assert Level		R_{TH} = 80Ω (Notes 3, 10)		24.3	48		mV_{P-P}

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High LOS Deassert Level		R_{TH} = 80Ω (Notes 3, 10)		73	124.7	mV_{P-P}
LOS Output High Voltage		Sinking 30µA	2.4			V
LOS Output Low Voltage		Sourcing 1.2mA			0.4	V
Squelch Input Current					400	µA

Note 1: Dice are designed and guaranteed from -40°C to +85°C but are tested only at T_A = +25°C.

Note 2: Supply current measurement excludes the current of the CML output stage (16mA typical). See Figure 1, *Power-Supply Current Measurement*.

Note 3: Guaranteed by design and characterization.

Note 4: Input edge speed is controlled using 4-pole, lowpass Bessel filters with bandwidth approximately 75% of the maximum data rate.

Note 5: Deterministic jitter is measured with a K28.5 pattern (0011 1110 1011 0000 0101). Deterministic jitter is the peak-to-peak deviation from ideal time crossings, measured at the zero-level crossings of the differential output per ANSI X3.230, Annex A.

Note 6: Random jitter is measured with the minimum input signal. For Fibre Channel and Gigabit Ethernet applications, the peak-to-peak random jitter is 14.1 times the RMS random jitter.

Note 7: Power-supply noise rejection (PSNR) is calculated by the equation PSNR = 20log ($\Delta V_{CC}/(\Delta V_{OUT})$), where ΔV_{OUT} is the change in differential output voltage due to the power-supply noise, ΔV_{CC}. See Power-Supply Noise Rejection vs. Frequency in the *Typical Operating Characteristics*.

Note 8: Hysteresis is defined as: $20 \times \log(V_{LOS\text{-}DEASSERT}/V_{LOS\text{-}ASSERT})$.

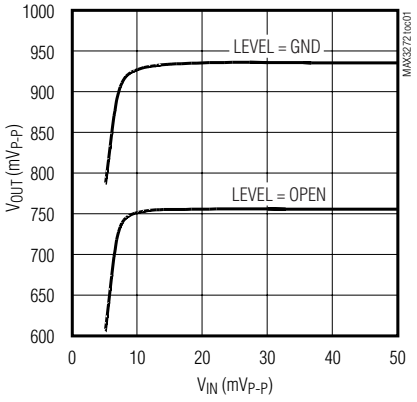
Note 9: Response time to a 10dB change in input power. For the specification guaranteed, the power is assumed to switch back and forth between two levels (separated by 10dB and equidistant from assert and deassert levels) outside of the two hysteresis thresholds.

Note 10: All power-detect AC parameters are guaranteed with a 2^{23} - 1 PRBS, 2.5Gbps input, with the longest possible run of 80CID.

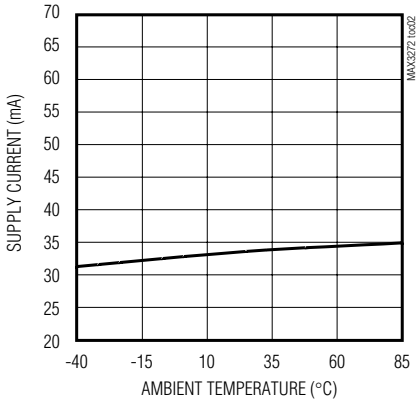
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

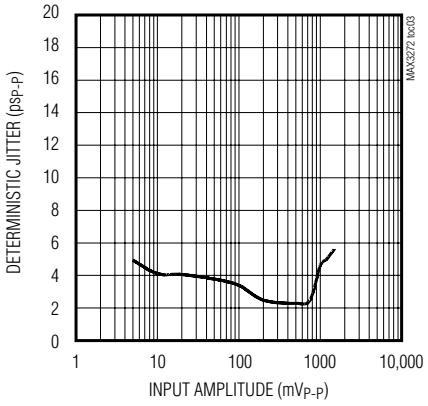
OUTPUT AMPLITUDE vs. INPUT AMPLITUDE



SUPPLY CURRENT vs. AMBIENT TEMPERATURE



DETERMINISTIC JITTER vs. INPUT AMPLITUDE

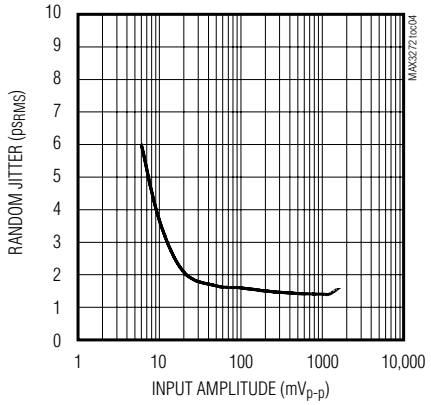


+3.3V, 2.5Gbps Low-Power Limiting Amplifiers

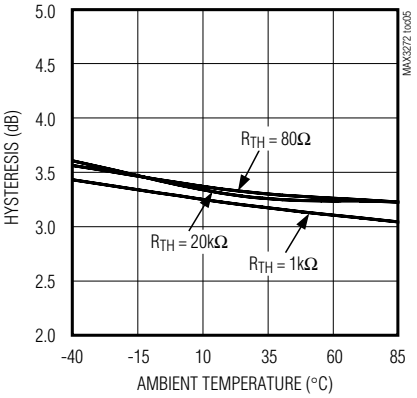
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

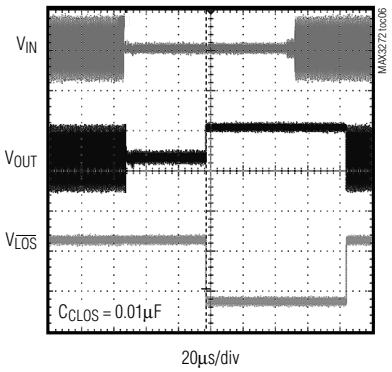
RANDOM JITTER vs. INPUT AMPLITUDE



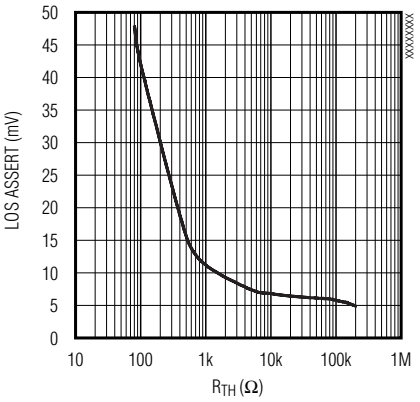
LOS HYSTERESIS vs. AMBIENT TEMPERATURE



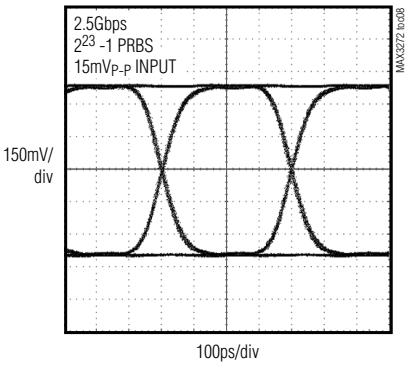
LOSS-OF-SIGNAL WITH SQUELCH



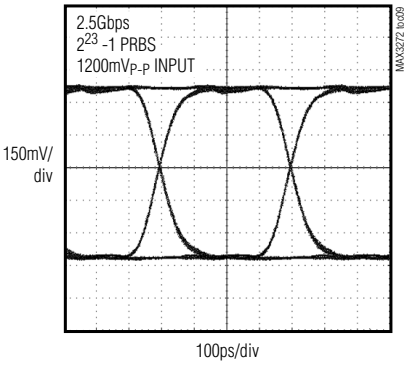
LOSS OF SIGNAL TRESHOLD vs. R_{TH}



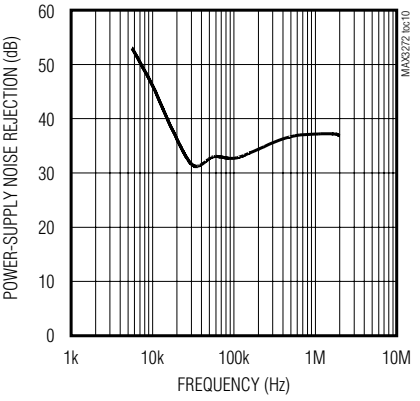
DATA OUTPUT EYE DIAGRAM (MINIMUM INPUT)



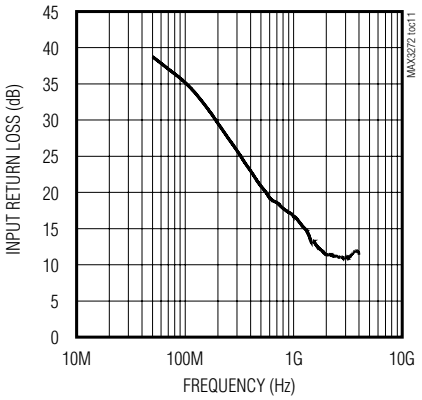
DATA OUTPUT EYE DIAGRAM (MAXIMUM INPUT)



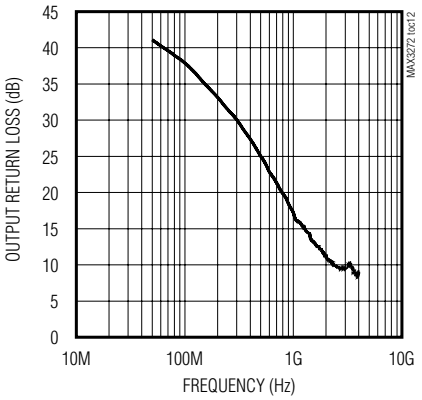
POWER-SUPPLY NOISE REJECTION vs. FREQUENCY



INPUT RETURN LOSS vs. FREQUENCY



OUTPUT RETURN LOSS vs. FREQUENCY

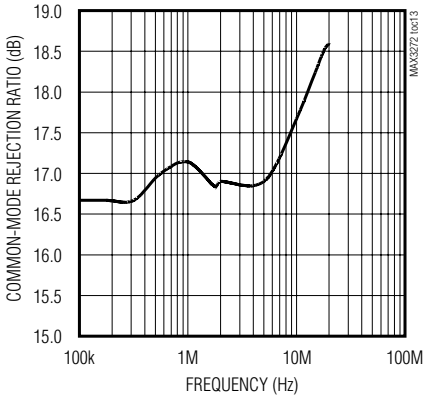


+3.3V, 2.5Gbps Low-Power Limiting Amplifiers

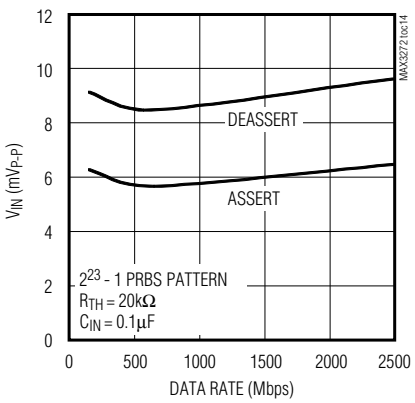
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

COMMON-MODE REJECTION RATIO vs. FREQUENCY



LOS ASSERT AND DEASSERT LEVELS vs. DATA RATE



Pin Description

PIN	NAME	FUNCTION
1, 4, 17	GND	Supply Ground
2	IN+	Noninverted Input Signal
3	IN-	Inverted Input Signal
5	TH	Loss-of-Signal Threshold Pin. Resistor to ground sets the LOS threshold.
6, 12, 15, 20	V_{CC}	Power Supply
7	CLOS	LOS Time-Constant Capacitor Connection. For SONET applications, C_{CLOS} = 0.01µF is recommended.
8	SQUELCH	Squelch Input. The squelch function is disabled when SQUELCH is not connected or set to TTL low level. When SQUELCH is set to TTL high level and LOS is asserted, the data outputs (OUT+, OUT-) are forced to static levels.
9	LOS	Noninverted Loss-of-Signal Output. LOS is asserted TTL high when the signal drops below the assert threshold set by the TH input. The MAX3272 does not have ESD protection on this pin. The MAX3272A has ESD protection on this pin.
10	$\overline{LOS}$	Inverted Loss-of-Signal Output. LOS is asserted TTL low when the signal drops below the assert threshold set by the TH input. The MAX3272 does not have ESD protection on this pin. The MAX3272A has ESD protection on this pin.
11	LEVEL	Output Current Level. When this pin is not connected, the CML output current is approximately 16mA. When this pin is connected to ground, the output current increases to about 20mA.
13	OUT-	Inverted Data Output
14	OUT+	Noninverted Data Output
16	OUTPOL	Output Polarity Control Input. Connect to GND for an inversion of polarity through the limiting amplifier and connect to V_{CC} for normal operation.
18	CAZ2	Offset-Correction-Loop Capacitor Connection. A capacitor connected between this pin and CAZ1 extends the time constant of the offset correction loop. Typical value of C_{AZ} is 0.1µF.
19	CAZ1	Offset-Correction-Loop Capacitor Connection. A capacitor connected between this pin and CAZ2 extends the time constant of the offset correction loop. Typical value of C_{AZ} is 0.1µF.
EP	EXPOSED PAD	Connect the exposed paddle to board ground for optimal electrical and thermal performance.

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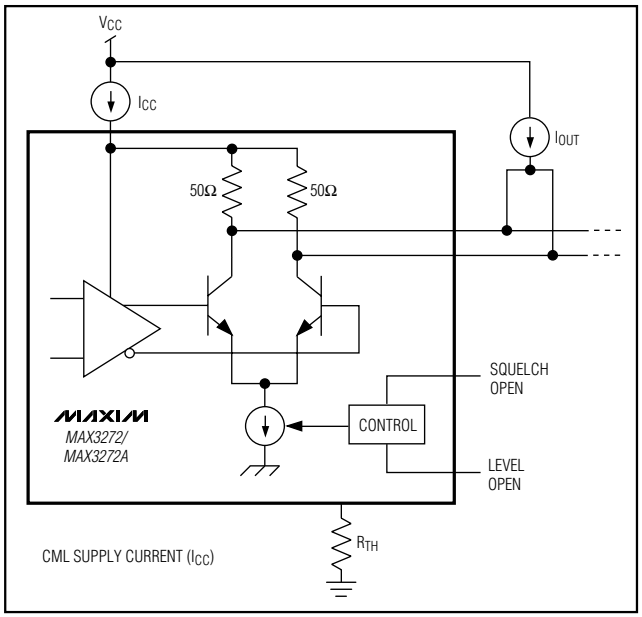


Figure 1. Power-Supply Current Measurement

Detailed Description

Figure 2 is a functional diagram of the MAX3272/MAX3272A, comprising a CML input buffer, power detector and loss-of- signal indicators, gain stage, offset-correction loop, and CML output buffer.

CML Input Buffer

The input buffer (Figure 3) provides 100Ω input impedance between IN+ and IN-. DC-coupling the inputs is not recommended; this prevents the DC offset-correction circuitry from functioning properly.

Power Detect and Loss-of-Signal Indicator

The MAX3272/MAX3272A are equipped with loss-of-signal (LOS) circuitry that indicates when the input signal is below a programmable threshold, set by resistor R_{TH} at the TH pin (see the *Typical Operating Characteristics* for appropriate resistor selection). An averaging peak-power detector compares the input signal amplitude with this threshold and feeds the signal-detect information to the LOS outputs, which are internally terminated to 8kΩ (Figure 4).

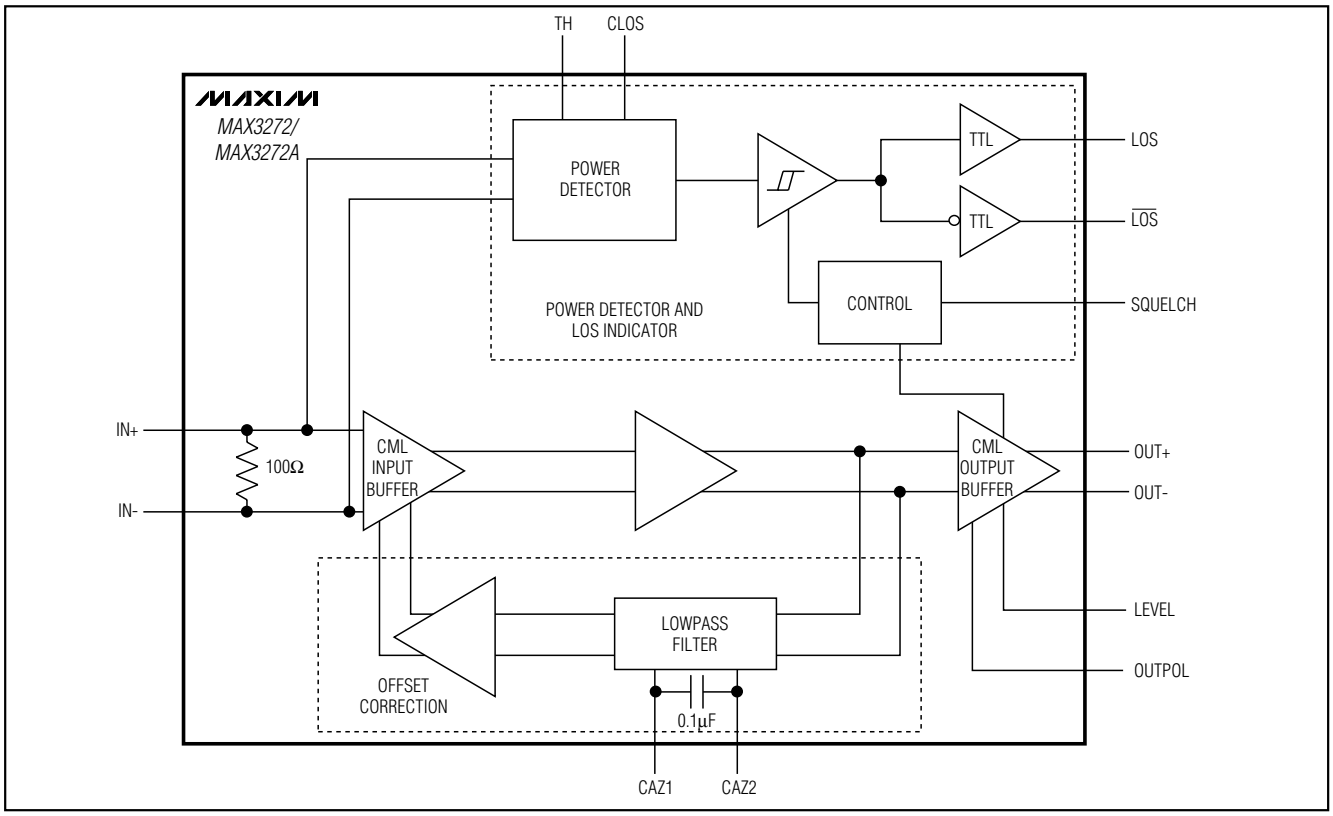


Figure 2. Functional Diagram

Interface Schematics

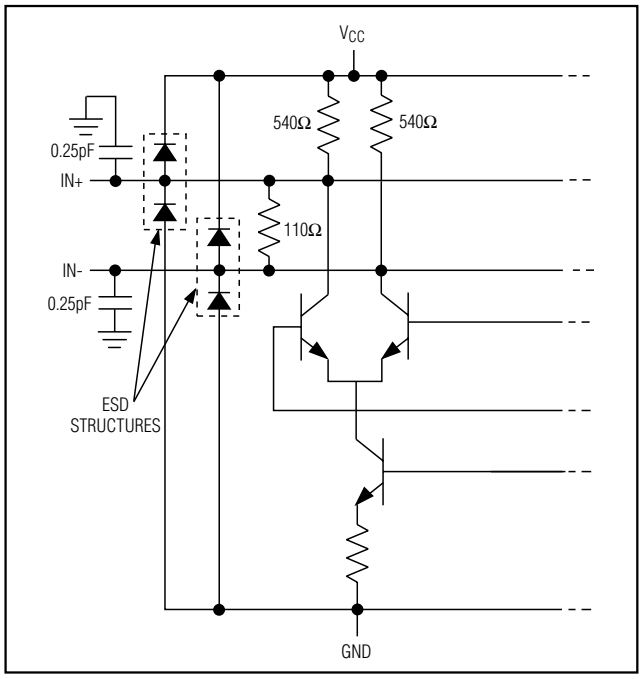


Figure 3. Input Circuit

Two control voltages V_{ASSERT}, and $V_{DEASSERT}$, define the LOS assert and deassert levels. To prevent LOS chatter in the region of the programmed threshold, approximately 3.3dB of hysteresis is built into the LOS assert/deassert function. Once asserted, LOS is not deasserted until the input amplitude rises to the required level ($V_{DEASSERT}$).

To facilitate interfacing with +5V modules, the LOS and $\overline{LOS}$ pins on the MAX3272 do not have internal ESD protection. If ESD protection is desired, a low-capacitance Schottky diode or diode array structure, such as the MAX3202E, is recommended (see the *Typical Operating Circuits*).

The LOS and $\overline{LOS}$ pins on the MAX3272A include ESD protection and, as a result, cannot be interfaced with +5V modules.

Gain Stage

The high-bandwidth gain stage provides approximately 42dB of gain.

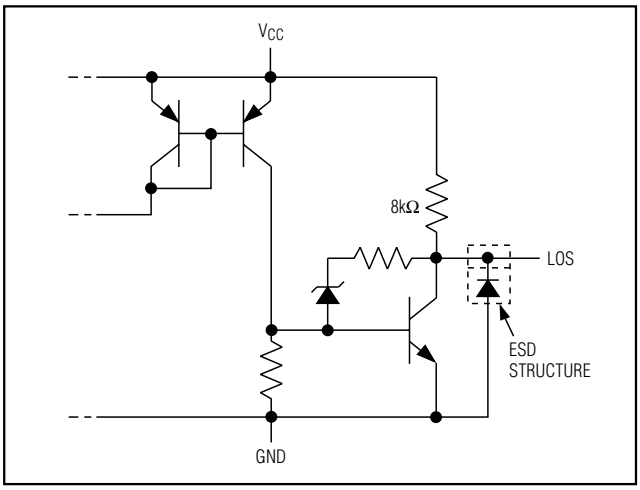


Figure 4a. LOS Output Circuit for MAX3272

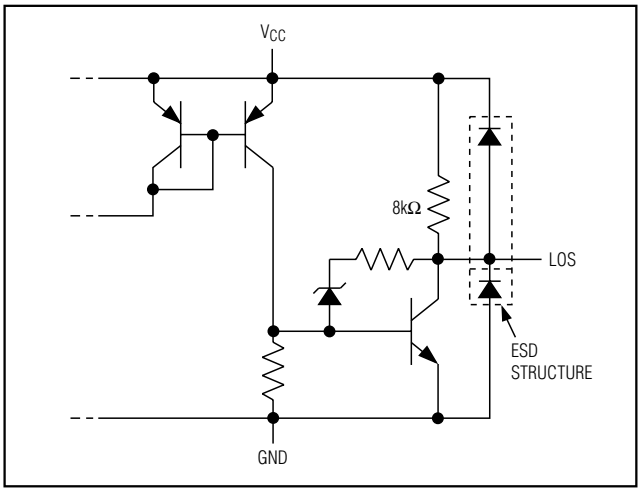


Figure 4b. LOS Output Circuit for MAX3272A

Offset-Correction Loop

Due to the high gain of the amplifier, the MAX3272/MAX3272A are susceptible to DC offsets in the signal path. In communications systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal or generated by the transimpedance amplifier appears as input offset and is removed by the offset-cancellation loop. An external capacitor is required between CAZ1 and CAZ2 to decouple the offset-cancellation loop and determine the lower 3dB frequency of the signal path.

+3.3V, 2.5Gbps Low-Power Limiting Amplifiers

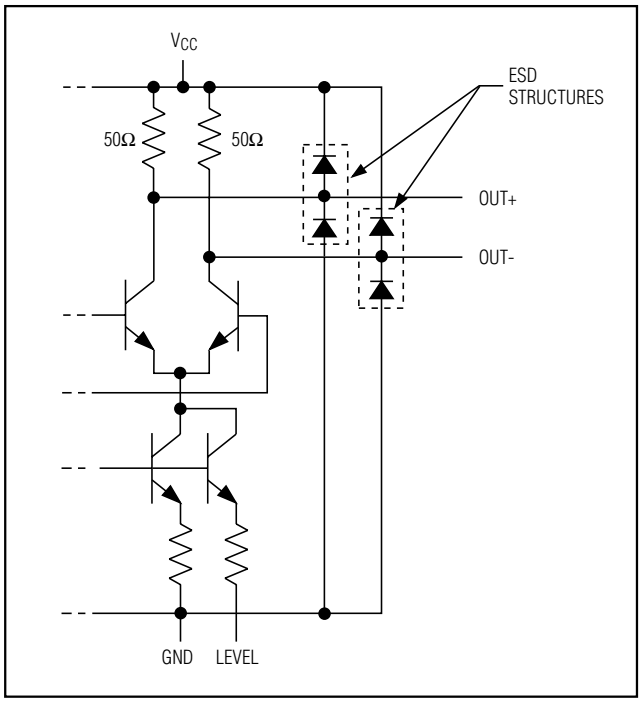


Figure 5. CML Output Circuit

CML Output Buffer

The MAX3272/MAX3272A CML output circuit (Figure 5) provides high tolerance to impedance mismatches and inductive connectors. The output current can be set to two levels using the LEVEL pin. When LEVEL is unconnected, the output current is approximately 16mA. Connecting LEVEL to ground sets the output current to approximately 20mA. The squelch function is enabled when the SQUELCH pin is set to a TTL high. This function holds OUT+ and OUT- to a static level whenever the input signal amplitude drops below the loss-of-signal threshold. This circuit is also equipped with a polarity selector, programmed by the OUTPOL pin. When this pin is connected to V_{CC}, no inversion will occur. When connected to ground, the output signal will be inverted.

Design Procedure

Program the LOS Assert Threshold

External resistor R_{TH} programs the loss-of-signal threshold. See the LOS Threshold vs. R_{TH} graph in the the *Typical Operating Characteristics* section to select the appropriate resistor.

Select the Coupling Capacitors

When AC-coupling, input and output coupling capacitors (C_{IN} and C_{OUT}) should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (f_{IN}) is decreased:

$$f_{IN} = 1 / [2\pi(50)(C_{IN})]$$

For ATM/SONET or other applications using scrambled NRZ data, select (C_{IN}, C_{OUT}) ≥ 0.1µF, which provides f_{IN} < 32kHz. For Fibre Channel, Gigabit Ethernet, or other applications using 8B/10B data coding, select (C_{IN}, C_{OUT}) ≥ 0.01µF, which provides f_{IN} < 320kHz. Refer to application note HFAN-1.1: *Choosing AC-Coupling Capacitors*.

Select the Offset-Correction Capacitor

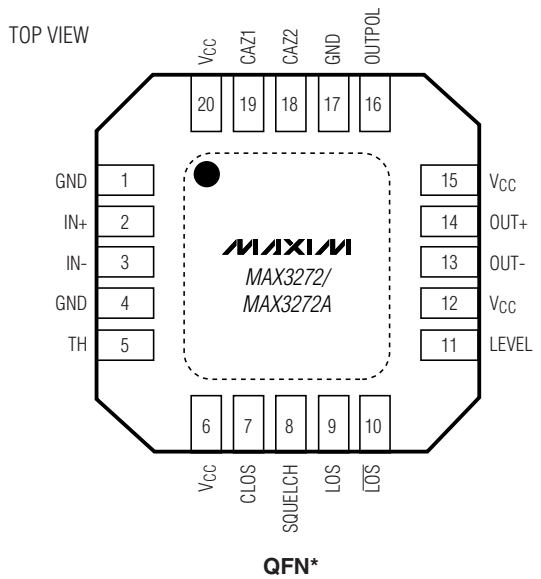
The capacitor between CAZ1 and CAZ2 determines the time constant of the signal path DC offset-cancellation loop. To maintain stability, it is important to keep a one-decade separation between f_{IN} and the low-frequency cutoff (f_{OC}) associated with the DC offset-cancellation circuit. For ATM/SONET or other applications using scrambled NRZ data, f_{IN} < 32kHz, so f_{OCMAX} < 3.2kHz. Therefore, C_{AZ} = 0.1µF (f_{OC} = 2kHz). For Fibre Channel or Gigabit Ethernet applications, leave pins CAZ1 and CAZ2 open.

Program the LOS Time Constant

External capacitor C_{CLOS} programs the LOS assert and deassert times. When inputting data with many consecutive identical digits (CIDs), a longer time constant may be advantageous, so LOS does not flag incorrectly. In this case, connect the CLOS pin to a 0.01µF capacitor to set the assert time in the range of 2µs to 100µs. For scrambled data where the mark density is kept at 50%, a shorter time constant may be desirable. Leave the CLOS pin open for a shorter time constant of about 1µs.

+3.3V, 2.5Gbps Low-Power Limiting Amplifiers

Pin Configuration



QFN*

NOTE: EXPOSED PAD MUST BE CONNECTED TO SUPPLY GROUND.

Pad Coordinates

PAD	NAME	COORDINATES (µm)
1	GND	47, 836
2	IN+	47, 603
3	IN-	47, 425
4	GND	47, 237
5	TH	47, 47
6	V_{CC}	255, -154
7	CLOS	436, -154
8	SQUELCH	645, -154
9	LOS	850, -154
10	$\overline{LOS}$	1063, -154
11	LEVEL	1331, 37
12	V_{CC}	1331, 212
13	OUT-	1331, 421
14	OUT+	1331, 573
15	V_{CC}	1331, 780
16	OUTPOL	1119, 1042
17	GND	957, 1042
18	CAZ2	773, 1042
19	CAZ1	583, 1042
20	N.C.	422, 1042
21	V_{CC}	268, 1042

Coordinates are for the center of the pad.

Coordinate 0, 0 is the lower left corner of the passivation opening for pad 5.

Applications Information

Optical Hysteresis

In an optical receiver, the electrical power change at the limiting amplifier is 2 times the optical power change.

As an example, if a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage input to the limiting amplifier also increases by a factor of two.

The optical power change is 10log(2x/x) = 10log(2) = +3dB.

At the limiting amplifier, the electrical power change is:

$$10\log\frac{(2V_{IN})^2 / R_{IN}}{V_{IN}^2 / R_{IN}} = 10\log(2^2) = 20\log(2) = +6dB$$

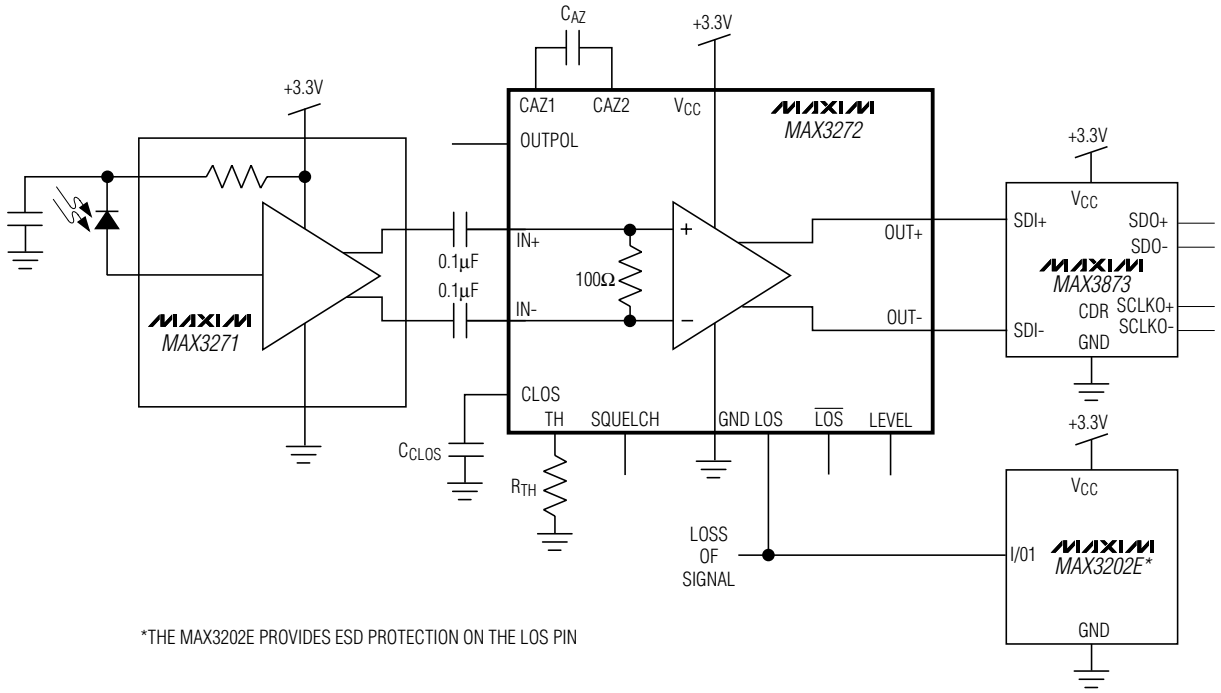
The MAX3272 typical voltage hysteresis is 3.3dB. This provides an optical hysteresis of 1.65dB.

Wire Bonding Die

For high-current density and reliable operation, the MAX3272 uses gold metallization. Make connections to the dice with gold wire only, and use ball-bonding techniques (wedge bonding is not recommended). Die pad dimensions are 94.4 microns by 94.4 microns. Die thickness is 15 mils (0.375mm).

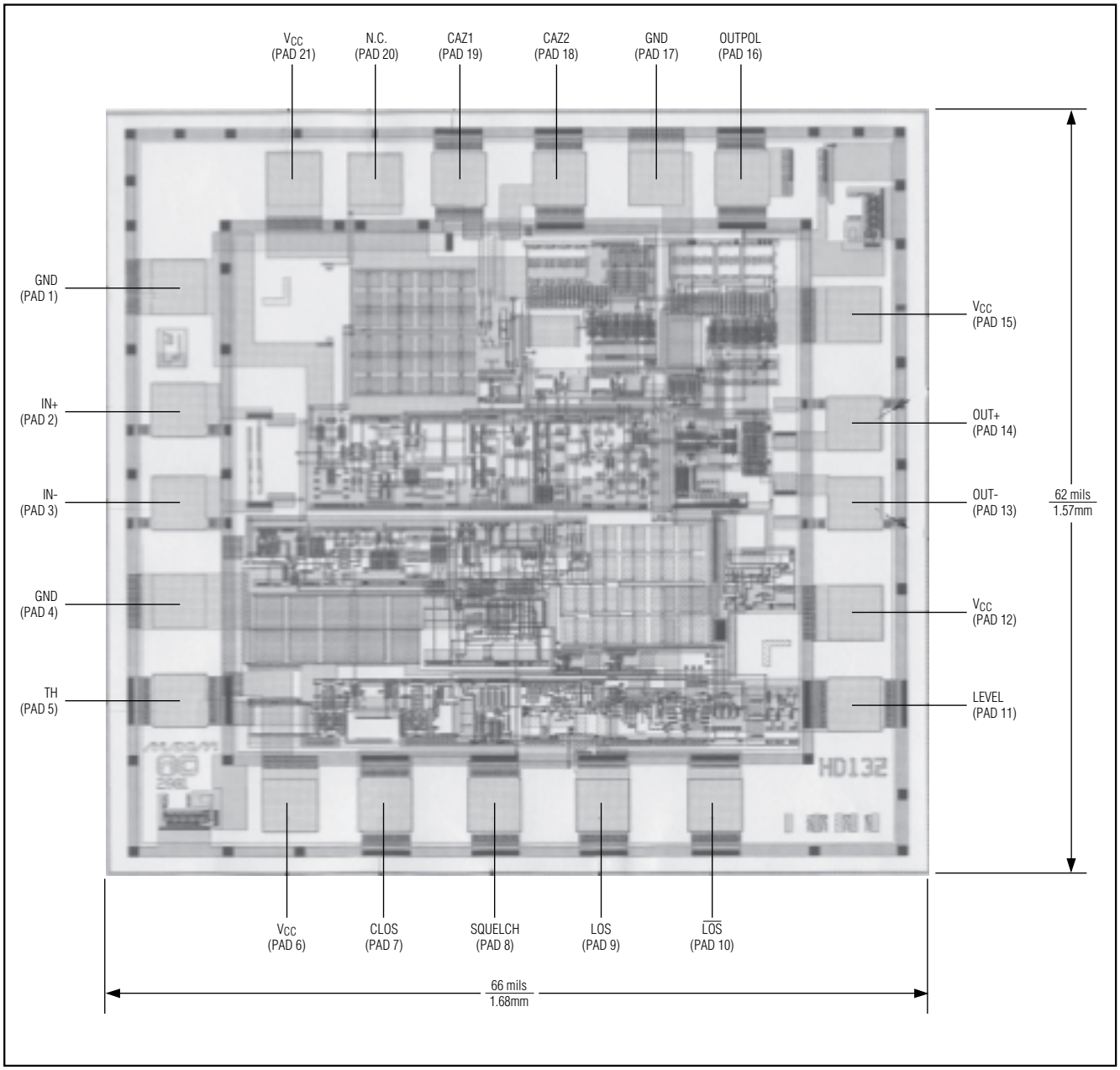
+3.3V, 2.5Gbps Low-Power Limiting Amplifiers

Typical Operating Circuit (continued)



*THE MAX3202E PROVIDES ESD PROTECTION ON THE LOS PIN

Chip Information



TRANSISTOR COUNT: 726

PROCESS: SiGe Bipolar

SUBSTRATE: Insulator, Connect to GND

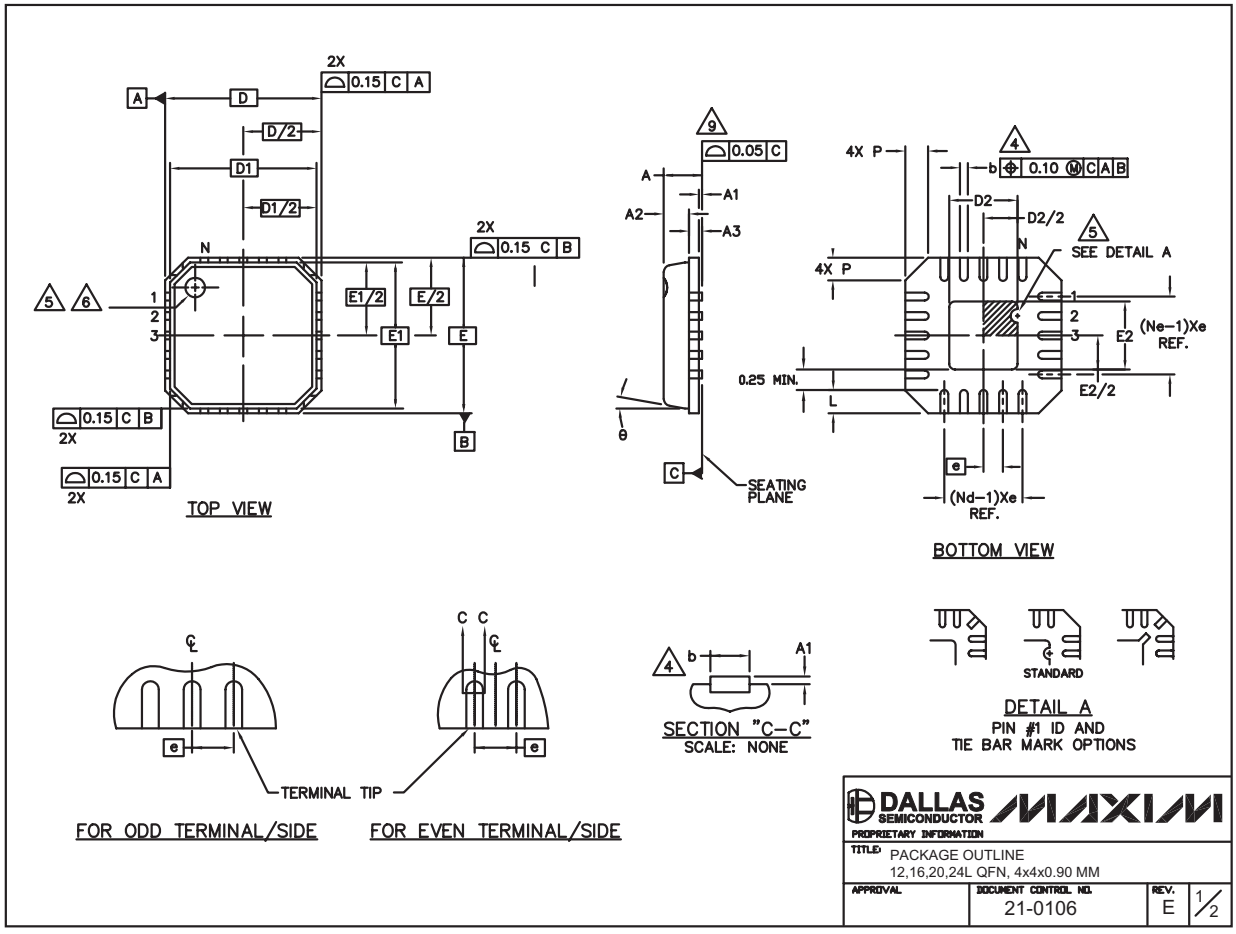
DIE SIZE: 1.68mm × 1.57mm

DIE THICKNESS: 15 mils

+3.3V, 2.5Gbps Low-Power Limiting Amplifiers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. THIS PACKAGE OUTLINE APPLIES TO PUNCHED QFN (STEPPED SIDES).

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ	0°	–	12°	
P	0.24	0.42	0.60	

SYMBOL	PITCH VARIATION A			NOTE	SYMBOL	PITCH VARIATION B			NOTE	SYMBOL	PITCH VARIATION C			NOTE	SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
e		0.80 BSC			e		0.65 BSC			e		0.50 BSC			e		0.50 BSC		
N		12		3	N		16		3	N		20		3	N		24		3
Nd		3		3	Nd		4		3	Nd		5		3	Nd		6		3
Ne		3		3	Ne		4		3	Ne		5		3	Ne		6		3
L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.30	0.40	0.50	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

PKG. CODE	EXPOSED PAD VARIATION					
	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
G1244–2	1.95	2.10	2.25	1.95	2.10	2.25
G1644–1	1.95	2.10	2.25	1.95	2.10	2.25
G2044–3	1.95	2.10	2.25	1.95	2.10	2.25
G2044–4	1.55	1.70	1.85	1.55	1.70	1.85
G2444–1	1.95	2.10	2.25	1.95	2.10	2.25

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 12,16,20,24L QFN, 4x4x0.90 MM			
APPROVAL	DOCUMENT CONTROL NO. 21-0106	REV. E	2/2