19-2215; Rev 0; 11/01

MAXIM

+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis

General Description

The MAX3892 serializer is ideal for converting 4-bit-wide, 622Mbps parallel data to 2.5Gbps serial data in DWDM and SONET/SDH applications. A 4 × 4-bit FIFO allows for any static delay between the parallel output clock and parallel input clock. Delay variation up to a unit interval (UI) is allowed after reset. A fully integrated phase-locked loop (PLL) synthesizes an internal 2.5GHz serial clock from a 622MHz, 155.5MHz, 77.8MHz, or 38.9MHz reference clock. A selectable dual VCO allows excellent jitter performance at both SONET and forward-error correction (FEC) data rates.

Operating from a single 3.3V supply, this device accepts low-voltage differential-signal (LVDS) clock and data inputs for interfacing with high-speed digital circuitry, and delivers current-mode logic (CML) serial data and clock outputs. A loopback data output is provided to facilitate system diagnostic testing. The MAX3892 is available in the extended temperature range (-40°C to +85°C) in a 44-pin QFN package.

Applications

SONET/SDH OC-48 Transmission Systems

WDM Transponders

Add/Drop Multiplexers

Dense Digital Cross-Connects

Backplane Interconnects

Features

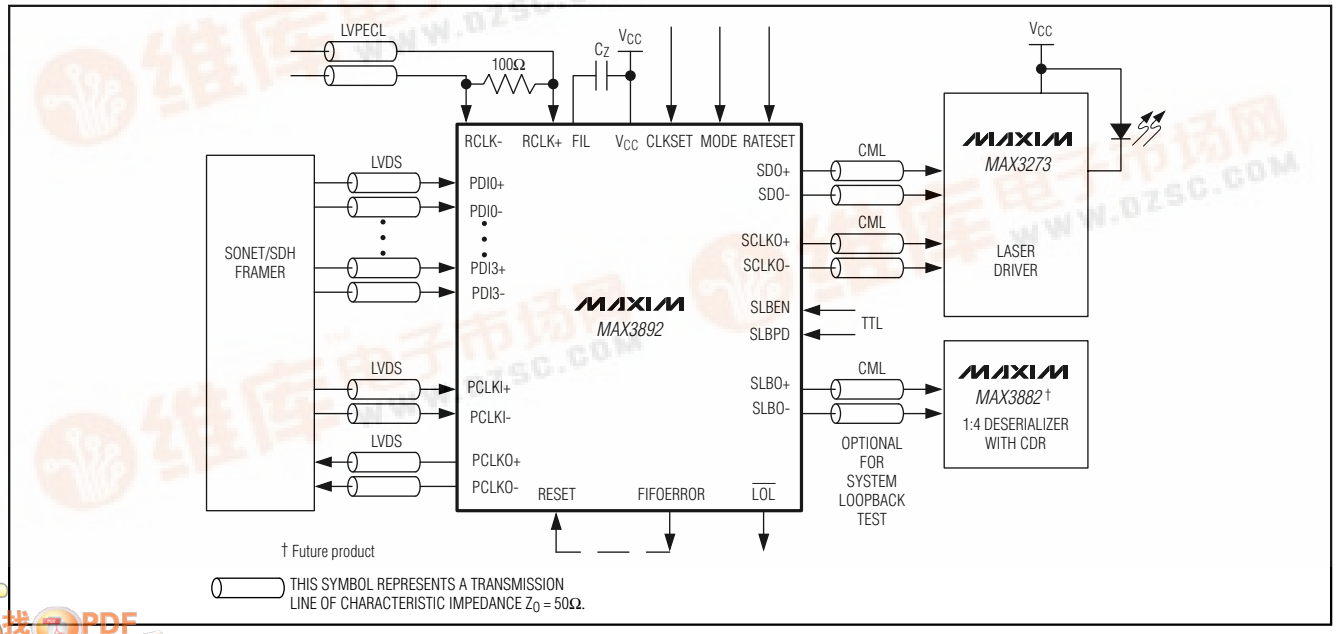
- ♦ **Single +3.3V Supply**
- ♦ **455mW Power Consumption**
- ♦ **1.4ps$_{RMS}$ Maximum Jitter Generation**
- ♦ **4 × 4-Bit FIFO Input Buffer**
- ♦ **622Mbps/666Mbps Parallel to 2.5Gbps/2.7Gbps Serial Conversion**
- ♦ **622MHz/667MHz or 311MHz/333MHz Clock Input**
- ♦ **On-Chip Clock Synthesizer**
- ♦ **Multiple Clock Reference Frequencies: (622.08MHz, 155.52MHz, 77.76MHz, 38.88MHz) or (666.51MHz, 166.63MHz, 83.31MHz, 41.66MHz)**
- ♦ **LVDS Parallel Clock and Data Inputs**
- ♦ **CML Serial Data and Clock Outputs**
- ♦ **Additional CML Output for System Loopback Testing**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3892EGH	-40°C to +85°C	44 QFN-EP*

*EP = exposed pad

Typical Application Circuit



+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}, VCCO, VCCVCO .....-0.5V to +5V
All Inputs and FIL .....-0.5V to (V_{CC} + 0.5V)
LVDS Output Voltage (PCLKO±).....-0.5V to (V_{CC} + 0.5V)
CML Output Current (SDO±, SCLKO±, SLBO±).....22mA
Continuous Power Dissipation (T_A = +85°C)
44-Pin QFN (derate 25mW/°C above +85°C) 1625mW

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, differential LVDS load = 100Ω ±1%, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Note 2)		138	190	mA
LVDS INPUT SPECIFICATIONS (PDI[3..0]±, PCLKI±)						
Input Voltage Range	V_I		0		2400	mV
Differential Input Voltage	$\|V_{ID}\|$		100			mV
Input Common-Mode Current		LVDS input V_{OS} = 1.2V		61		µA
Threshold Hysteresis				45		mV
Differential Input Resistance	R_{IN}		83	100	117	Ω
LVPECL INPUT SPECIFICATIONS (RCLK±)						
Input High Voltage	V_{IH}		V_{CC} - 1.16		V_{CC} - 0.88	V
Input Low Voltage	V_{IL}		V_{CC} - 1.81		V_{CC} - 1.48	V
Input Bias Voltage				V_{CC} - 1.3		V
Single-Ended Input Resistance				>1.0		kΩ
Differential Input Voltage Swing			300		1900	mVp-p
LVDS OUTPUT SPECIFICATIONS (PCLKO±)						
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\|V_{OD}\|$		250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	$\Delta\|V_{OD}\|$				25	mV
Offset Output Voltage			1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\|V_{OS}\|$				25	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, differential LVDS load = 100Ω ±1%, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Resistance			80		140	Ω
Output Current		Shorted together			12	mA
Output Current		Shorted to ground			40	mA
CML OUTPUT SPECIFICATIONS (SDO±, SCLKO±, SLBO±)						
Differential Output		R_L = 100Ω differential	640	800	1000	mVp-p
Differential Output Resistance			83	100	117	Ω
Output Common-Mode Voltage		R_L = 50Ω to V_{CC}		V_{CC} - 0.2		V
LVTTL SPECIFICATIONS (RESET, RATESET, SLBEN, SLBPD FIFOERROR, $\overline{LOL}$)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}		-30		+10	µA
Input Low Current	I_{IL}		-50		+10	µA
Output High Voltage	V_{OH}	I_{OH} = 20µA	2.4		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.4	V
PROGRAMMING INPUTS (CLKSET, MODE)						
Input Current		Input = 0 or V_{CC}	-500		+500	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, differential LVDS loads = 100Ω ±1%, CML loads = 50Ω ±1%, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL INPUT SPECIFICATIONS (PDI±, PCLKI±)						
Parallel Input Data Rate		RATESET = GND		622		Mbps
		RATESET = V_{CC}		666		
Parallel Input Clock Rate		MODE = OPEN or V_{CC}		622		MHz
		MODE = SHORT or 30kΩ to GND		311		
Parallel Input Setup Time	t_{SU}	(Note 4)	-94			ps
Parallel Input Hold Time	t_H	(Note 4)	300			ps
PARALLEL CLOCK OUTPUT SPECIFICATIONS (PCLKO±)						
Parallel Clock Output Rise/Fall Time	t_r, t_f	20% to 80%	100		200	ps
Parallel Clock Output Duty Cycle			46		54	%
SERIAL OUTPUT SPECIFICATIONS (SDO±, SCLKO±)						
Serial Output Data Rate		RATESET = GND		2.488		Gbps
		RATESET = V_{CC}		2.666		
Serial Data Output Rise/Fall Time	t_r, t_f	20% to 80%			80	ps
Serial Output Clock to Data Delay	t_{CLK-Q}	(Note 5)	-25		25	ps

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AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, differential LVDS loads = 100Ω ±1%, CML loads = 50Ω ±1%, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Output Jitter Generation	JG	(Note 6)		1.2	1.4	ps_{RMS}
Serial Data Output Random Jitter	RJ				1.4	ps_{RMS}
Serial Data Output Deterministic Jitter	DJ	(Note 7)			19	ps_{p-p}
REFERENCE CLOCK INPUT SPECIFICATIONS (RCLK)						
Reference Clock Frequency Tolerance			±100			ppm
Reference Clock Input Duty Cycle			30		70	%
RESET INPUTS (RESET)						
Minimum Pulse Width of FIFO Reset		UI is PCLKO period		4		UI
Tolerated Drift Between PCLKI and PCLKO After Reset		UI is PCLKO period		±1		UI

Note 1: Specifications at -40°C are guaranteed by design and characterization.

Note 2: Measured with SLBO/CLK622 and SCLK outputs disabled and CML outputs open.

Note 3: AC characteristics are guaranteed by design and characterization.

Note 4: In 622MHz clock mode, the parallel data is clocked in by the rising edge of the 622MHz/666MHz parallel clock input. In the 311MHz clock mode, the parallel data is clocked in on both the rising and falling edges of the clock. The parallel input setup and hold time increases by 60ps if the duty cycle is between 48% to 52% in 311MHz mode (Figure 1).

Note 5: Relative to the falling edge of the SCLKO.

Note 6: Measurement bandwidth is BW = 12kHz to 20MHz.

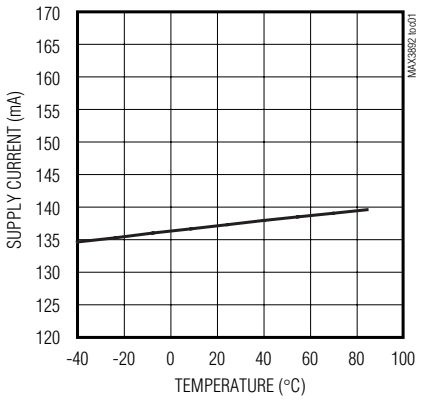
Note 7: Deterministic jitter includes pattern-dependent jitter and pulse-width distortion. Measured using a 2^7 - 1 PRBS pattern with 96 consecutive identical digits.

+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis

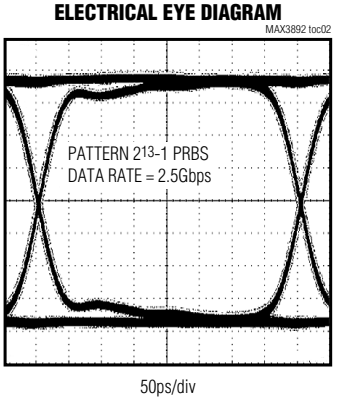
Typical Operating Characteristics

(V_{CC} = +3.3V, CML loads AC-coupled to 50Ω ±1%, T_A = +25°C, unless otherwise noted.)

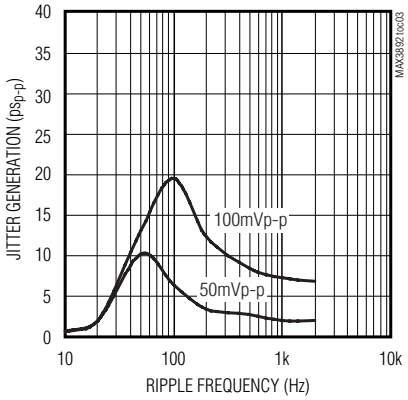
SUPPLY CURRENT vs. TEMPERATURE



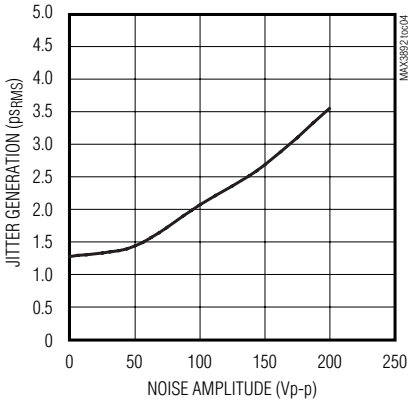
ELECTRICAL EYE DIAGRAM



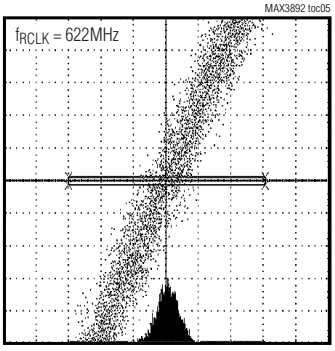
POWER-SUPPLY JITTER GENERATION vs. RIPPLE FREQUENCY



JITTER GENERATION vs. POWER SUPPLY NOISE AMPLITUDE (BW = 2MHz)



SERIAL-DATA OUTPUT JITTER



TOTAL WIDEBAND RMS JITTER = 1.3ps
PEAK-TO-PEAK JITTER = 15.8ps

Pin Description

PIN	NAME	FUNCTION
1, 16, 22, 27, 33, 44	GND	Supply Ground
2, 5, 8, 11	VCCO	Supply Voltage for Outputs +3.3V. Add bypass capacitors near these pins before connecting to the V_{CC} power plane.
3	SCLKO-	Negative Serial Clock Output, CML 2.488GHz or 2.666GHz
4	SCLKO+	Positive Serial Clock Output, CML 2.488GHz or 2.666GHz
6	SDO-	Negative Serial Data Output, CML 2.488Gbps or 2.666Gbps
7	SDO+	Positive Serial Data Output, CML 2.488Gbps or 2.666Gbps

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Pin Description (continued)

PIN	NAME	FUNCTION
9	SLBO-	Negative System Loop-Back Output or 622MHz/666MHz Clock Output. Select CML data or clock as shown in Table 1.
10	SLBO+	Positive System Loop-Back Output or 622MHz/666MHz Clock Output. Select CML data or clock as shown in Table 1.
12	SLBPD	System Loopback Power Down, TTL Input. SLPD = high activates the system loopback output driver; SLBPD = low powers down the loop-back output driver
13	SLBEN	System Loop-Back Enable Input, TTL Input. SLBEN = high activates the system loop-back output; SLBEN = low activates the 622MHz/666MHz reference clock output.
14	RESET	FIFO Reset, TTL Input. An active-high reset recenters the FIFO to tolerate maximum skew between PCLKI and PCLKO.
15	FIFOERROR	FIFO Error Indicator, TTL Output. Active high when the read/write clocks access the same FIFO address. This signal may be used to control RESET.
17, 28, 36, 41	V_{CC}	Supply Voltage, +3.3V
18	$\overline{LOL}$	Loss of Lock, TTL Output. An active low indicates that the VCO and reference frequency differ by 500ppm.
19	MODE	Clock Control Input: MODE = GND; f_{PCLKI} = 311.04MHz/333MHz with SCLKO active MODE = 30kΩ to GND; f_{PCLKI} = 311.04MHz/333MHz with SCLKO off MODE = OPEN (float); f_{PCLKI} = 622.08MHz/666MHz with SCLKO off MODE = V_{CC}; f_{PCLKI} = 622.08MHz/666MHz with SCLKO active
20	PCLKI+	Positive Parallel Clock, LVDS Input. Data is written to the input register on the clock rising edge in 622Mbps mode and on both rising and falling edges in 311Mbps mode (Figure 1).
21	PCLKI-	Negative Parallel Clock, LVDS Input (Figure 1).
23, 25, 29, 31	PDI3+ to PDI0+	Positive Data Inputs, LVDS (622Mbps or 666Mbps)
24, 26, 30, 32	PDI3- to PDI0-	Negative Data Inputs, LVDS (622Mbps or 666Mbps)
34	PCLKO+	Positive Parallel Clock Output, LVDS. This clock may be 622.08MHz or 666MHz.
35	PCLKO-	Negative Parallel Clock Output, LVDS. This clock may be 622.08MHz or 666MHz.
37	RCLK+	Positive Reference Clock Input, LVPECL
38	RCLK-	Negative Reference Clock Input, LVPECL
39	CLKSET	Reference Clock Rate Programming Pin: CLKSET = V_{CC}; RCLK = 622.08MHz/666MHz CLKSET = OPEN (float); RCLK = 155.52MHz/167MHz CLKSET = 30kΩ to GND; RCLK = 77.76MHz/83.3MHz CLKSET = GND; RCLK = 38.88MHz/41.6MHz
40	RATESET	Data Rate Select, TTL Input. RATESET = high for 2.666Gbps, RATESET = low for 2.488Gbps.
42	FIL	PLL Capacitor Pin. Connect a 0.1µF capacitor from this pin to VCCVCO.
43	VCCVCO	Supply Voltage for VCO +3.3V. Add bypass capacitors near this pin before connecting to the V_{CC} power plane.
EP	Exposed Paddle	The exposed paddle must be soldered to ground for proper thermal and electrical operation.

+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis

Detailed Description

The MAX3892 converts 4-bit-wide, 622Mbps/667Mbps data to 2.5Gbps/2.7Gbps serial data (Figure 2). Data is loaded into the 4:1 MUX through a 4 × 4-bit FIFO buffer for wide tolerance to clock skew. Clock and data inputs are LVDS levels while high-speed serial outputs are CML. An internal PLL frequency synthesizer generates a serial clock from a low-speed reference clock.

Low-Voltage Differential-Signal Inputs and Outputs

The MAX3892 has LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses differential low-voltage swings to achieve fast transition times, minimized power dissipation, and noise immunity. For proper operation, the parallel clock LVDS outputs (PCLKO+, PCLKO-) require 100Ω differential DC termination between the positive and negative outputs. Do not terminate these outputs to ground. The parallel data and parallel clock LVDS inputs (PDI+, PDI-, PCLKI+, PCLKI-) are internally terminated with 100Ω differential input resistance, and therefore do not require external termination.

PECL Inputs

The reference clock (RCLK+, RCLK-) has PECL inputs for interfacing to a crystal oscillator with AC or DC connections. The RCLK inputs are self-biasing to V_{CC} - 1.3V for AC-coupled inputs. Only a 100Ω differential termination resistance must be added when inputs are AC-coupled.

Current-Mode Logic Outputs

The 2.5Gbps/2.7Gbps data, clock, and system loopback outputs (SDO+, SDO-, SCLKO+, SCLKO-, SLBO+, SLBO-) of the MAX3892 are designed using current-mode logic (CML). The configuration of the MAX3892 CML output circuit includes internal 50Ω back termination to V_{CC} (Figure 3). These outputs are intended to drive a 50Ω transmission line terminated with a matched load impedance.

FIFO Buffer

Data is latched into the MAX3892 by the parallel input clock PCLKI. The parallel input clock serves as the FIFO write clock. The parallel output clock PCLKO acts as the FIFO read clock that loads the 4:1 MUX. The FIFO allows the read and write clocks to vary by up to ±1UI. Conditions that result in the read and write clock accessing the same FIFO address are indicated by

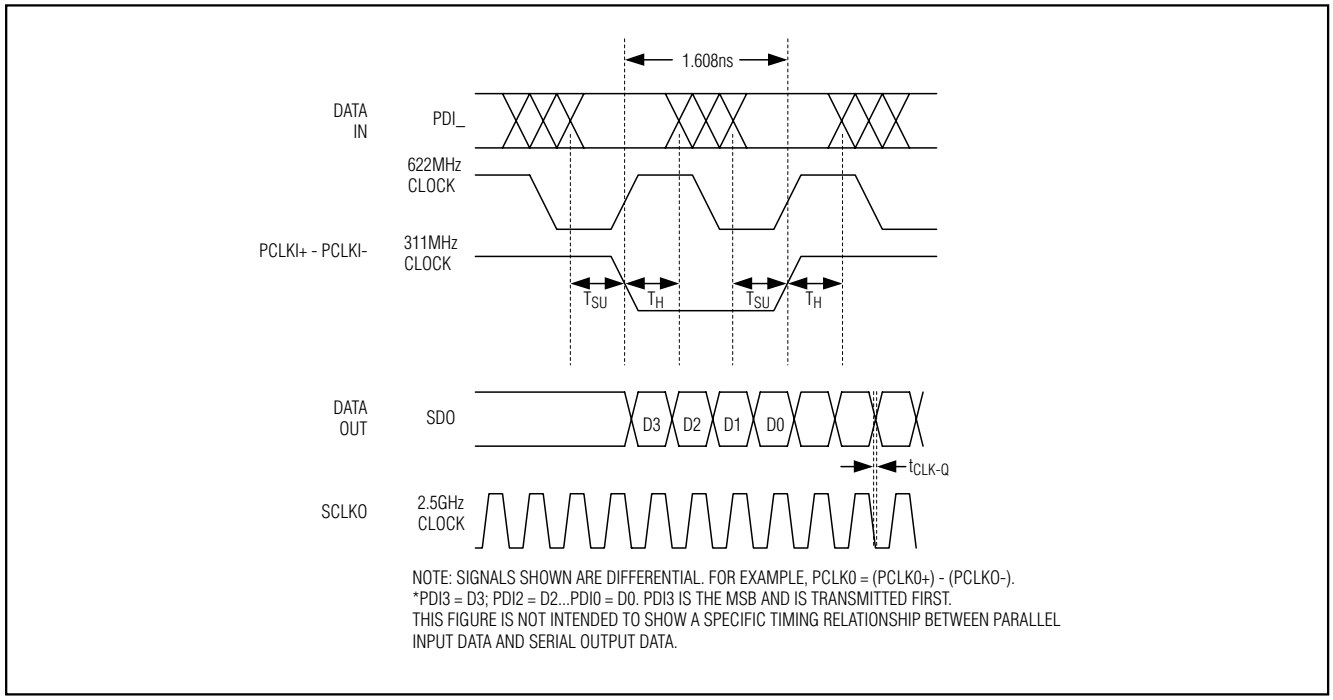

Figure 1. Timing Diagram

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Table 1. Loop-Back Operation Mode

SLBPD	SLBEN	SLBO± OUTPUT
V_{IL}	X	Power-Down SLBO Output
V_{IH}	V_{IL}	622MHz/667MHz Clock Output
V_{IH}	V_{IH}	2.5Gbps/2.7Gbps System Loop-Back Output

Table 2. Setting the Reference Clock Frequency

CLKSET	RATESET	RCLK± FREQUENCY (MHz)
V_{CC}	V_{CC}	666
	GND	622
OPEN	V_{CC}	166.5
	GND	155.52
30kΩ to GND	V_{CC}	83.25
	GND	77.76
GND	V_{CC}	41.63
	GND	38.88

latching high FIFOERROR. To clear this condition, RESET must be asserted high for at least 4UI. FIFOERROR may be tied directly to the RESET input to recenter the FIFO. After reset, the full elastic range of the FIFO is available again.

Frequency Synthesizer

The PLL synthesizes a 2.5Gbps/2.7Gbps clock (SCLKO) from an external reference clock. The PLL reference clock (RCLK) may be 622.08MHz/666.53MHz, 155.52MHz/166.6MHz, 77.76MHz/83.3MHz or 38.88MHz/41.65MHz as determined by CLKSET and RATESET. See Table 2 for the reference frequency selection. The parallel output clock PCLKO is also derived from the synthesizer to be SCLKO divided by 4. A TTL-compatible loss-of-lock indicator, $\overline{LOL}$, goes low when the VCO is unable to lock to the reference frequency. Frequency difference on RCLK with respect to the divided down SCLKO greater than 500ppm is indicated by a low state on $\overline{LOL}$. When the frequency difference between the clocks is less than 250ppm, $\overline{LOL}$ high indicates a lock condition.

System Loopback

The MAX3892 is designed to allow system loop-back testing. The loop-back outputs (SLBO+, SLBO-) of the MAX3892 may be directly connected to the loop-back inputs of a deserializer (such as the MAX3882) for system diagnostics. Alternatively, the SLBO pins can be programmed to provide a 622MHz reference clock.

Table 3. Setting the Clock Mode

MODE	RATESET	PCLKI± FREQUENCY (MHz)	SCLKO± FREQUENCY (GHz)
V_{CC}	V_{CC}	666Hz	2.666
	GND	622Hz	2.488
OPEN	V_{CC}	666Hz	Disabled
	GND	622Hz	Disabled
30kΩ to GND	V_{CC}	333Hz	Disabled
	GND	311Hz	Disabled
GND	V_{CC}	333Hz	2.666
	GND	311Hz	2.488

This reference clock can provide a clock hold-over signal to a clock and data recovery (CDR) circuit in the event of loss of signal (LOS).

Design Procedure

Clock Mode Selection

The frequencies of the MAX3892 can be set up using CLKSET, RATESET, and MODE as shown in Tables 2 and 3.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3892 clock and data inputs and outputs.

Exposed-Pad Package

The EP 44-pin QFN incorporates features that provide a very low thermal-resistance path for heat removal from the IC to a PC board. The MAX3892's EP must be soldered directly to a ground plane with good thermal conductance.

+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis

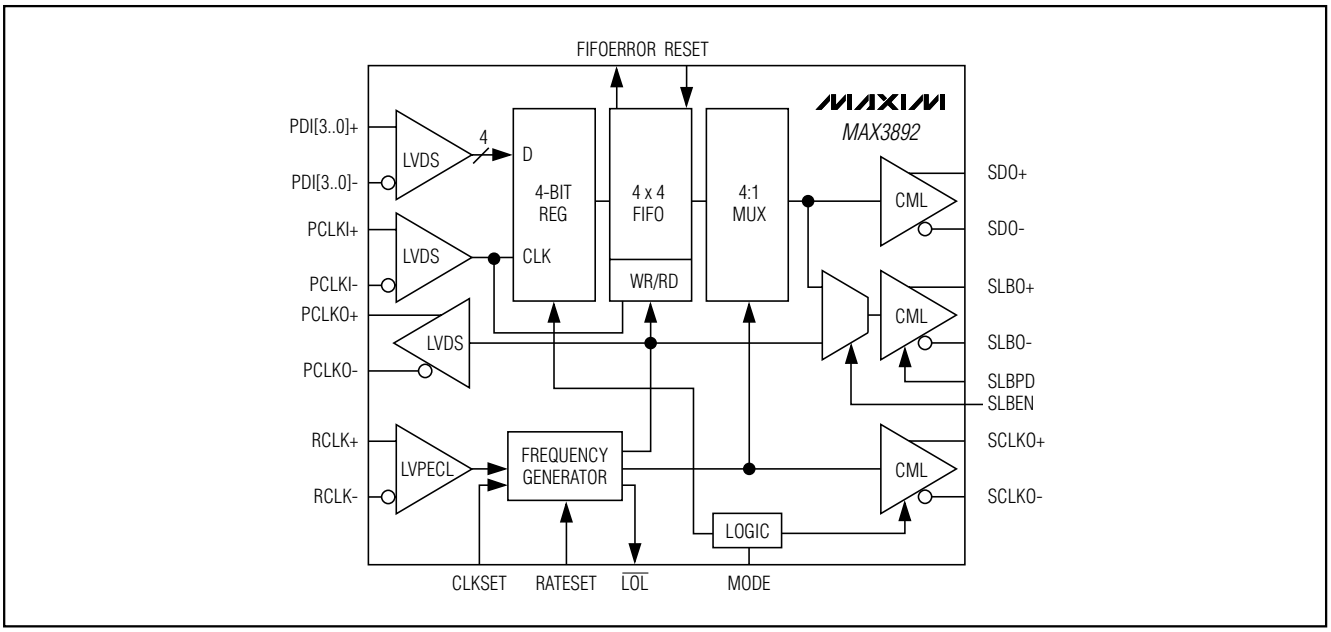


Figure 2. Functional Diagram

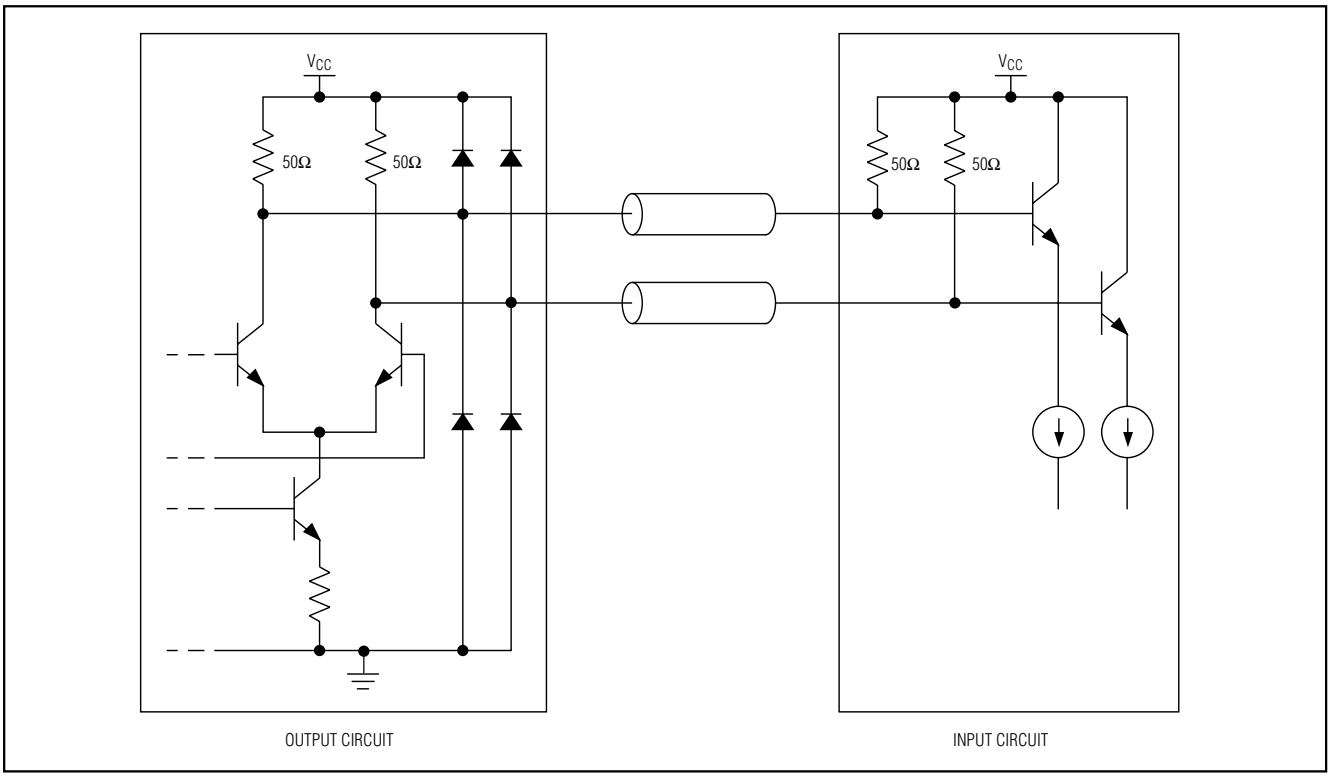


Figure 3. Current-Mode Logic

+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis

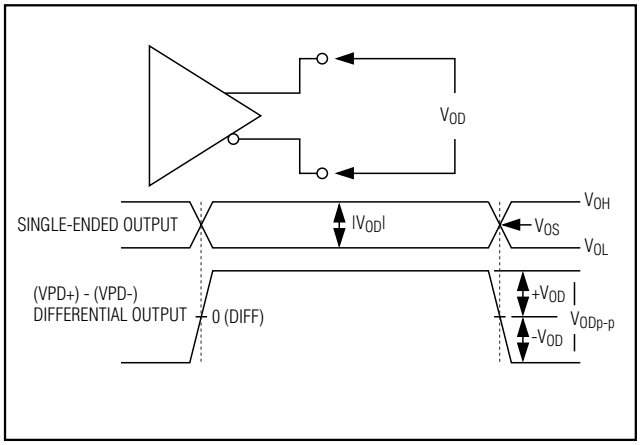
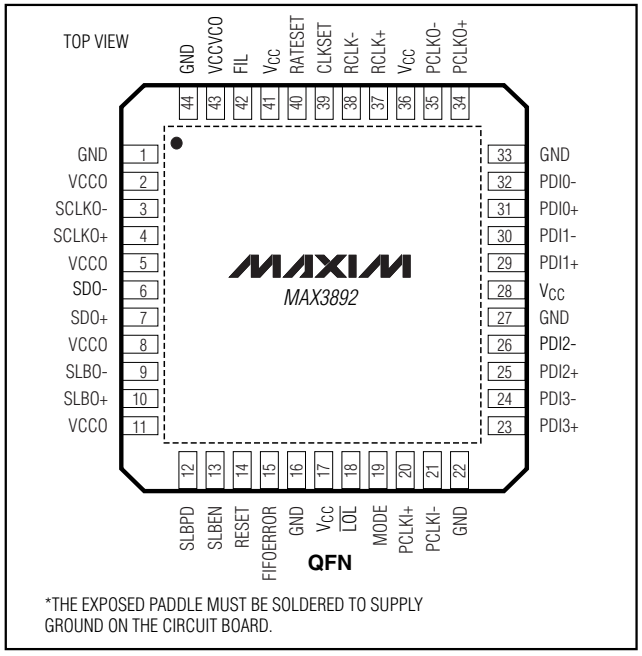


Figure 4. Differential Output Levels

Pin Configuration



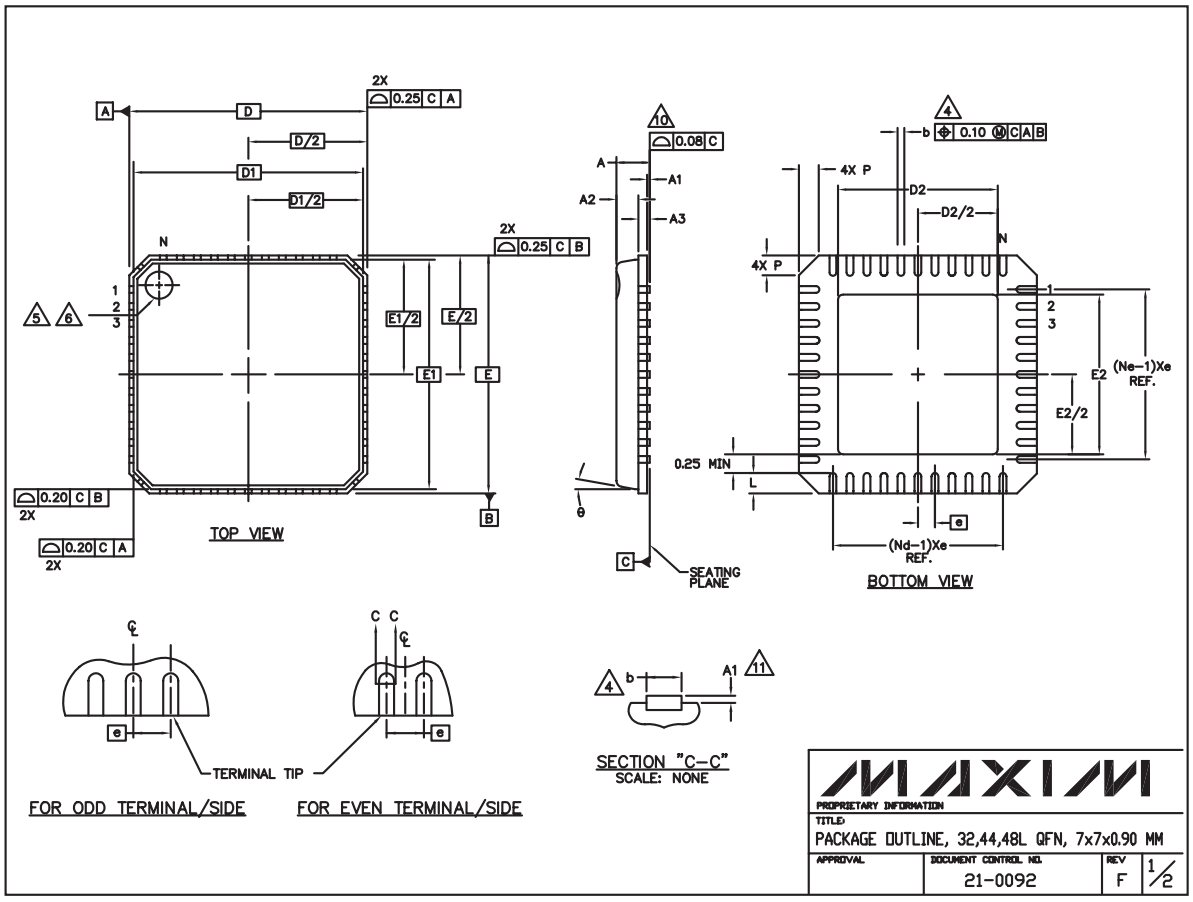
Chip Information

TRANSISTOR COUNT: 6210

+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis

Package Information

QFN 28, 32,44, 48L.EPS



+3.3V, 2.5Gbps/2.7Gbps, SDH/SONET 4:1 Serializer with Clock Synthesis

Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED. OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.08mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		7.00 BSC		
D1		6.75 BSC		
E		7.00 BSC		
E1		6.75 BSC		
θ	0°		12°	
P	0		0.60	
D2	2.25	–	5.25	
E2	2.25	–	5.25	

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		44		3
Nd		11		3
Ne		11		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		48		3
Nd		12		3
Ne		12		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32,44,48L QFN, 7x7x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0092	F	2/2