



+3.3V, 2.5Gbps Quad Limiting Amplifier

MAX3822

General Description

The MAX3822 quad limiting amplifier is ideal for multi-channel systems with data rates up to 2.5Gbps. The MAX3822 operates from a single +3.3V supply, over temperatures ranging from 0°C to +85°C. A channel-select (CS) pin is provided to program single-, dual-, or quad-channel operation. The disabled channels are shut down to reduce power consumption. The output interface for all four channels is CML.

The input can be driven from 20mVp-p to 1000mVp-p differentially. The threshold voltage control is common for all four channels and is programmable by an external resistor. Four separate power detectors are incorporated to monitor the received signal level for each channel. Individual TTL-compatible loss-of-power (LOP) indicators assert low if the channel signal input is below the programmed threshold. Typically 4dB LOP hysteresis (2dB optical) is provided to prevent chattering when the input signal level is close to the threshold. A general LOP indicator is also provided which asserts low if one or more of the four inputs is in the LOP condition.

Applications

- Optical System Interconnects
- Multichannel Receiver Modules
- Dense Digital Cross-Connects
- ATM Switch Networks
- High-Speed Parallel Links

Features

- ◆ Single +3.3V Supply
- ◆ Single-, Dual-, or Quad-Channel Operation at 2.5Gbps
- ◆ 700mW Total Power Dissipation (Quad-Channel Operation)
- ◆ 120ps Maximum Output Edge Speed
- ◆ Overall and Individual Channel Loss-of-Power (LOP) Indicator
- ◆ Differential CML Outputs with On-Chip Back Termination Resistors
- ◆ 30ps Maximum Deterministic Jitter
- ◆ 2ps Random Jitter
- ◆ Power-Down Feature Shuts Down Unused Channels
- ◆ Operating Temperature Range: 0°C to +85°C

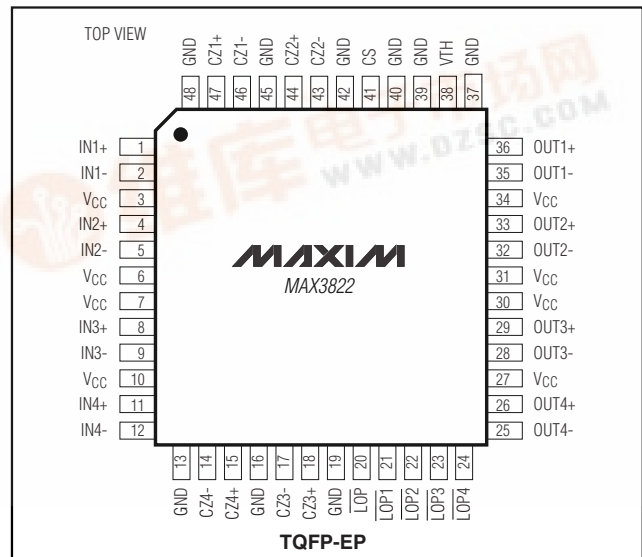
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3822UCM	0°C to +85°C	48 TQFP-EP*
MAX3822U/D	0°C to +85°C	Dice**

*Exposed pad

**Contact factory for availability. Dice are designed to operate from $T_A = 0^\circ\text{C}$ to $T_A = +85^\circ\text{C}$, but are tested and guaranteed only at $T_A = +25^\circ\text{C}$.

Pin Configuration



Typical Operating Circuit appears at end of data sheet.

+3.3V, 2.5Gbps Quad Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	-0.5V to +6.0V	Current into OUT1+, OUT1-, OUT2+, OUT2-, OUT3+, OUT3-, OUT4+, OUT4-,	$\pm 22\text{mA}$
Differential Input Voltage Swing (IN1+ - IN1-), (IN2+ - IN2-), (IN3+ - IN3-), (IN4+ - IN4-)	2Vp-p	Continuous Power Dissipation ($T_A = +85^\circ\text{C}$) 48-Pin TQFP-EP (derate 29.4mW/ $^\circ\text{C}$ above +85 $^\circ\text{C}$)	2.35W
Voltage at LOP1, LOP2, LOP3, LOP4, LOP, CS	-0.5V to ($V_{CC} + 0.5\text{V}$)	Operating Junction Temperature Range (die)	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Voltage at IN1+, IN1-, IN2+, IN2-, IN3+, IN3-, IN4+, IN4-	($V_{CC} - 1\text{V}$) to ($V_{CC} + 0.5\text{V}$)	Processing Temperature (die)	+400 $^\circ\text{C}$
Voltage at VTH	+0.5V to +2.3V	Storage Temperature Range	-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Voltage at CZ1+, CZ1-, CZ2+, CZ2-, CZ3+, CZ3-, CZ4+, CZ4-	-0.5V to ($V_{CC} + 0.5\text{V}$)	Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0\text{V}$ to +3.6V, $T_A = 0^\circ\text{C}$ to +85 $^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.3\text{V}$ and $T_A = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Current	I _{CC}	Single channel (Note 2)		60	72	mA
		Dual channel (Note 2)		110	137	
		Quad channel		210	265	
Single-Ended Data Input Voltage Range	V _{IS}		$V_{CC} - 0.5$		$V_{CC} + 0.25$	V
Single-Ended Data Input Resistance			40	50	60	Ω
Data Input Voltage for $\overline{\text{LOP}}$ Assert		$R_{TH} = 1\text{k}\Omega$		14		mVp-p
		$R_{TH} = 649\Omega$	11.5	18.5	32.5	
		$R_{TH} = 400\Omega$		34		
$\overline{\text{LOP}}$ Hysteresis		$R_{TH} = 1\text{k}\Omega$		4.5		dB
		$R_{TH} = 649\Omega$	3.0		6.0	
		$R_{TH} = 400\Omega$		3.4		
CML Differential Output	V _{OD}	$R_L = 50\Omega$ to V_{CC}	640	740	1000	mVp-p
Single-Ended Data Output Resistance			40	50	60	Ω
CML Output Common-Mode Voltage				$V_{CC} - 0.2$		V
TTL Output High	V _{OH}	Sourcing 200 μA	2.4		V_{CC}	V
TTL Output Low	V _{OL}	Sinking 2mA			0.4	V

+3.3V, 2.5Gbps Quad Limiting Amplifier

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0V$ to $+3.6V$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^{\circ}C$.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Voltage Range	V_{IN}		20		1000	mVp-p
Random Jitter		(Note 4)		2	9.5	psRMS
Deterministic Jitter		$V_{IN} = 20mVp-p$ (Notes 5, 6)		8		psp-p
		$V_{IN} = 1000mVp-p$ to $1000mVp-p$ (Notes 5, 6)		4	30	
Data Output Edge Speed		(20% to 80%)		90	120	ps
LOP Assert/Deassert Time			100			ns
Input-Referred Noise		(Note 7)		105	594	μV_{RMS}
Offset Correction Low-Frequency Cutoff		$CZ1 = CZ2 = CZ3 = CZ4 = 0.033\mu F$		150		kHz
Channel-to-Channel Skew		(Note 8)		20	70	ps

Note 1: Characteristics at $0^{\circ}C$ are guaranteed by design and characterization. Dice are tested at $T_A = +25^{\circ}C$.

Note 2: When power is first applied, all four channels are briefly active.

Note 3: AC characteristics are guaranteed by design and characterization.

Note 4: Input data edge speed of 150ps (20% to 80%).

Note 5: Data rate = 2.5Gbps. Measured with $2^{13} - 1$ PRBS plus 100 consecutive identical digits.

Note 6: Deterministic jitter (p-p) equals total jitter (p-p) minus random jitter (p-p).

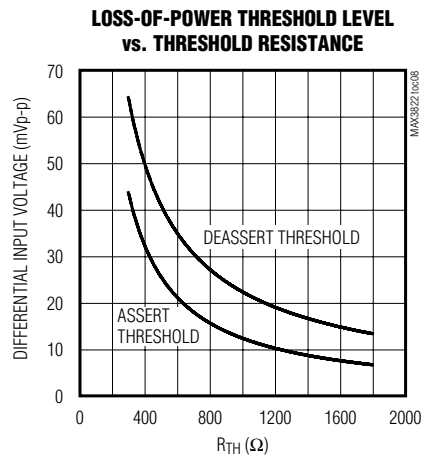
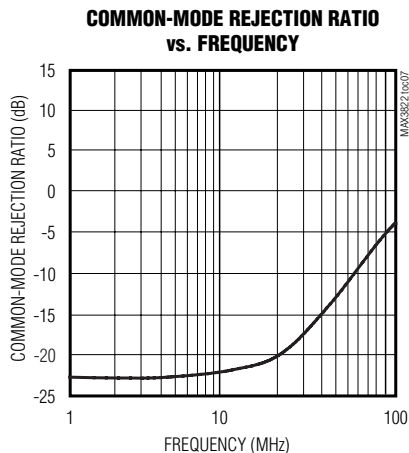
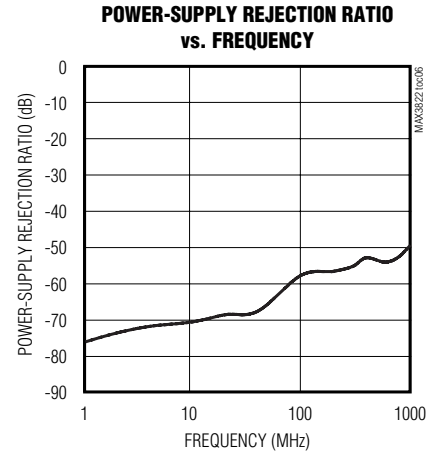
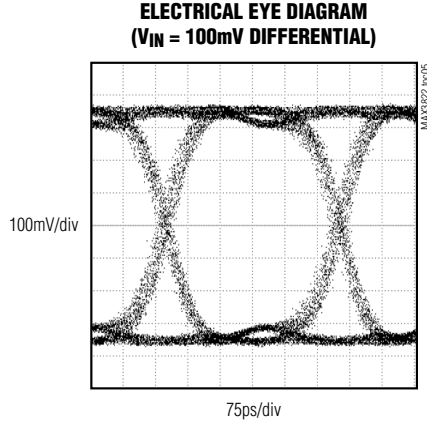
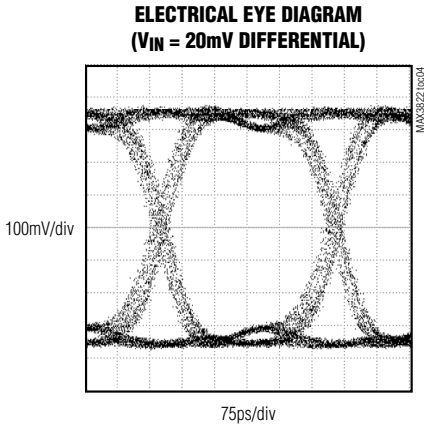
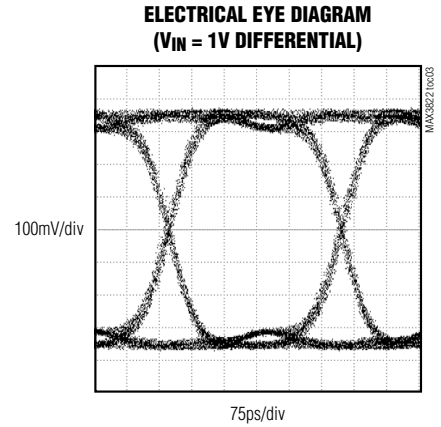
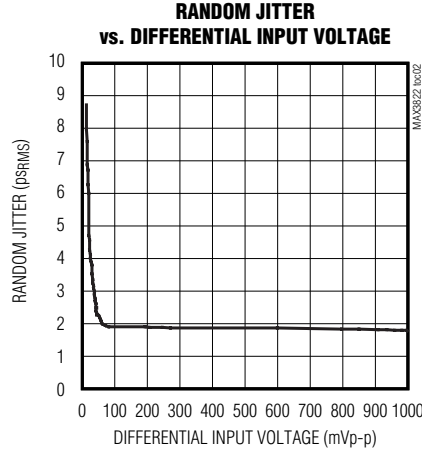
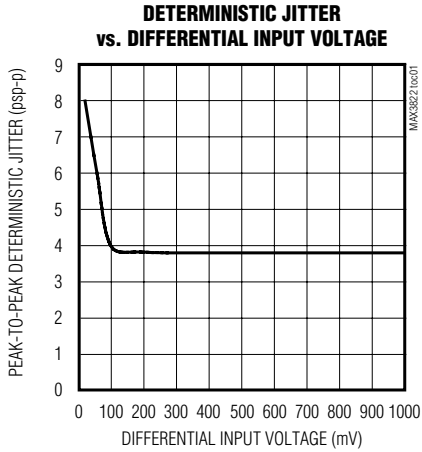
Note 7: Input-referred noise is specified (differential output noise)/(small-signal gain).

Note 8: Measured by applying the same input signal to all channels. Skew measurements are made at 50% point of the transition.

+3.3V, 2.5Gbps Quad Limiting Amplifier

Typical Operating Characteristics

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



+3.3V, 2.5Gbps Quad Limiting Amplifier

Pin Description

MAX3822

PIN	NAME	DESCRIPTION
1	IN1+	Noninverted Data Input for Channel 1
2	IN1-	Inverted Data Input for Channel 1
3, 6, 7, 10, 27, 30, 31, 34	VCC	+3.3V Supply Voltage
4	IN2+	Noninverted Data Input for Channel 2
5	IN2-	Inverted Data Input for Channel 2
8	IN3+	Noninverted Data Input for Channel 3
9	IN3-	Inverted Data Input for Channel 3
11	IN4+	Noninverted Data Input for Channel 4
12	IN4-	Inverted Data Input for Channel 4
13, 16, 19, 37, 39, 40, 42, 45, 48	GND	Supply Ground
14	CZ4-	A capacitor connected between this pin and CZ4+ extends the time constant for the offset-correction loop associated with channel 4. Maxim recommends a capacitor value of 0.033μF.
15	CZ4+	A capacitor connected between this pin and CZ4- extends the time constant for the offset-correction loop associated with channel 4. Maxim recommends a capacitor value of 0.033μF.
17	CZ3-	A capacitor connected between this pin and CZ3+ extends the time constant for the offset-correction loop associated with channel 3. Maxim recommends a capacitor value of 0.033μF.
18	CZ3+	A capacitor connected between this pin and CZ3- extends the time constant for the offset-correction loop associated with channel 3. Maxim recommends a capacitor value of 0.033μF.
20	$\overline{\text{LOP}}$	LOP is low when any of the individual power detectors ($\overline{\text{LOP1}}$, $\overline{\text{LOP2}}$, $\overline{\text{LOP3}}$, $\overline{\text{LOP4}}$) are low.
21	$\overline{\text{LOP1}}$	$\overline{\text{LOP1}}$ asserts low when the data input signal level to channel 1 drops below the programmed threshold.
22	$\overline{\text{LOP2}}$	$\overline{\text{LOP2}}$ asserts low when the data input signal level to channel 2 drops below the programmed threshold.
23	$\overline{\text{LOP3}}$	$\overline{\text{LOP3}}$ asserts low when the data input signal level to channel 3 drops below the programmed threshold.
24	$\overline{\text{LOP4}}$	$\overline{\text{LOP4}}$ asserts low when the data input signal level to channel 4 drops below the programmed threshold.
25	OUT4-	Inverted Data Output for Channel 4

+3.3V, 2.5Gbps Quad Limiting Amplifier

Pin Description (continued)

PIN	NAME	DESCRIPTION
26	OUT4+	Noninverted Data Output for Channel 4
28	OUT3-	Inverted Data Output for Channel 3
29	OUT3+	Noninverted Data Output for Channel 3
32	OUT2-	Inverted Data Output for Channel 2
33	OUT2+	Noninverted Data Output for Channel 2
35	OUT1-	Inverted Data Output for Channel 1
36	OUT1+	Noninverted Data Output for Channel 1
38	VTH	A resistor connected from this pin to ground sets the data input signal level at which the loss-of-power outputs will be asserted.
41	CS	Channel-Select Input. To enable channel 1 only, leave CS open. To enable channels 1 and 2, connect CS to V _{CC} . To enable all four channels, connect CS to GND.
43	CZ2-	A capacitor connected between this pin and CZ2+ extends the time constant for the offset-correction loop associated with channel 2. Maxim recommends a capacitor value of 0.033 μ F.
44	CZ2+	A capacitor connected between this pin and CZ2- extends the time constant for the offset-correction loop associated with channel 2. Maxim recommends a capacitor value of 0.033 μ F.
46	CZ1-	A capacitor connected between this pin and CZ1+ extends the time constant for the offset-correction loop associated with channel 1. Maxim recommends a capacitor value of 0.033 μ F.
47	CZ1+	A capacitor connected between this pin and CZ1- extends the time constant for the offset-correction loop associated with channel 1. Maxim recommends a capacitor value of 0.033 μ F.
EP	Exposed Pad	Ground. This must be soldered to a circuit board for proper thermal and electrical performance (see <i>Exposed Pad (EP) Package</i>).

Detailed Description

The MAX3822 is a 2.5Gbps quad limiting amplifier designed for fiber applications with input sensitivities as low as 20mVp-p. This device has internally terminated CML inputs with loss-of-power circuitry for each channel, as well as a general loss-of-power indicator valid for the whole part. Offset correction ensures low pulse-width distortion (PWD) and reduced pattern-dependent jitter (PDJ). A channel-select (CS) pin is used to control the device's mode of operation as single, dual, or quad.

The inputs of the MAX3822 are typically connected to a transimpedance amplifier (TIA) (MAX3825) found within a fiber-optic link. The output signal from a TIA can contain significant amounts of noise, and may vary in amplitude over time. The MAX3822 limiting amplifier quantizes the input signal, and outputs a voltage-limited waveform over a 40dB input dynamic range. Signal input to this device passes through a buffer to a linear-gain amplifier. This linear-gain amplifier (Figure 1) drives the power-detection circuitry and a chain of limiting amplifiers leading to the CML output buffer.

The power-detection circuitry is used to indicate that the data input voltage has fallen below the programmed threshold level. Each individual channel has a power detector output (LOP1, LOP2, LOP3, LOP4). The LOP output is low when any of the individual power-detector outputs are low. A threshold adjustment pin (VTH) programs the signal-detect threshold for all four channels with a single external resistor. The offset-correction loop adjusts the input buffer bias until the CML output buffer has a zero offset. This offset-correction loop acts as a high-pass filter where signal components below 150kHz are attenuated.

Input Buffer and Gain Stages

The MAX3822's inputs are terminated with 50 Ω to V_{CC} (Figure 2). The inputs do not need to be AC-coupled if the upstream TIA has CML outputs, but should be AC-coupled if the differential logic levels are in any other format. The differential input signal is passed through a buffer, and then continues through two sets of differential amplifiers, each with an emitter-follower output stage. The first differential amplifier provides approximately 10dB gain and a linear output for input signals

+3.3V, 2.5Gbps Quad Limiting Amplifier

MAX3822

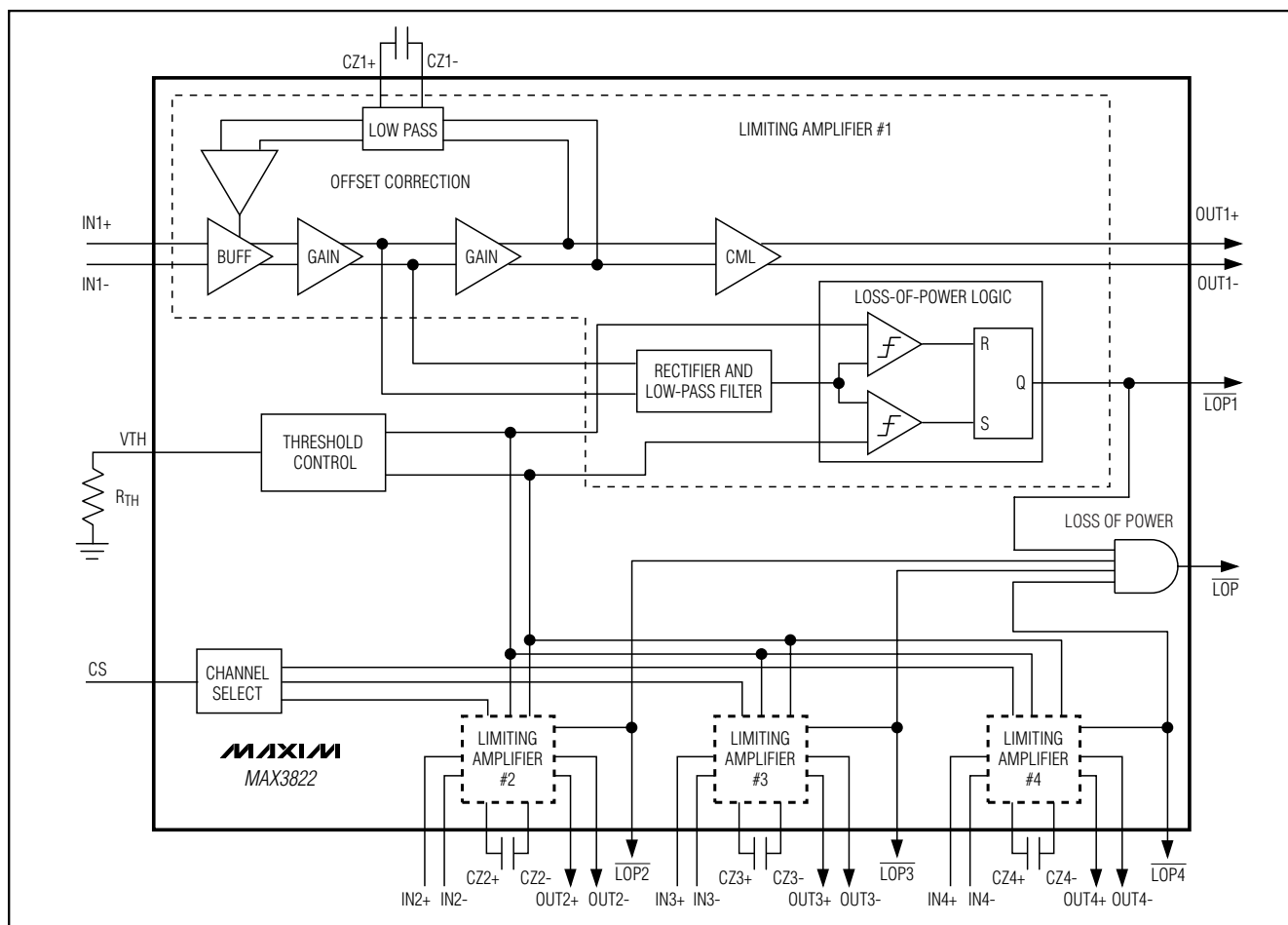


Figure 1. Functional Diagram

up to 80mVp-p. This differential amplifier is designed to work with the power-detect circuitry.

The next high-gain amplifier provides an additional gain of approximately 22dB. This gain stage functions similarly to the input-gain stage. The output signal from this gain stage is applied to the CML output buffer shown in Figure 3, and is used in the offset-correction loop.

The input voltage range is limited to $V_{CC} + 0.5V$ by the ESD structure, and to a minimum of $V_{CC} - 1V$ by the internal resistor. Figure 2 shows a model of the input stage of the MAX3822, including the package capacitance and the bond wire inductance. The additional 0.4pF capacitance on the inputs represents the ESD diode's junction capacitance and a small contribution by the bond pad. For more information about the CML electrical specifications and interfacing to other proto-

cols, refer to Application Note HFAN-1.0, *Introduction to LVDS, PECL, and CML*.

Be sure the MAX3822 is placed as close as possible to the TIA when using this device near sensitivity. If you are using a TIA with CML outputs, such as the MAX3825, AC-coupling capacitors are not required. Taking these precautions will ensure the best possible sensitivity.

Output Buffer

The MAX3822's CML output buffer is designed to drive 50Ω lines that are used to feed the input of a clock- and data-recovery device (CDR). Figure 3 shows a model of the output stage showing some important details. The outputs of the device are terminated internally with 50Ω to V_{CC} . ESD diode structures are connected to V_{CC} and GND. Figure 3 also shows the model of the output

+3.3V, 2.5Gbps Quad Limiting Amplifier

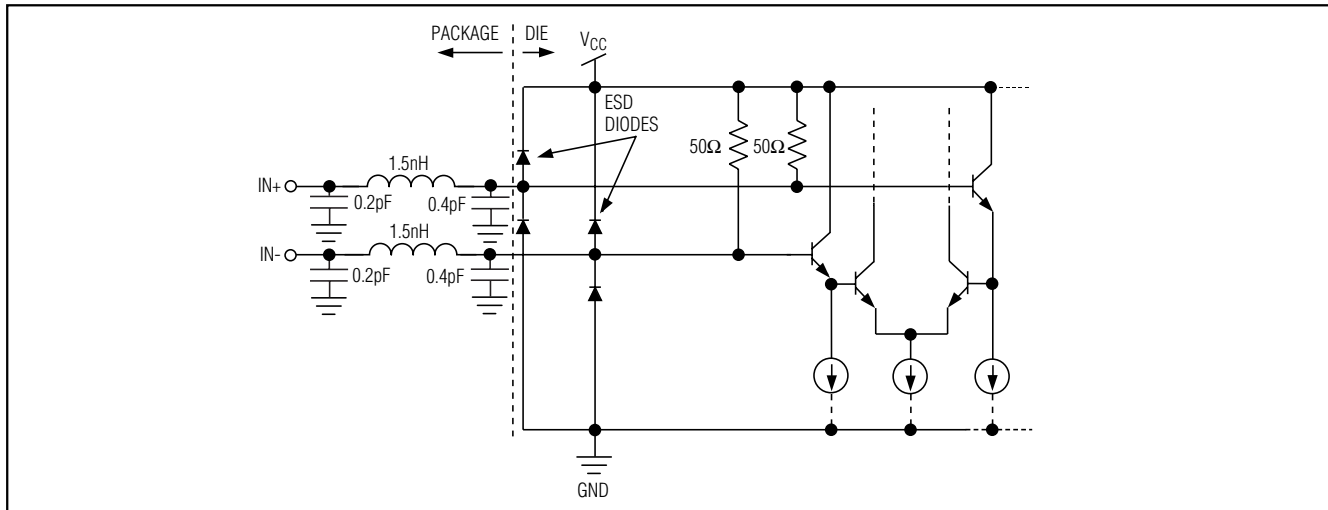


Figure 2. Input Structure

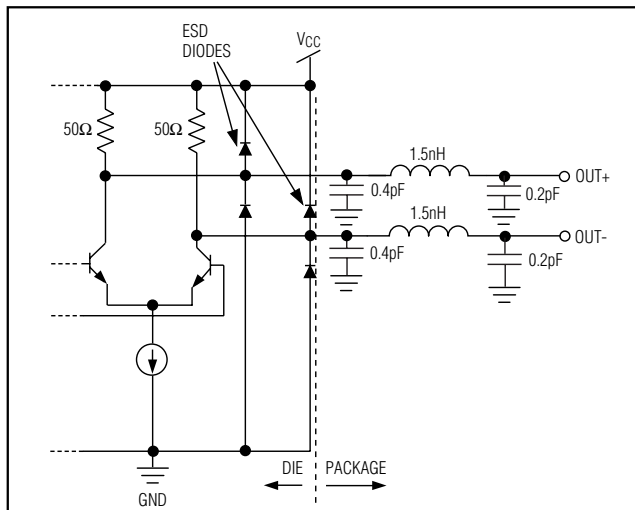


Figure 3. Output Structure

stage of the MAX3822, including package capacitance and bond-wire inductance. The additional 0.4pF capacitance on the output represents the ESD diode's junction capacitance and a small contribution by the bond pad. For more information about the CML electrical specifications and interfacing to other protocols, refer to Application Note HFAN-1.0, *Introduction to LVDS, PECL, and CML*.

Offset Correction

Each limiting amplifier on the MAX3822 provides approximately 50dB of gain. An input offset as small as 1mV reduces the power-detection circuitry's accuracy

and may cause deterministic jitter through an increase of PWD.

Each of the MAX3822's integrated limiting amplifiers includes a DC cancellation loop that provides offset correction to the CML output signal in addition to low-frequency power-supply noise rejection. The DC cancellation loop consists of a low-pass filter and a high-gain amplifier. The input voltage difference of the CML output buffer is amplified, sent through a low-pass filter, inverted, and summed up with the input signal that drives the high-gain input stage. This removes from the output signal all frequency components between the cutoff frequency and DC. The low-frequency cutoff of the DC cancellation loop is set by an external capacitor connected between CZ₊ and CZ₋.

Power Detection and Threshold Control

The MAX3822 incorporates a chatter-free loss-of-power function that is used to determine if the input signal has dropped below the programmed threshold level. The power detector is implemented by comparing the DC-rectified output of the first gain stage to the programmed loss-of-power threshold.

The threshold control circuitry enables programming of $\overline{\text{LOP}}_{\text{assert}}$ and deassert reference voltages by using one external resistor, R_{TH} (Figure 4). An internal amplifier guarantees a voltage at V_{TH} of approximately 0.5V. The external resistor (R_{TH}) connected to GND converts this voltage into a current. The current through this resistor sets the power threshold level for the device (see *Typical Operating Characteristics, Loss-of-Power Threshold Level vs. R_{TH}*).

+3.3V, 2.5Gbps Quad Limiting Amplifier

Loss-Of-Power Logic (LOP)

The loss-of-power logic circuitry is asserted anytime the input power of one of the limiting amplifiers is observed below the threshold set by R_{TH} . The logic of this is comprised of two comparators and an S-R flip-flop to compare the outputs of the threshold-control and power-detect circuitry for each of the limiting amplifiers on the MAX3822. The \overline{LOP}_- output corresponding to a given input is asserted if the input power is too low. A general \overline{LOP} output is also given for the whole part; if any \overline{LOP}_- signal is low, the \overline{LOP} output will also go low.

Once a \overline{LOP}_- signal has been asserted, the input power must rise above the threshold before resetting. This prevents the \overline{LOP}_- output from turning on and off when the input signal is near the programmed threshold level, an effect called chatter. The \overline{LOP}_- indicator will return to its unasserted state when the input power level is increased (4dB typ). Figure 5 shows the output structure.

Channel Select

The channel-select circuitry controls the operating mode of the MAX3822 by shutting down unused amplifiers. Single-, dual-, and quad-mode operation is programmed by the channel-select (CS) pin. When CS is left open, the

device is placed into single-mode operation with channel 1 enabled, and channels 2, 3, and 4 disabled. Dual-mode operation is programmed by connecting CS directly to V_{CC} . In dual-mode operation, channels 1 and 2 are enabled and channels 3 and 4 are disabled. Quad-mode operation is programmed by connecting CS directly to GND. In quad-mode operation, all four channels are enabled. Figure 6 shows the input circuitry of the CS pin.

Applications Information

Set Up the DC Cancellation Loop

The value of the offset-correction capacitor (CZ_) affects the maximum speed at which the DC cancellation loop can adjust to changes in DC offset at the input. PWD and pattern-dependent jitter (PDJ) are both error sources that can be minimized by the proper selection of CZ_. Therefore, the loop should be as slow as possible to reduce PDJ while performing its DC cancellation function. Select the CZ_ capacitor to set the bandwidth of the DC cancellation loop. The input impedance between CZ+ and CZ- is approximately 10k Ω . This impedance is in series with CZ_. Therefore, the low-frequency cutoff (foc) associated with the DC offset-correction loop is computed as follows:

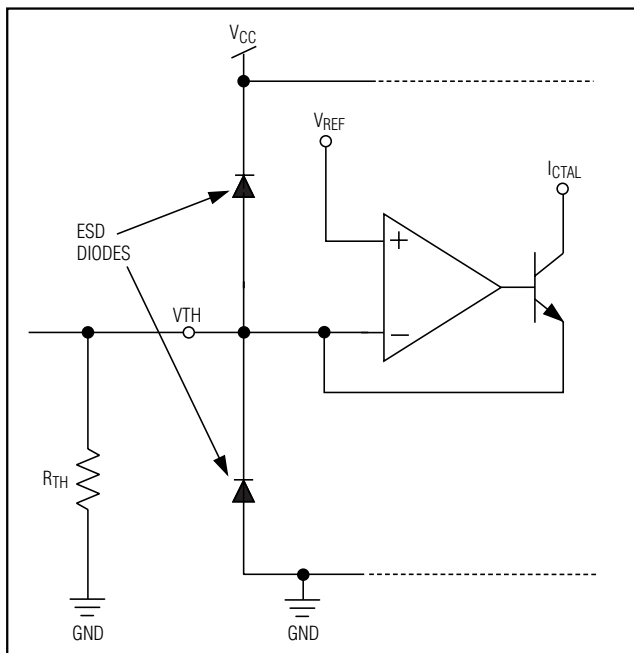


Figure 4. Threshold Set Structure

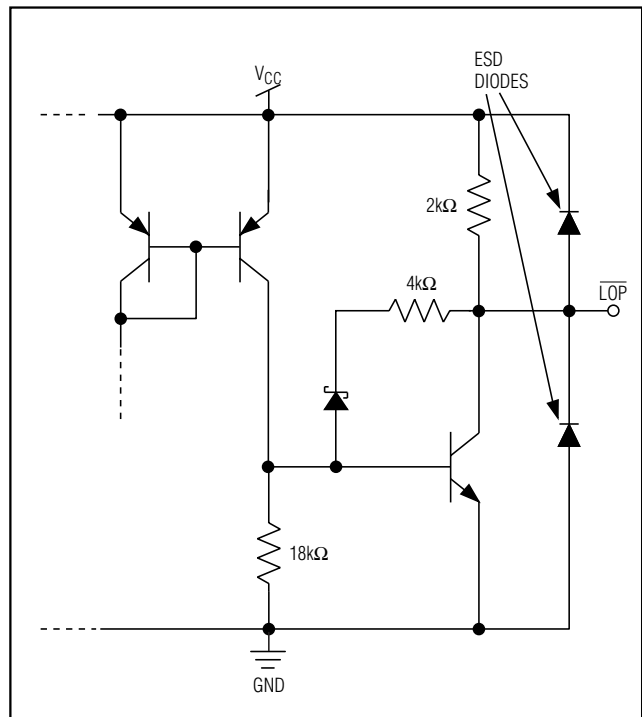


Figure 5. TTL Output Structure

+3.3V, 2.5Gbps Quad Limiting Amplifier

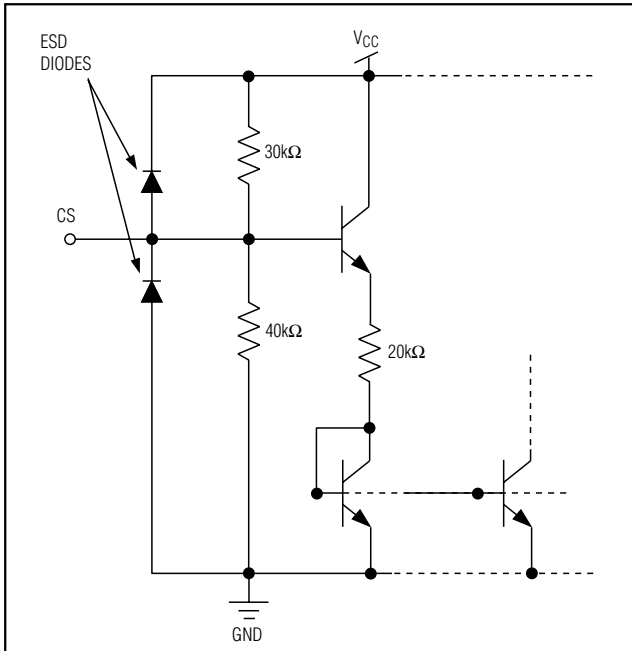


Figure 6. Channel-Select Interface

$$f_{oc} = \frac{10^{\frac{50dB}{20}}}{2\pi \times 10k\Omega \times C_{z-}}$$

where 50dB is the gain of the offset-correction loop. Maxim recommends a value of 0.033μF for the filter capacitor. This value will set the lower cutoff frequency of the DC cancellation loop to approximately 150kHz.

Optical Hysteresis

Power and hysteresis are often expressed in decibels. By definition, decibels are always 10log (ratio power). At the inputs to the MAX3822 limiting amplifier, the power is V_{IN}^2 / R . If a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage input to the MAX3822 will also increase by a factor of two.

The optical power change is:

$$10\log \frac{2x}{x} = 10\log(2) = +3dB$$

At the MAX3822, the voltage change is:

$$10\log \frac{(2V_{IN})^2 / R}{V_{IN}^2 / R} = 10\log(2^2) = 20\log(2) = +6dB$$

In an optical receiver, the dB change at the MAX3822 will equal twice the optical dB change. The MAX3822's typical voltage hysteresis is 4dB. This provides an optical hysteresis of 2dB.

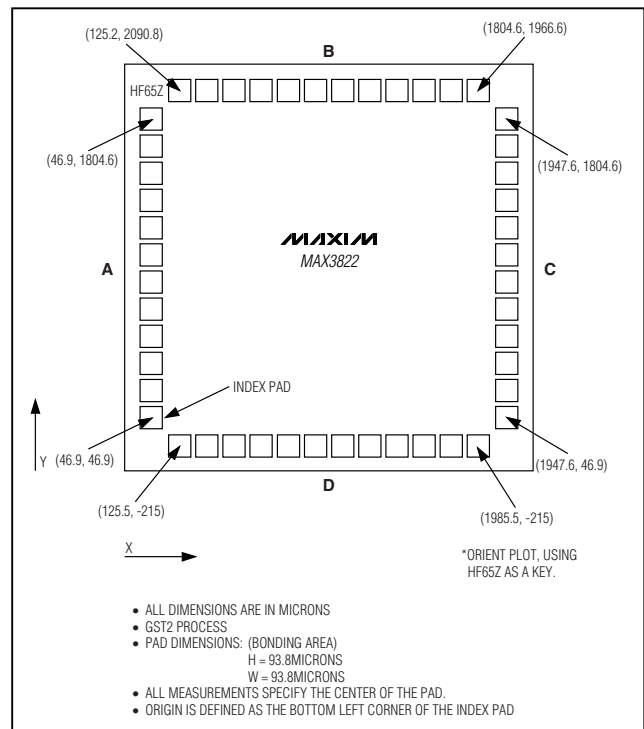
Exposed-Pad (EP) Package

The exposed-pad, 48-pin TQFP-EP incorporates features that provide a very low thermal resistance path for heat removal from the IC. The pad is electrical ground on the MAX3822 and should be soldered to the circuit board for proper thermal and electrical performance.

Chip Information

TRANSISTOR COUNT: 813
 SUBSTRATE CONNECTED TO GND
 PROCESS: Bipolar
 DIE SIZE: 90mil × 102mil

Bond Pad Information



- ALL DIMENSIONS ARE IN MICRONS
- GST2 PROCESS
- PAD DIMENSIONS: (BONDING AREA)
 H = 93.8MICRONS
 W = 93.8MICRONS
- ALL MEASUREMENTS SPECIFY THE CENTER OF THE PAD.
- ORIGIN IS DEFINED AS THE BOTTOM LEFT CORNER OF THE INDEX PAD

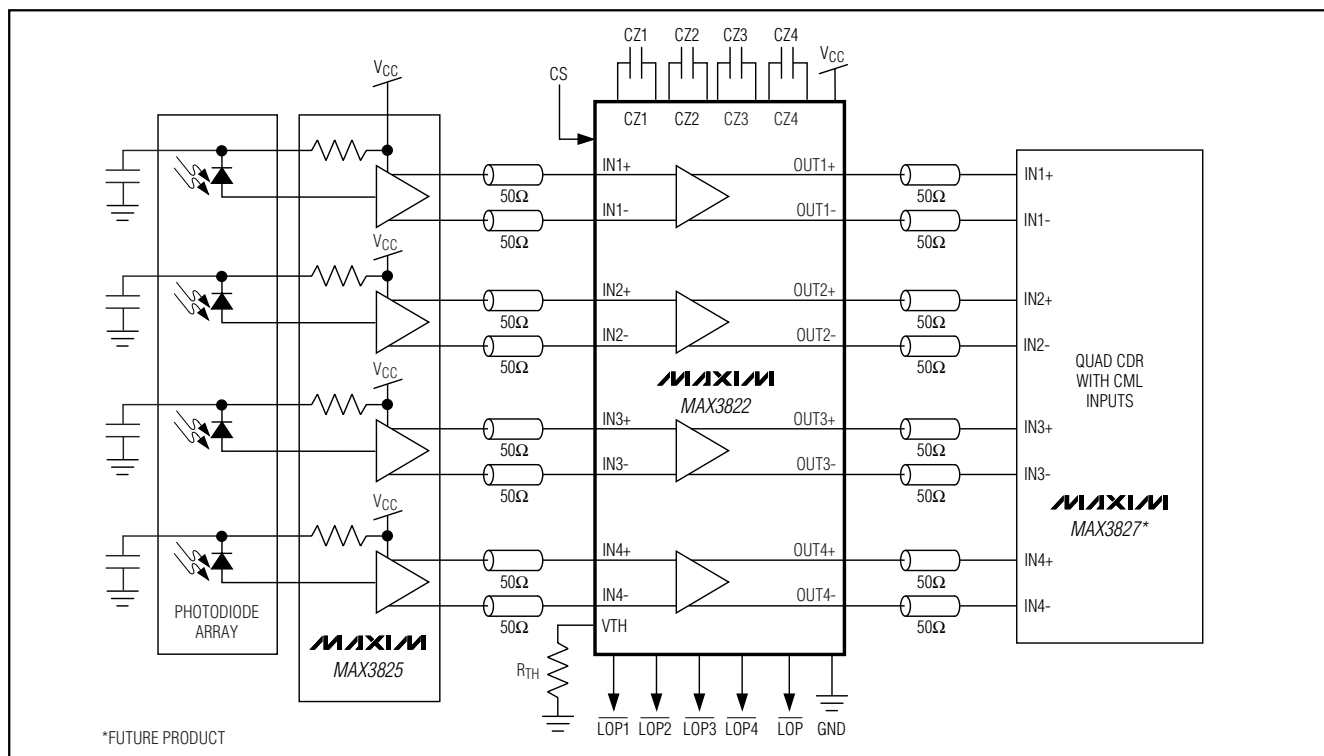
+3.3V, 2.5Gbps Quad Limiting Amplifier

Bond Pad Information (continued)

MAX3822

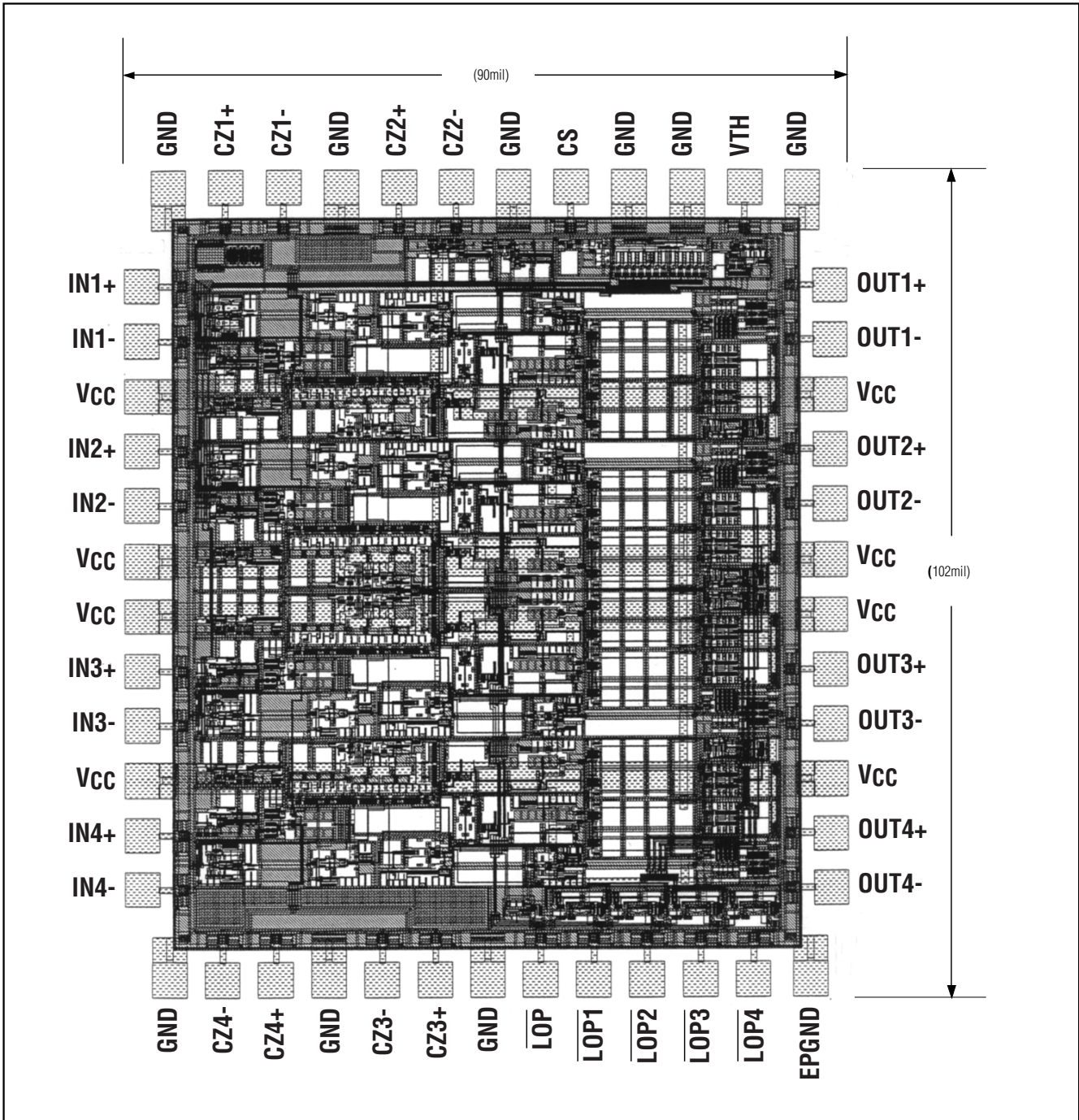
MAX3822 (HF65Z) DIMENSIONS							
SIDE A		SIDE B		SIDE C		SIDE D	
46.9	46.9	125.2	2090.8	1947.6	46.9	125.2	-215
46.9	206.2	292.6	2090.8	1947.6	206.2	279.1	-215
46.9	365.5	460.0	2090.8	1947.6	365.5	433.0	-215
46.9	524.8	627.4	2090.8	1947.6	524.8	586.9	-215
46.9	684.1	794.8	2090.8	1947.6	684.1	740.8	-215
46.9	846.1	962.2	2090.8	1947.6	846.1	894.7	-215
46.9	1005.4	1129.6	2090.8	1947.6	1005.4	1048.6	-215
46.9	1167.4	1297.0	2090.8	1947.6	1167.4	1202.5	-215
46.9	1326.7	1464.4	2090.8	1947.6	1326.7	1356.4	-215
46.9	1486.0	1631.8	2090.8	1947.6	1486.0	1510.3	-215
46.9	1645.3	1799.2	2090.8	1947.6	1645.3	1664.2	-215
46.9	1804.6	1966.6	2090.8	1947.6	1804.6	1818.1	-215
						1985.5	-215

Typical Operating Circuit



+3.3V, 2.5Gbps Quad Limiting Amplifier

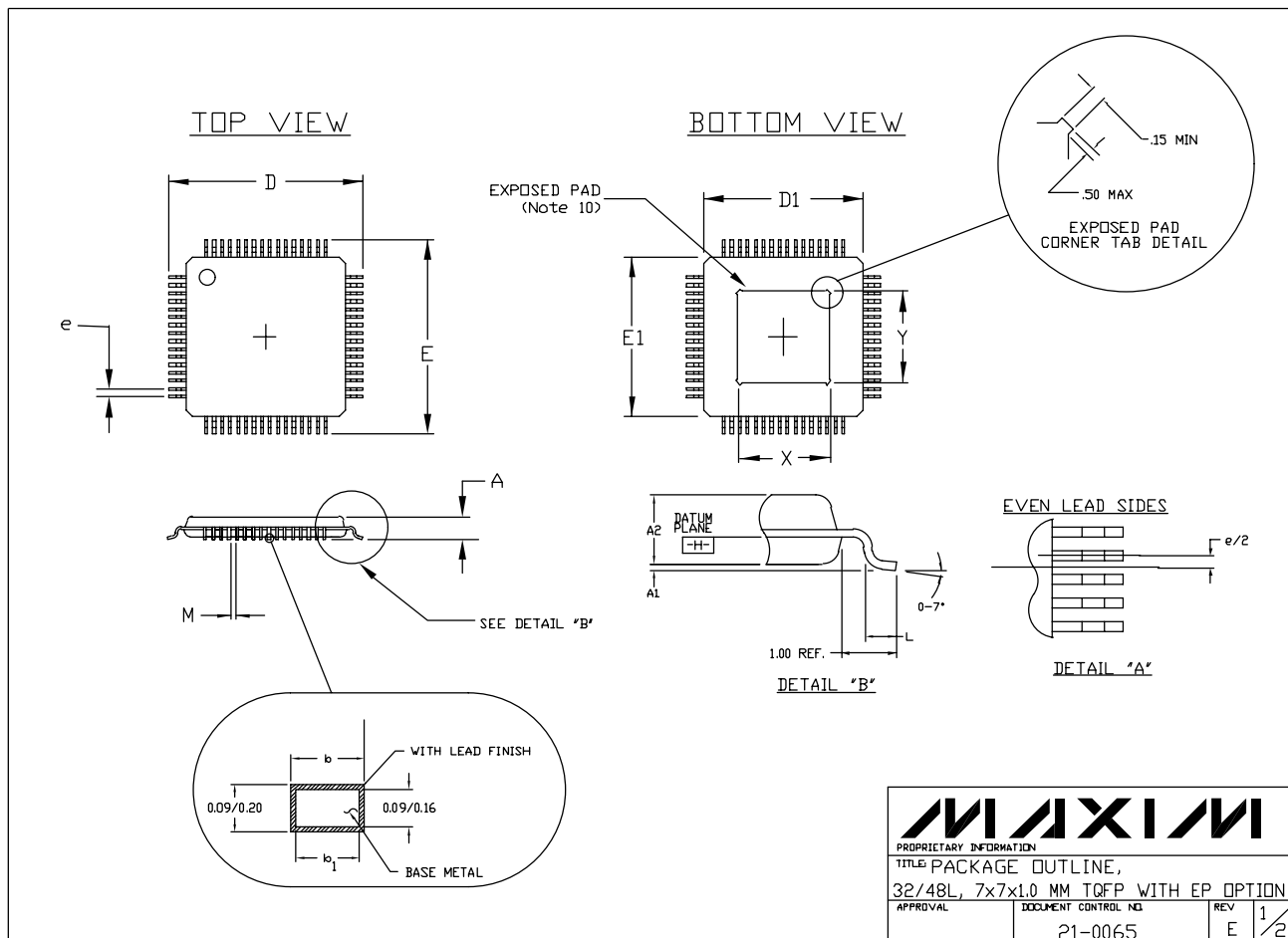
Chip Topography



+3.3V, 2.5Gbps Quad Limiting Amplifier

Package Information

MAX3822



+3.3V, 2.5Gbps Quad Limiting Amplifier


Package Information (continued)

NOTES:

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE $\square-H-$ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS AC AND AE.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION					
	ALL DIMENSIONS IN MILLIMETERS					
	AC			AE		
	MIN.	NDM.	MAX.	MIN.	NDM.	MAX.
A	$\cancel{0.05}$	$\cancel{0.10}$	1.20	$\cancel{0.05}$	$\cancel{0.10}$	1.20
A ₁	0.05	0.10	0.15	0.05	0.10	0.15
A ₂	0.95	1.00	1.05	0.95	1.00	1.05
D	9.00 BSC.			9.00 BSC.		
D ₁	7.00 BSC.			7.00 BSC.		
E	9.00 BSC.			9.00 BSC.		
E ₁	7.00 BSC.			7.00 BSC.		
L	0.45	0.60	0.75	0.45	0.60	0.75
M	0.15	$\cancel{0.15}$	$\cancel{0.15}$	0.14	$\cancel{0.15}$	$\cancel{0.15}$
N	32			48		
e	0.80 BSC.			0.50 BSC.		
b	0.30	0.37	0.45	0.17	0.22	0.27
b ₁	0.30	0.35	0.40	0.17	0.20	0.23
*X	3.20	3.50	3.80	3.70	4.00	4.30
*Y	3.20	3.50	3.80	3.70	4.00	4.30

* EXPOSED PAD
(Note 10)

			
<small>PROPRIETARY INFORMATION</small>			
TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.0 MM TQFP WITH EP OPTION			
<small>APPROVAL</small>	<small>DOCUMENT CONTROL NO.</small>	<small>REV</small>	<small>2/2</small>
	21-0065	E	

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.