

# MAXIM

## Programmable DC-Balance 21-Bit Deserializers

### General Description

The MAX9210/MAX9212/MAX9214/MAX9216 deserialize three LVDS serial data inputs into 21 single-ended LVCMOS/LVTTL outputs. A parallel rate LVDS clock received with the LVDS data streams provides timing for deserialization. The outputs have a separate supply, allowing 1.8V to 5V output logic levels.

The MAX9210/MAX9212/MAX9214/MAX9216 feature programmable DC balance, which allows isolation between serializer and deserializer using AC-coupling. A deserializer decodes data transmitted by a MAX9209/MAX9211/MAX9213/MAX9215 serializer. When DC balance is not programmed, the deserializers are compatible with non-DC-balanced 21-bit deserializers like the DS90CR216A and DS90CR218A.

Two frequency versions and two DC-balance default conditions are available for maximum replacement flexibility and compatibility with popular non-DC balanced serializers. The transition time of the single-ended outputs is increased on the low-frequency version parts (MAX9210/MAX9212) for reduced EMI.

The MAX9210/MAX9212/MAX9214/MAX9216 are available in TSSOP and space-saving thin QFN packages, and operate over the -40°C to +85°C temperature range.

### Applications

Automotive Navigation Systems  
Automotive DVD Entertainment Systems  
Digital Copiers  
Laser Printers

### Features

- ◆ Programmable DC Balance or Non-DC Balance
- ◆ DC Balance Allows AC-Coupling for Wider Input Common-Mode Voltage Range
- ◆ As Low as 8MHz Operation (MAX9210/MAX9212)
- ◆ Slower Output Transitions for Reduced EMI (MAX9210/MAX9212)
- ◆ High-Impedance Outputs when PWRDWN Is Low Allow Output Busing
- ◆ Pin Compatible with DS90CR216A/DS90CR218A
- ◆ Fail-Safe Inputs in Non-DC-Balanced Mode
- ◆ 5V Tolerant PWRDWN Input
- ◆ PLL Requires No External Components
- ◆ Up to 1.785Gbps Throughput
- ◆ Separate Output Supply Pins Allow Interface to 1.8V, 2.5V, 3.3V, and 5V Logic
- ◆ LVDS Inputs Meet IEC 61000-4-2 Level 4 ESD Requirements
- ◆ LVDS Inputs Conform to ANSI TIA/EIA-644 LVDS Standard
- ◆ Low-Profile 48-Lead TSSOP and Space-Saving QFN Packages
- ◆ +3.3V Main Supply
- ◆ -40°C to +85°C Operating Temperature Range

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
<b>MAX9210ETM*</b>	-40°C to +85°C	48 Thin QFN-EP**
MAX9210EUM*	-40°C to +85°C	48 TSSOP
<b>MAX9212ETM*</b>	-40°C to +85°C	48 Thin QFN-EP**
MAX9212EUM*	-40°C to +85°C	48 TSSOP
<b>MAX9214ETM*</b>	-40°C to +85°C	48 Thin QFN-EP**
MAX9214EUM	-40°C to +85°C	48 TSSOP
<b>MAX9216ETM*</b>	-40°C to +85°C	48 Thin QFN-EP**
MAX9216EUM*	-40°C to +85°C	48 TSSOP

\*Future product—contact factory for availability.

\*\*EP = Exposed pad.

Functional Diagram and Pin Configurations appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at

1-800-282-6212, or visit [Maxim/Dallas Direct!](#) on the web at [www.maxim-dallas.com](#).

# Programmable DC-Balance 21-Bit Deserializers

## ABSOLUTE MAXIMUM RATINGS

V <sub>CC</sub> to GND	-0.5V to +4.0V
V <sub>CCO</sub> to GND	-0.5V to +6.0V
RxIN <sub>l</sub> , RxCLK IN <sub>l</sub> to GND	-0.5V to +4.0V
PWRDWN to GND	-0.5V to +6.0V
DCB/NC to GND	-0.5V to (V <sub>CC</sub> + 0.5V)
RxOUT <sub>l</sub> , RxCLK OUT to GND	-0.5V to (V <sub>CCO</sub> + 0.5V)
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
48-Pin TSSOP (derate 16mW/°C above +70°C)	1282mW
48-Lead Thin QFN (derate 26.3mW/°C above +70°C)	2105mW
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3.0V to +3.6V, V<sub>CCO</sub> = +3.0V to +5.5V, PWRDWN = high, DCB/NC = high or low, differential input voltage |V<sub>ID</sub>| = 0.05V to 1.2V, input common-mode voltage V<sub>CM</sub> = |V<sub>ID</sub>/2| to 2.4V - |V<sub>ID</sub>/2|, T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at V<sub>CC</sub> = V<sub>CCO</sub> = +3.3V, |V<sub>ID</sub>| = 0.2V, V<sub>CM</sub> = 1.25V, T<sub>A</sub> = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SINGLE-ENDED INPUTS (PWRDWN, DCB/NC)</b>						
High-Level Input Voltage	V <sub>IH</sub>	PWRDWN	2.0	5.5		V
		DCB/NC	2.0	V <sub>CC</sub> + 0.3		
Low-Level Input Voltage	V <sub>IL</sub>		-0.3	+0.8		V
Input Current	I <sub>IN</sub>	V <sub>IN</sub> = high or low, PWRDWN = high or low	-20	+20		µA
Input Clamp Voltage	V <sub>CL</sub>	I <sub>CL</sub> = -18mA		-1.5		V
<b>SINGLE-ENDED OUTPUTS (RxOUT<sub>l</sub>, RxCLK OUT)</b>						
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100µA	V <sub>CCO</sub> - 0.1			V
		I <sub>OH</sub> = -2mA	V <sub>CCO</sub> - 0.25			
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100µA		0.1		V
		I <sub>OL</sub> = 2mA		0.2		
High-Impedance Output Current	I <sub>OZ</sub>	PWRDWN = low, V <sub>OUT</sub> = -0.3V to V <sub>CCO</sub> + 0.3V	-20	+20		µA
Output Short-Circuit Current <b>Note:</b> Short one output at a time.	I <sub>OS</sub>	V <sub>CCO</sub> = 3.0V to 3.6V, V <sub>OUT</sub> = 0V	-10	-40		mA
		V <sub>CCO</sub> = 4.5V to 5.5V, V <sub>OUT</sub> = 0V	-28	-75		
<b>LVDS INPUTS</b>						
Differential Input High Threshold	V <sub>TH</sub>			50		mV
Differential Input Low Threshold	V <sub>TL</sub>		-50			mV

# Programmable DC-Balance 21-Bit Deserializers

## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = +3.0V$  to  $+3.6V$ ,  $V_{CCO} = +3.0V$  to  $+5.5V$ ,  $\overline{PWRDWN} = \text{high}$ ,  $\text{DCB/NC} = \text{high or low}$ , differential input voltage  $|V_{ID}| = 0.05V$  to  $1.2V$ , input common-mode voltage  $V_{CM} = |V_{ID}/2|$  to  $2.4V - |V_{ID}/2|$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC} = V_{CCO} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.25V$ ,  $T_A = +25^\circ\text{C}$ .) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current	$I_{IN+}$ , $I_{IN-}$	$\overline{PWRDWN} = \text{high or low}$	-25	+25		$\mu\text{A}$
Power-Off Input Current	$I_{INO+}$ , $I_{INO-}$	$V_{CC} = V_{CCO} = 0V$ or open, $\text{DCB/NC}$ , $\overline{PWRDWN} = 0V$ or open	-25	+25		$\mu\text{A}$
Input Resistor 1	$R_{IN1}$	$\overline{PWRDWN} = \text{high or low}$ (Figure 1)	42	78	$\text{k}\Omega$	
		$V_{CC} = V_{CCO} = 0V$ or open (Figure 1)				
Input Resistor 2	$R_{IN2}$	$\overline{PWRDWN} = \text{high or low}$ (Figure 1)	246	410	$\text{k}\Omega$	
		$V_{CC} = V_{CCO} = 0V$ or open (Figure 1)				
<b>POWER SUPPLY</b>						
Worst-Case Supply Current	$I_{CCW}$	$C_L = 8\text{pF}$ , worst-case pattern, DC-balanced mode; $V_{CC} = V_{CCO} = 3.0V$ to $3.6V$ , Figure 2	16MHz	52	63	mA
			34MHz	86	106	
			66MHz	152	177	
		$C_L = 8\text{pF}$ , worst-case pattern, non-DC-balanced mode; $V_{CC} = V_{CCO} = 3.0V$ to $3.6V$ , Figure 2	20MHz	53	64	
			33MHz	72	85	
			40MHz	81	99	
			66MHz	127	149	
			85MHz	159	186	
Power-Down Supply Current	$I_{CCZ}$	$\overline{PWRDWN} = \text{low}$		50		$\mu\text{A}$

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = V_{CCO} = +3.0V$  to  $3.6V$ ,  $100\text{mV}_{\text{P-P}}$  at  $200\text{kHz}$  supply noise,  $C_L = 8\text{pF}$ ,  $\overline{PWRDWN} = \text{high}$ ,  $\text{DCB/NC} = \text{high or low}$ , differential input voltage  $|V_{ID}| = 0.1V$  to  $1.2V$ , input common-mode voltage  $V_{CM} = |V_{ID}/2|$  to  $2.4V - |V_{ID}/2|$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC} = V_{CCO} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.25V$ ,  $T_A = 25^\circ\text{C}$ .) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Output Rise Time	$CLHT$	$0.1V_{CCO}$ to $0.9V_{CCO}$ , Figure 3	MAX9214/ MAX9216	2.2	3.15	3.9	ns
Output Fall Time	$CHLT$	$0.9V_{CCO}$ to $0.1V_{CCO}$ , Figure 3	MAX9214/ MAX9216	1.3	2.12	2.9	ns
RxIN Skew Margin	$RSKM$	DC-balanced mode, Figure 4 (Note 6)	16MHz	2560	3137	ps	
			34MHz	900	1327		
			66MHz	330	685		
			20MHz	2500	3300		
		Non-DC-balanced mode, Figure 4 (Note 6)	40MHz	960	1448		
			85MHz	330	685		

MAX9210/MAX9212/MAX9214/MAX9216

# Programmable DC-Balance 21-Bit Deserializers

## AC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC} = V_{CCO} = +3.0V$  to  $3.6V$ ,  $100mVp-p$  at  $200kHz$  supply noise,  $C_L = 8pF$ ,  $\overline{PWRDWN} = \text{high}$ , DCB/NC = high or low, differential input voltage  $|V_{ID}| = 0.1V$  to  $1.2V$ , input common-mode voltage  $V_{CM} = |V_{ID}/2|$  to  $2.4V - |V_{ID}/2|$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise noted. Typical values are at  $V_{CC} = V_{CCO} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.25V$ ,  $T_A = 25^\circ\text{C}$ .) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
RxCLK OUT High Time	RCOH	Figure 5	0.35 x RCOP	0.4 x RCOP		ns	
RxCLK OUT Low Time	RCOL	Figure 5	0.35 x RCOP	0.44 x RCOP		ns	
RxOUT Setup to RxCLK OUT	RSRC	Figure 5	0.30 x RCOP	0.35 x RCOP		ns	
RxOUT Hold from RxCLK OUT	RHRC	Figure 5	0.45 x RCOP	0.48 x RCOP		ns	
RxCLK IN to RxCLK OUT Delay	RCCD	Figure 6		4.9	6.17	8.1	ns
Deserializer Phase-Locked Loop Set	RPLLS	Figure 7			32800 x RCIP		ns
Deserializer Power-Down Delay	RPDD	Figure 8			100	ns	

**Note 1:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except  $V_{TH}$  and  $V_{TL}$ .

**Note 2:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at  $T_A = +25^\circ\text{C}$ .

**Note 3:** AC parameters are guaranteed by design and characterization, and are not production tested. Limits are set at  $\pm 6$  sigma.

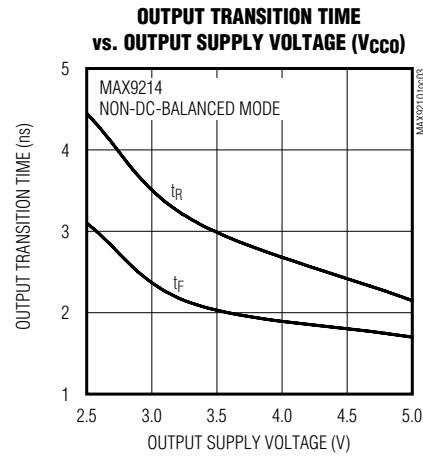
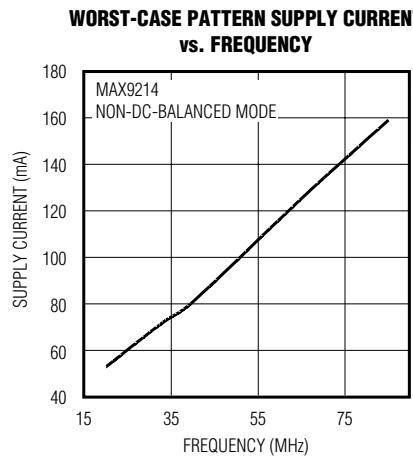
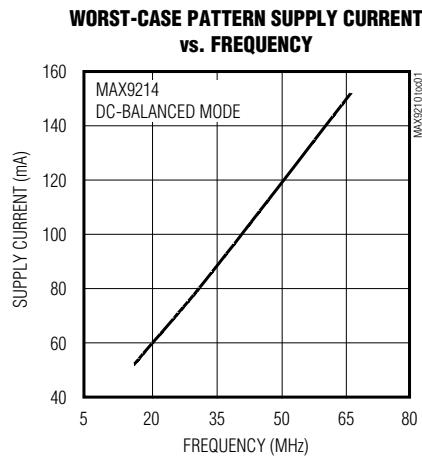
**Note 4:**  $C_L$  includes probe and test jig capacitance.

**Note 5:** RCIP is the period of RxCLK IN. RCOP is the period of RxCLK OUT. RCIP = RCOP.

**Note 6:** RSKM measured with  $\leq 150\text{ps}$  cycle-to-cycle jitter on RxCLK IN.

## Typical Operating Characteristics

( $V_{CC} = V_{CCO} = +3.3V$ ,  $C_L = 8pF$ ,  $\overline{PWRDWN} = \text{high}$ , differential input voltage  $|V_{ID}| = 0.2V$ , input common-mode voltage  $V_{CM} = 1.2V$ , unless otherwise noted.)



# Programmable DC-Balance 21-Bit Deserializers

## Pin Description

PIN		NAME	FUNCTION
TSSOP	QFN		
1, 2, 4, 5, 45, 46, 47	39, 40, 41, 43, 44, 46, 47	RxOUT14–RxOUT20	Channel 2 Single-Ended Outputs
3, 25, 32, 38, 44	19, 26, 32, 38, 45	GND	Ground
6	48	DCB/NC	LVTT/LVCMOS DC-Balance Programming Input: MAX9210: pulled up to Vcc MAX9212: pulled down to GND MAX9214: pulled up to Vcc MAX9216: pulled down to GND See Table 1.
7, 13, 18	1, 7, 12	LVDS GND	LVDS Ground
8	2	RxIN0-	Inverting Channel 0 LVDS Serial Data Input
9	3	RxIN0+	Noninverting Channel 0 LVDS Serial Data Input
10	4	RxIN1-	Inverting Channel 1 LVDS Serial Data Input
11	5	RxIN1+	Noninverting Channel 1 LVDS Serial Data Input
12	6	LVDS V <sub>CC</sub>	LVDS Supply Voltage
14	8	RxIN2-	Inverting Channel 2 LVDS Serial Data Input
15	9	RxIN2+	Noninverting Channel 2 LVDS Serial Data Input
16	10	RxCLK IN-	Inverting LVDS Parallel Rate Clock Input
17	11	RxCLK IN+	Noninverting LVDS Parallel Rate Clock Input
19, 21	13, 15	PLL GND	PLL Ground
20	14	PLL V <sub>CC</sub>	PLL Supply Voltage
22	16	PWRDWN	5V Tolerant LVTT/LVCMOS Power-Down Input. Internally pulled down to GND. Outputs are high impedance when PWRDWN = low or open.
23	17	RxCLK OUT	Parallel Rate Clock Single-Ended Output
24, 26, 27, 29, 30, 31, 33	18, 20, 21, 23, 24, 25, 27	RxOUT0–RxOUT6	Channel 0 Single-Ended Outputs
28, 36, 48	22, 30, 42	V <sub>CCO</sub>	Output Supply Voltage
34, 35, 37, 39, 40, 41, 43	28, 29, 31, 33, 34, 35, 37	RxOUT7–RxOUT13	Channel 1 Single-Ended Outputs
42	36	V <sub>CC</sub>	Digital Supply Voltage
—	EP	EP	Exposed Paddle. Solder to ground.

MAX9210/MAX9212/MAX9214/MAX9216

## Programmable DC-Balance 21-Bit Deserializers

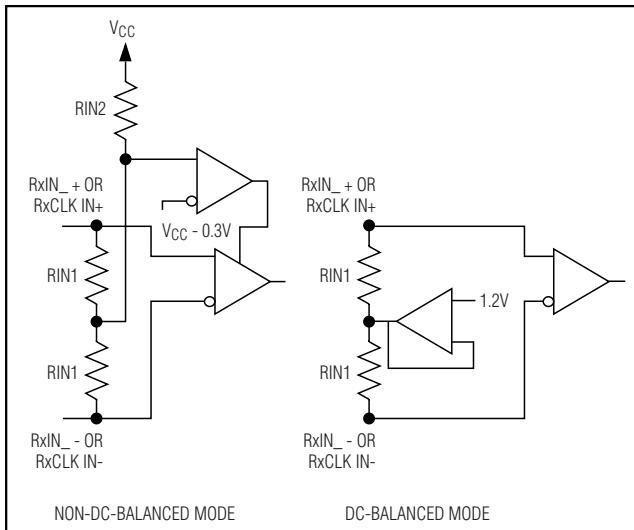


Figure 1. LVDS Input Circuits

Table 1. DC-Balance Programming

DEVICE	DCB/NC	OPERATING MODE	OPERATING FREQUENCY (MHz)
MAX9210	High or open	DC balanced	8 to 34
	Low	Non-DC balanced	10 to 40
MAX9212	High	DC balanced	8 to 34
	Low or open	Non-DC balanced	10 to 40
MAX9214	High or open	DC balanced	16 to 66
	Low	Non-DC balanced	20 to 85
MAX9216	High	DC balanced	16 to 66
	Low or open	Non-DC balanced	20 to 85

### Detailed Description

The MAX9210/MAX9212 operate at a parallel clock frequency of 8MHz to 34MHz in DC-balanced mode and 10MHz to 40MHz in non-DC-balanced mode. The MAX9214/MAX9216 operate at a parallel clock frequency of 16MHz to 66MHz in DC-balanced mode and 20MHz to 85MHz in non-DC-balanced mode. The transition times of the single-ended outputs are increased on the MAX9210/MAX9212 for reduced EMI.

DC-balanced or non-DC-balanced operation is controlled by the DCB/NC pin (see Table 1 for DCB/NC default settings and operating modes). In non-DC-balanced mode, each channel deserializes 7 bits every cycle of the parallel clock. In DC-balanced mode, 9 bits are deserialized every clock cycle (7 data bits + 2 DC-

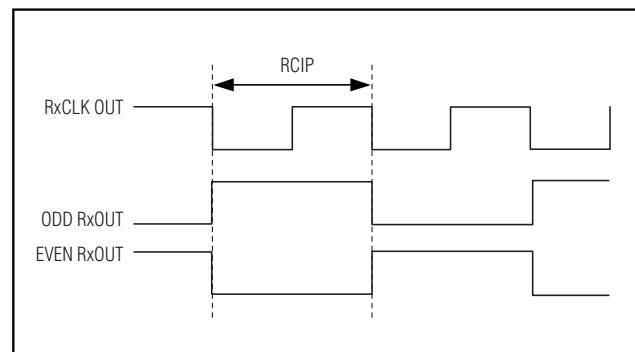


Figure 2. Worst-Case Test Pattern

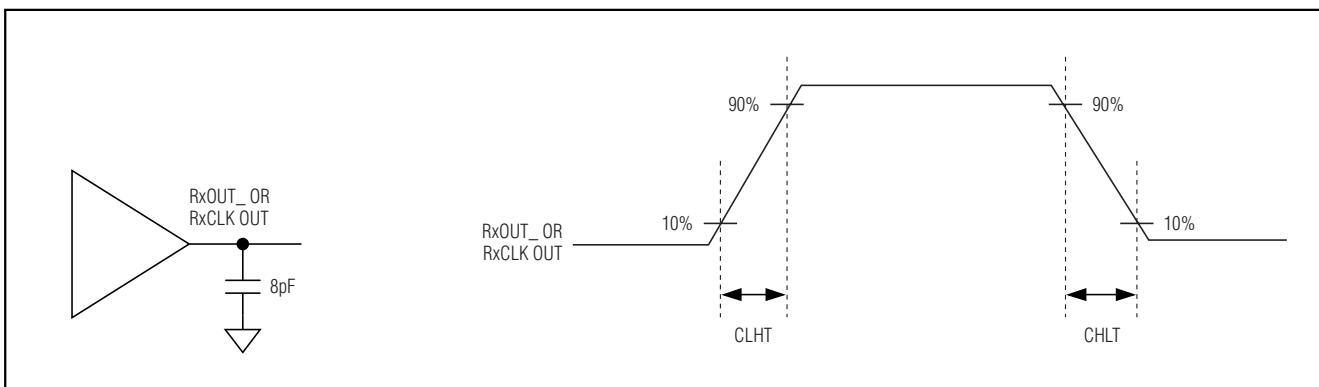


Figure 3. Output Load and Transition Times

# Programmable DC-Balance 21-Bit Deserializers

**MAX9210/MAX9212/MAX9214/MAX9216**

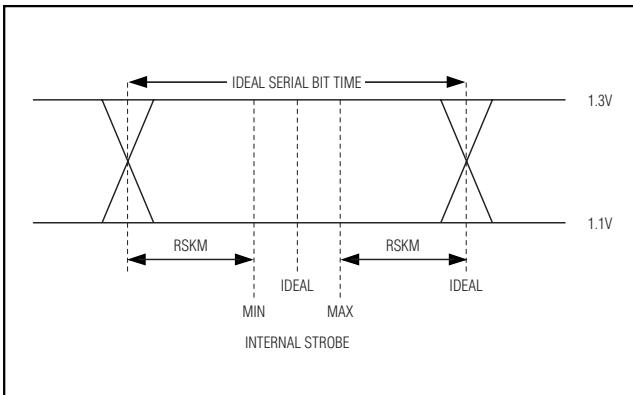


Figure 4. LVDS Receiver Input Skew Margin

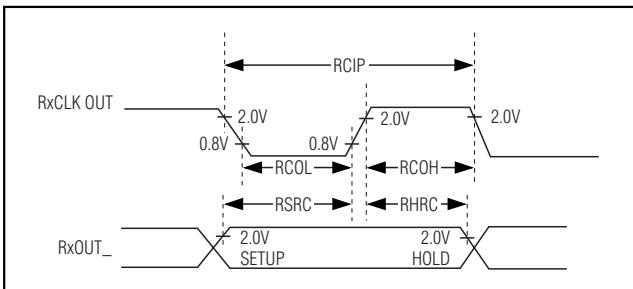


Figure 5. Output Setup/Hold and High/Low Times

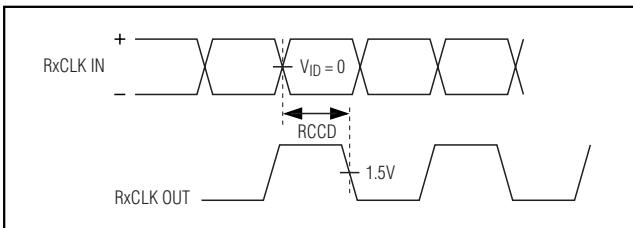


Figure 6. Clock-IN to Clock-OUT Delay

balance bits). The highest data rate in DC-balanced mode for the MAX9214 or MAX9216 is 66MHz x 7 = 594Mbps. In non-DC-balanced mode, the maximum data rate is 85MHz x 7 = 595Mbps.

## DC Balance

Data coding by the MAX9210/MAX9212/MAX9214/MAX9216 serializers (which are companion devices to the MAX9209/MAX9211/MAX9213/MAX9215 deserializers) limits the imbalance of ones and zeros transmitted on each channel. If +1 is assigned to each binary 1 transmitted and -1 is assigned to each binary 0 transmitted, the variation in the running sum of assigned values is called the digital sum variation (DSV). The maximum DSV for the data channels is 10. At most, 10 more zeros

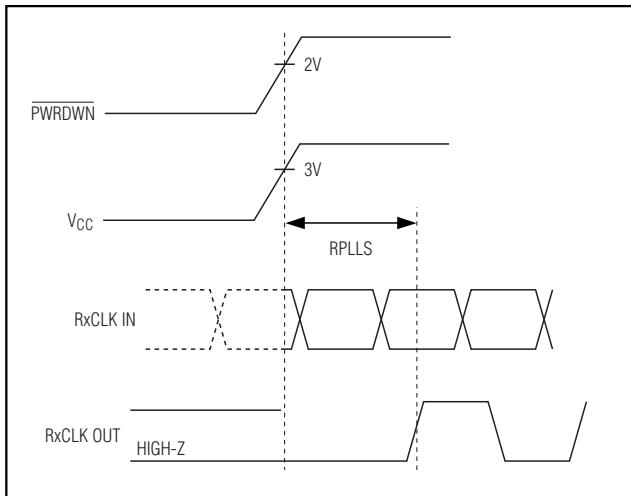


Figure 7. Phase-Locked Loop Set Time

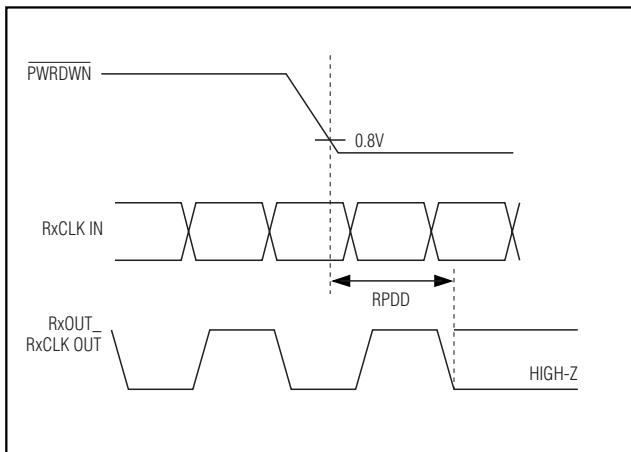


Figure 8. Power-Down Delay

than ones, or 10 more ones than zeros, are transmitted. The maximum DSV for the clock channel is five. Limiting the DSV and choosing the correct coupling capacitors maintains differential signal amplitude and reduces jitter due to droop on AC-coupled links.

To obtain DC balance on the data channels, the serializer parallel data is inverted or not inverted, depending on the sign of the digital sum at the word boundary. Two complementary bits are appended to each group of 7 parallel input data bits to indicate to the MAX9210/MAX9212/MAX9214/MAX9216 deserializers whether the data bits are inverted (see Figures 9 and 10). The deserializer restores the original state of the parallel data. The LVDS clock signal alternates duty cycles of 4/9 and 5/9, which maintain DC balance.

## Programmable DC-Balance 21-Bit Deserializers

### AC-Coupling Benefits

Bit errors experienced with DC-coupling can be eliminated by increasing the receiver common-mode voltage range by AC-coupling. AC-coupling increases the common-mode voltage range of an LVDS receiver to nearly the voltage rating of the capacitor. The typical LVDS driver output is 350mV centered on an offset voltage of 1.25V, making single-ended output voltages of 1.425V and 1.075V. An LVDS receiver accepts signals from 0V to 2.4V, allowing approximately  $\pm 1$ V common-mode difference between the driver and receiver on a DC-coupled link ( $2.4V - 1.425V = 0.975V$  and  $1.075V - 0V = 1.075V$ ). Common-mode voltage differences may be due to ground potential variation or common-mode

noise. If there is more than  $\pm 1$ V of difference, the receiver is not guaranteed to read the input signal correctly and may cause bit errors. AC-coupling filters low-frequency ground shifts and common-mode noise and passes high-frequency data. A common-mode voltage difference up to the voltage rating of the coupling capacitor (minus half the differential swing) is tolerated. DC-balanced coding of the data is required to maintain the differential signal amplitude and limit jitter on an AC-coupled link. A capacitor in series with each output of the LVDS driver is sufficient for AC-coupling. However, two capacitors—one at the serializer output and one at the deserializer input—provide protection in case either end of the cable is shorted to a high voltage.

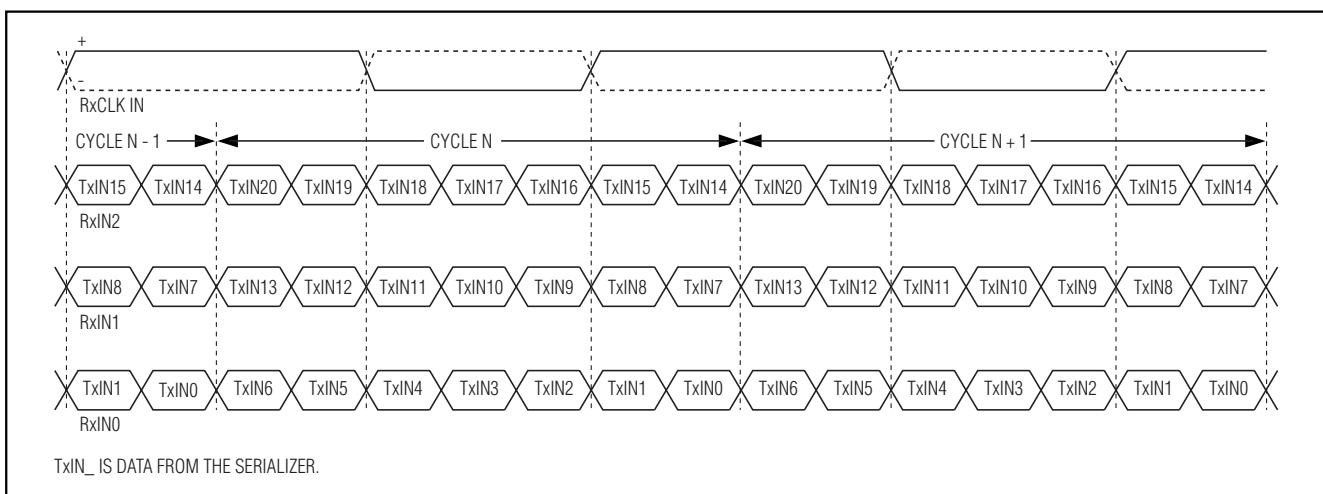


Figure 9. Deserializer Serial Input in Non-DC-Balanced Mode

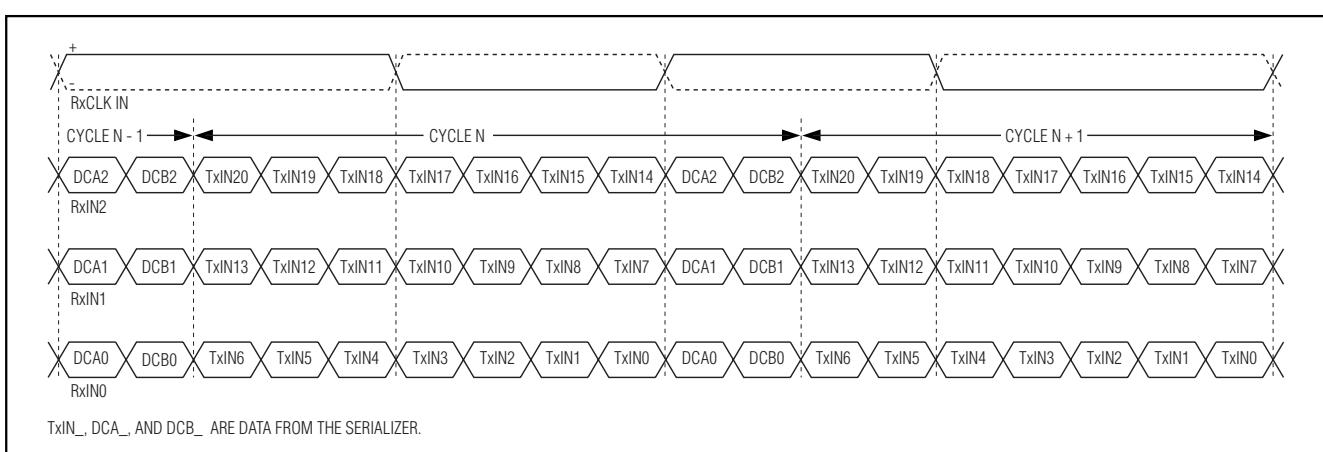


Figure 10. Deserializer Serial Input in DC-Balanced Mode

# Programmable DC-Balance 21-Bit Deserializers

## Applications Information

### Selection of AC-Coupling Capacitors

Voltage droop and the DSV of transmitted symbols causes signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level.

The RC network for an AC-coupled link consists of the LVDS receiver termination resistor ( $R_T$ ), the LVDS driver output resistor ( $R_O$ ), and the series AC-coupling capacitors (C). The RC time constant for two equal-value series capacitors is  $(C \times (R_T + R_O))/2$  (Figure 12). The RC time constant for four equal-value series capacitors is  $(C \times (R_T + R_O))/4$  (Figure 13).

$R_T$  is required to match the transmission line impedance (usually  $100\Omega$ ) and  $R_O$  is determined by the LVDS driver design (the minimum differential output resistance of  $78\Omega$  for the MAX9209/MAX9211/MAX9213/MAX9215 serializers is used in the following example). This leaves the capacitor selection to change the system time constant.

In the following example, the capacitor value for a droop of 2% is calculated. Jitter due to this droop is then calculated assuming a 1ns transition time:

$$C = -(2 \times t_B \times DSV) / (\ln(1 - D) \times (R_T + R_O)) \quad (\text{Eq 1})$$

where:

C = AC-coupling capacitor (F)

$t_B$  = bit time (s)

DSV = digital sum variation (integer)

$\ln$  = natural log

D = droop (% of signal amplitude)

$R_T$  = termination resistor ( $\Omega$ )

$R_O$  = output resistance ( $\Omega$ )

Equation 1 is for two series capacitors (Figure 12). The bit time ( $t_B$ ) is the period of the parallel clock divided by 9. The DSV is 10. See equation 3 for four series capacitors (Figure 13).

The capacitor for 2% maximum droop at 8MHz parallel rate clock is:

$$C = -(2 \times t_B \times DSV) / (\ln(1 - D) \times (R_T + R_O))$$

$$C = -(2 \times 13.9\text{ns} \times 10) / (\ln(1 - 0.02) \times (100\Omega + 78\Omega))$$

$$C = 0.0773\mu\text{F}$$

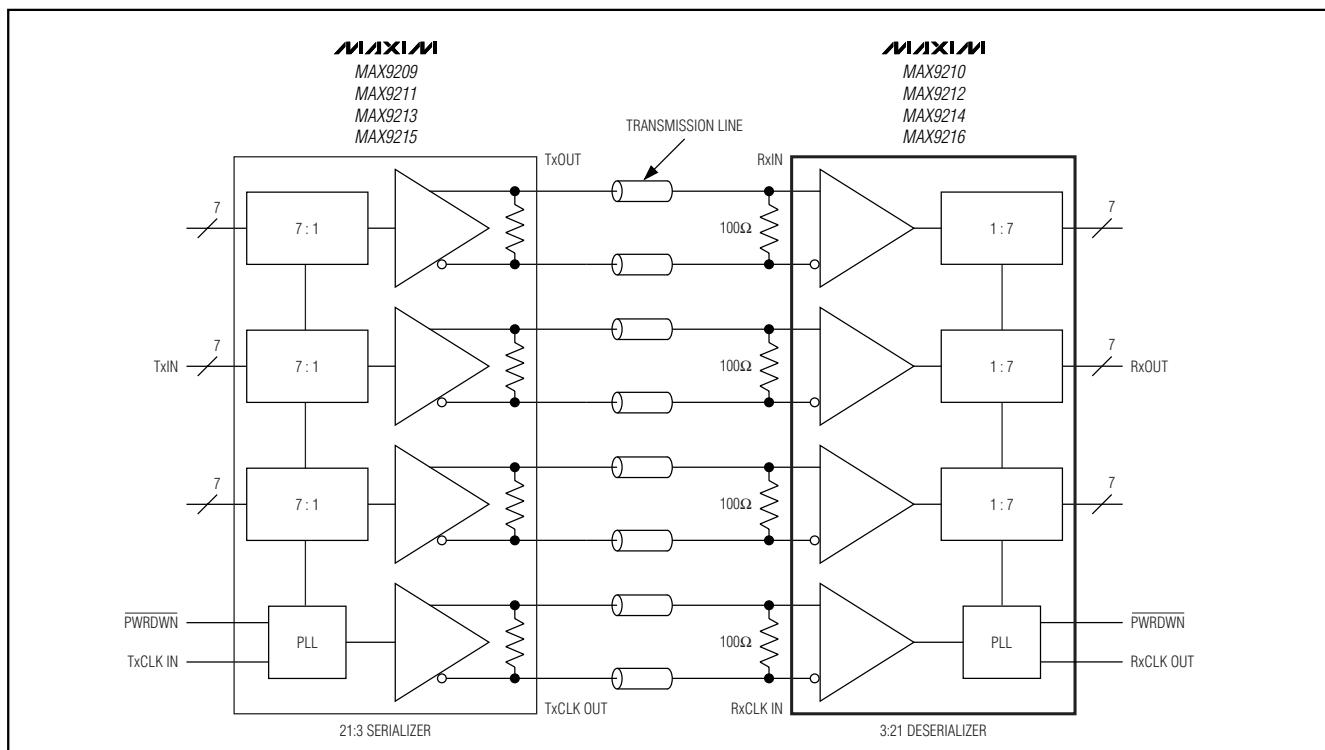


Figure 11. DC-Coupled Link, Non-DC-Balanced Mode

**MAX9210/MAX9212/MAX9214/MAX9216**

## Programmable DC-Balance 21-Bit Deserializers

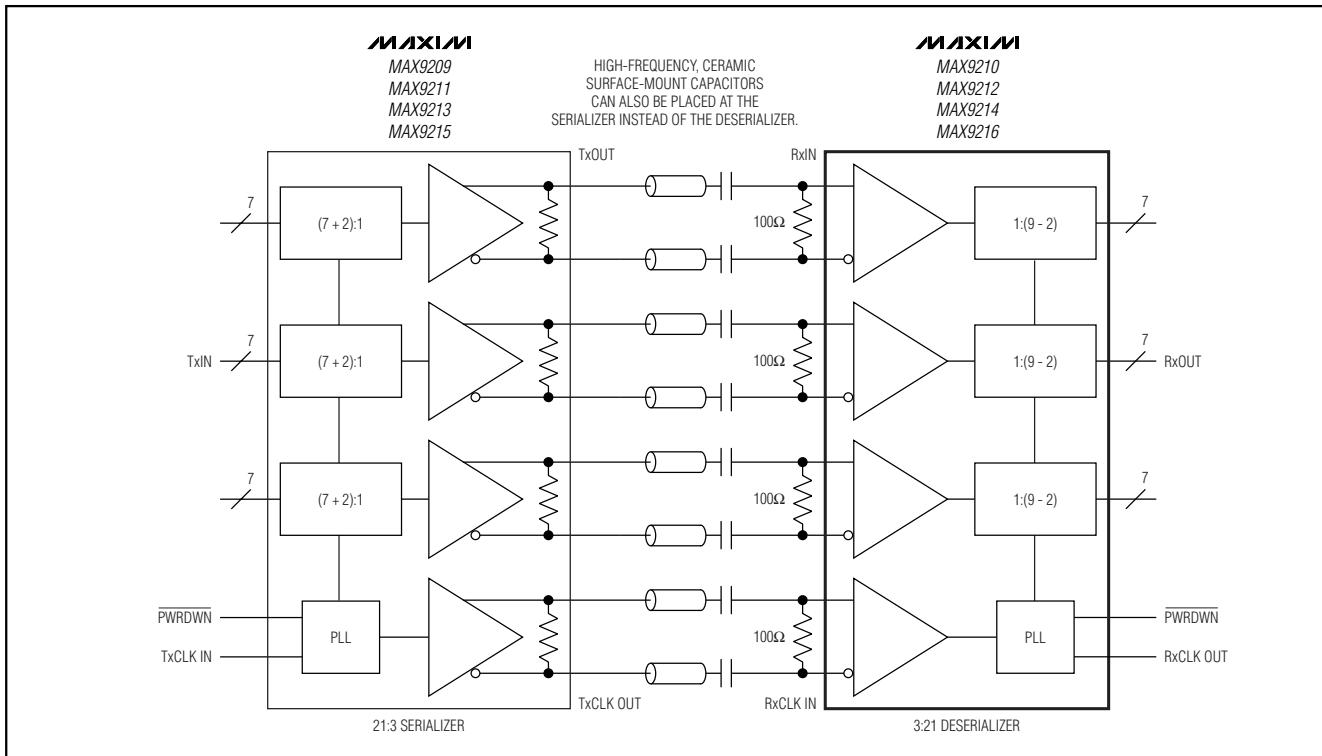


Figure 12. Two Capacitors per Link, AC-Coupled, DC-Balanced Mode

Jitter due to droop is proportional to the droop and transition time:

$$t_J = t_T \times D \quad (\text{Eq 2})$$

where:

$t_J$  = jitter (s)

$t_T$  = transition time (s) (0% to 100%)

D = droop (% of signal amplitude)

Jitter due to 2% droop and assumed 1ns transition time is:

$$t_J = 1\text{ns} \times 0.02$$

$$t_J = 20\text{ps}$$

The transition time in a real system depends on the frequency response of the cable driven by the serializer. The capacitor value decreases for a higher frequency parallel clock and for higher levels of droop and jitter. Use high-frequency, surface-mount ceramic capacitors.

Equation 1 altered for four series capacitors (Figure 13) is:

$$C = - (4 \times t_B \times DSV) / (\ln(1 - D) \times (R_T + R_O)) \quad (\text{Eq 3})$$

### Fail-Safe

The MAX9210/MAX9212/MAX9214/MAX9216 have fail-safe LVDS inputs in non-DC-balanced mode (Figure 1). Fail-safe drives the outputs low when the corresponding LVDS input is open, undriven and shorted, or undriven and parallel terminated. The fail-safe on the LVDS clock input drives all outputs low. Fail-safe does not operate in DC-balanced mode.

### Input Bias and Frequency Detection

In DC-balanced mode, the inverting and noninverting LVDS inputs are internally connected to +1.2V through  $42\text{k}\Omega$  (min) to provide biasing for AC-coupling (Figure 1). A frequency-detection circuit on the clock input detects when the input is not switching, or is switching at low frequency. In this case, all outputs are driven low. To prevent switching due to noise when the clock input is not driven, bias the clock input to differential +15mV by connecting a  $10\text{k}\Omega \pm 1\%$  pullup resistor between the noninverting input and  $V_{CC}$ , and a  $10\text{k}\Omega \pm 1\%$  pulldown resistor between the inverting input and ground. These bias resistors, along with the  $100\Omega \pm 1\%$  tolerance termination resistor, provide +15mV of differential input. However, the +15mV bias causes degradation of

# Programmable DC-Balance 21-Bit Deserializers

**MAX9210/MAX9212/MAX9214/MAX9216**

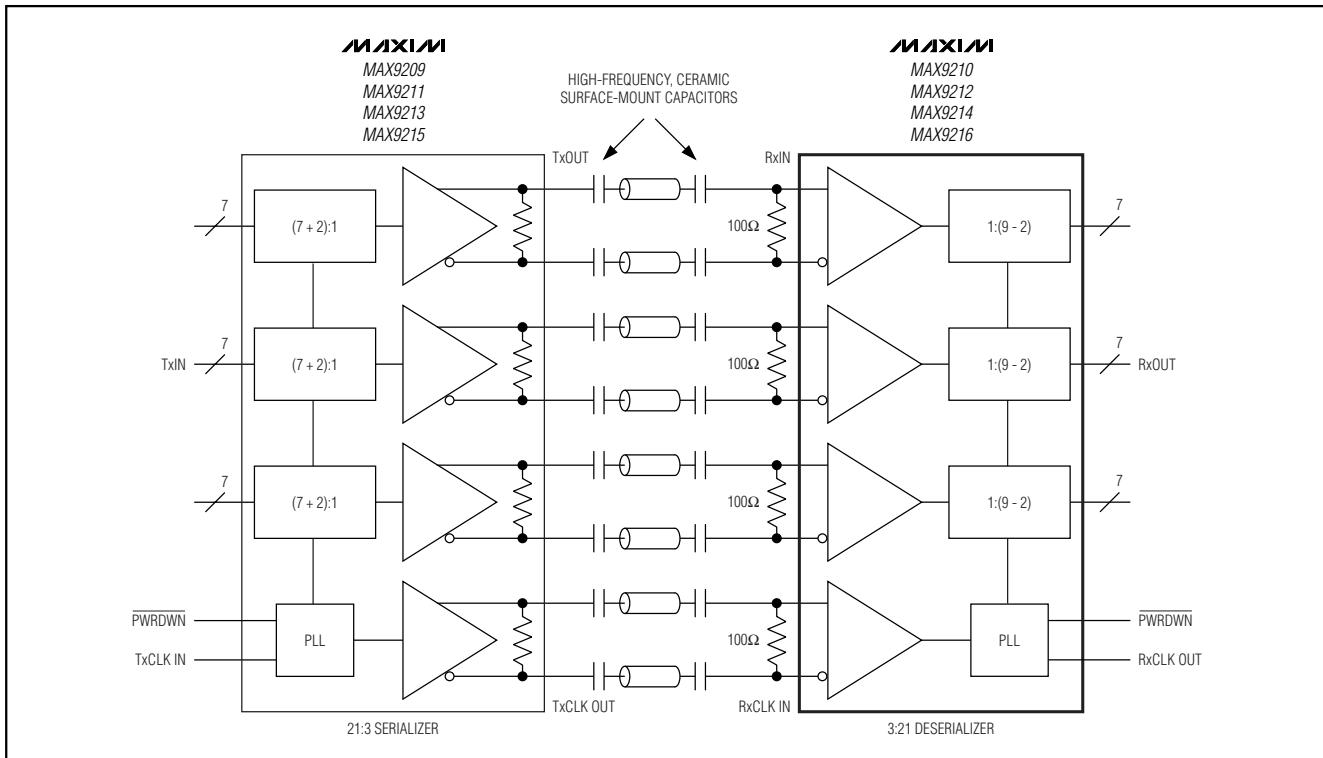


Figure 13. Four Capacitors per Link, AC-Coupled, DC-Balanced Mode

RSKM proportional to the slew rate of the clock input. For example, if the clock transitions 250mV in 500ps, the slew rate of 0.5mV/ps reduces RSKM by 30ps.

### Unused LVDS Data Inputs

In non-DC-balanced mode, leave unused LVDS data inputs open. In non-DC balanced mode, the input fail-safe circuit drives the corresponding outputs low and no pullup or pulldown resistors are needed. In DC-balanced mode, at each unused LVDS data input, pull the inverting input up to VCC using a  $10\text{k}\Omega$  resistor, and pull the noninverting input down to ground using a  $10\text{k}\Omega$  resistor. Do not connect a termination resistor. The pullup and pulldown resistors drive the corresponding outputs low and prevent switching due to noise.

### PWRDWN

Driving PWRDWN low puts the outputs in high impedance, stops the PLL, and reduces supply current to  $50\mu\text{A}$  or less. Driving PWRDWN high drives the outputs low until the PLL locks. The outputs of two deserializers can be bused to form a 2:1 mux with the outputs con-

trolled by PWRDWN. Wait 100ns between disabling one deserializer (driving PWRDWN low) and enabling the second one (driving PWRDWN high) to avoid contention of the bused outputs.

### Input Clock and PLL Lock Time

There is no required timing sequence for the application or reapplication of the parallel rate clock (RxCLK IN) relative to PWRDWN, or to a power-supply ramp for proper PLL lock. The PLL lock time is set by an internal counter. The maximum time to lock is 32,800 clock periods. Power and clock should be stable to meet the lock time specification. When the PLL is locking, the outputs are low.

### Power-Supply Bypassing

There are separate on-chip power domains for digital circuits, outputs, PLL, and LVDS inputs. Bypass each VCC, VCCO, PLL VCC, and LVDS VCC pin with high-frequency, surface-mount ceramic  $0.1\mu\text{F}$  and  $0.001\mu\text{F}$  capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.

# Programmable DC-Balance 21-Bit Deserializers

## Cables and Connectors

Interconnect for LVDS typically has a differential impedance of  $100\Omega$ . Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

## Board Layout

Keep the LVTT/LVCMOS outputs and LVDS input signals separated to prevent crosstalk. A four-layer PC board with separate layers for power, ground, LVDS inputs, and digital signals is recommended.

## IEC 61000-4-2 Level 4 ESD Protection

The IEC 61000-4-2 standard specifies ESD tolerance for electronic systems. The IEC 61000-4-2 model (Figure 14) specifies a 150pF capacitor that is discharged into the device through a  $330\Omega$  resistor. The MAX9210/MAX9212/MAX9214/MAX9216 LVDS inputs are rated for IEC 61000-4-2 level 4 ( $\pm 8kV$  contact discharge and  $\pm 15kV$  air discharge). IEC 61000-4-2 discharges higher peak current and more energy than the HBM due to the lower series resistance and larger capacitor. The HBM (Figure 15) specifies a 100pF capacitor that is discharged into the device through a  $1.5k\Omega$  resistor. All pins are rated for  $\pm 2kV$  HBM.

## 5V Tolerant Input

PWRDWN is 5V tolerant and is internally pulled down to GND. DCB/NC is not 5V tolerant. The input voltage range for DCB/NC is nominally ground to Vcc. Normally, DCB/NC is tied to Vcc or ground.

## Skew Margin (RSKM)

Skew margin (RSKM) is the time allowed for degradation of the serial data sampling setup and hold times by sources other than the deserializer. The deserializer sampling uncertainty is accounted for and does not need to be subtracted from RSKM. The main outside contributors of jitter and skew that subtract from RSKM are interconnect intersymbol interference, serializer pulse position uncertainty, and pair-to-pair path skew.

## V<sub>CCO</sub> Output Supply and Power Dissipation

The outputs have a separate supply (V<sub>CCO</sub>) for interfacing to systems with 1.8V to 5V nominal input logic levels. The *DC Electrical Characteristics* table gives the maximum supply current for V<sub>CCO</sub> = 3.6V with 8pF load at several switching frequencies with all outputs switching in the worst-case switching pattern. The approximate incremental supply current for V<sub>CCO</sub> other than 3.6V **with the same 8pF** load and worst-case pattern can be calculated using:

$$I_I = C_T V_I 0.5 F_C \times 21 \text{ (data outputs)} \\ + C_T V_I F_C \times 1 \text{ (clock output)} \dots$$

where:

I<sub>I</sub> = incremental supply current

C<sub>T</sub> = total internal (C<sub>INT</sub>) and external (C<sub>L</sub>) load capacitance

V<sub>I</sub> = incremental supply voltage

F<sub>C</sub> = output clock switching frequency

The incremental current is added to (for V<sub>CCO</sub> > 3.6V) or subtracted from (for V<sub>CCO</sub> < 3.6V) the *DC Electrical Characteristics* table maximum supply current. The internal output buffer capacitance is C<sub>INT</sub> = 6pF. The worst-case pattern switching frequency of the data outputs is half the switching frequency of the output clock.

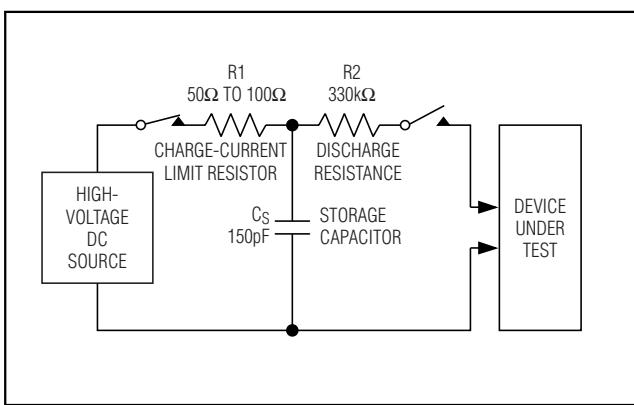


Figure 14. IEC 61000-4-2 Contact Discharge ESD Test Circuit

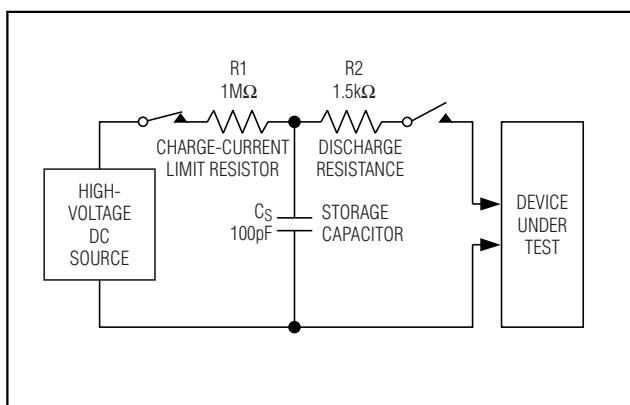


Figure 15. Human Body ESD Test Circuit

## Programmable DC-Balance 21-Bit Deserializers

In the following example, the incremental supply current is calculated for  $V_{CCO} = 5.5V$ ,  $F_C = 34MHz$ , and  $C_L = 8pF$ :

$$V_I = 5.5V - 3.6V = 1.9V$$

$$C_T = C_{INT} + C_L = 6pF + 8pF = 14pF$$

where:

$$I_I = C_T V_I 0.5 F_C \times 21 \text{ (data outputs)} + C_T V_I F \times 1 \text{ (clock output)}$$

$$I_I = (14pF \times 1.9V \times 0.5 \times 34MHz \times 21) + (14pF \times 1.9V \times 34MHz)$$

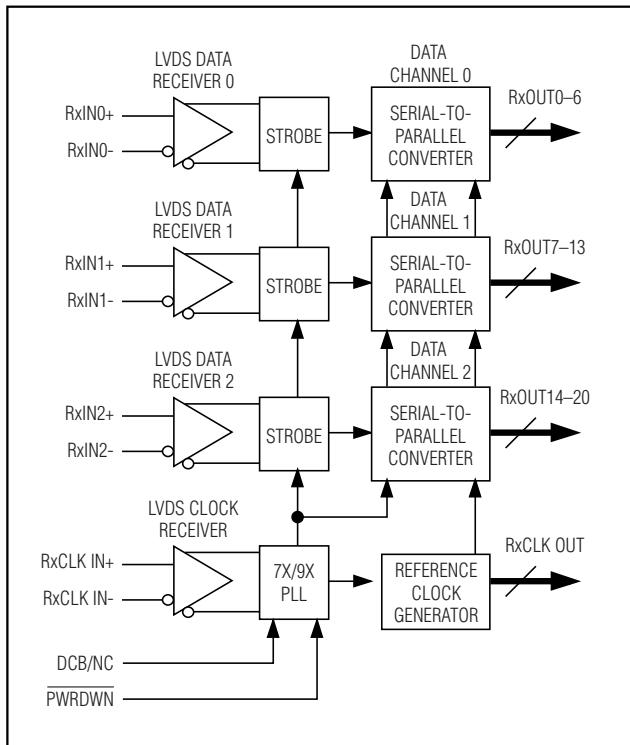
$$I_I = 9.5mA + 0.9mA = 10.4mA$$

The maximum supply current in DC-balanced mode for  $V_{CC} = V_{CCO} = 3.6V$  at  $F = 34MHz$  is 106mA (from the *DC Electrical Characteristics* table). Add 10.4mA to get the total approximate maximum supply current at  $V_{CCO} = 5.5V$  and  $V_{CC} = 3.6V$ .

If the output supply voltage is less than  $V_{CCO} = 3.6V$ , the reduced supply current can be calculated using the same formula and method.

At high switching frequency, high supply voltage, and high capacitive loading, power dissipation can exceed the package power dissipation rating. Do not exceed the maximum package power dissipation rating. See the *Absolute Maximum Ratings* for maximum package power dissipation capacity and temperature derating.

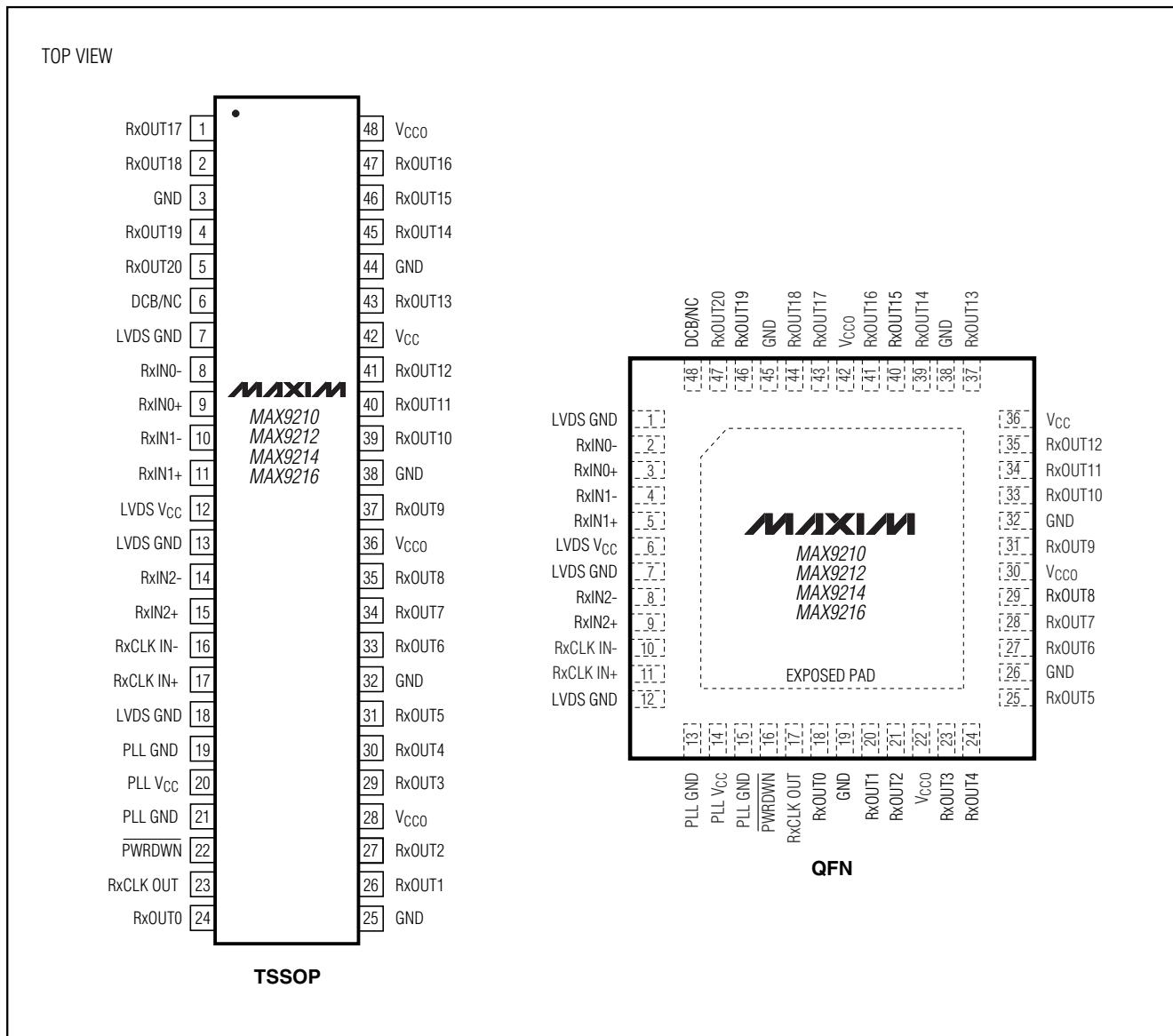
### Functional Diagram



**MAX9210/MAX9212/MAX9214/MAX9216**

# Programmable DC-Balance 21-Bit Deserializers

## Pin Configurations



## Chip Information

MAX9210 TRANSISTOR COUNT: 10,248  
MAX9212 TRANSISTOR COUNT: 10,248  
MAX9214 TRANSISTOR COUNT: 10,248  
MAX9216 TRANSISTOR COUNT: 10,248  
PROCESS: CMOS

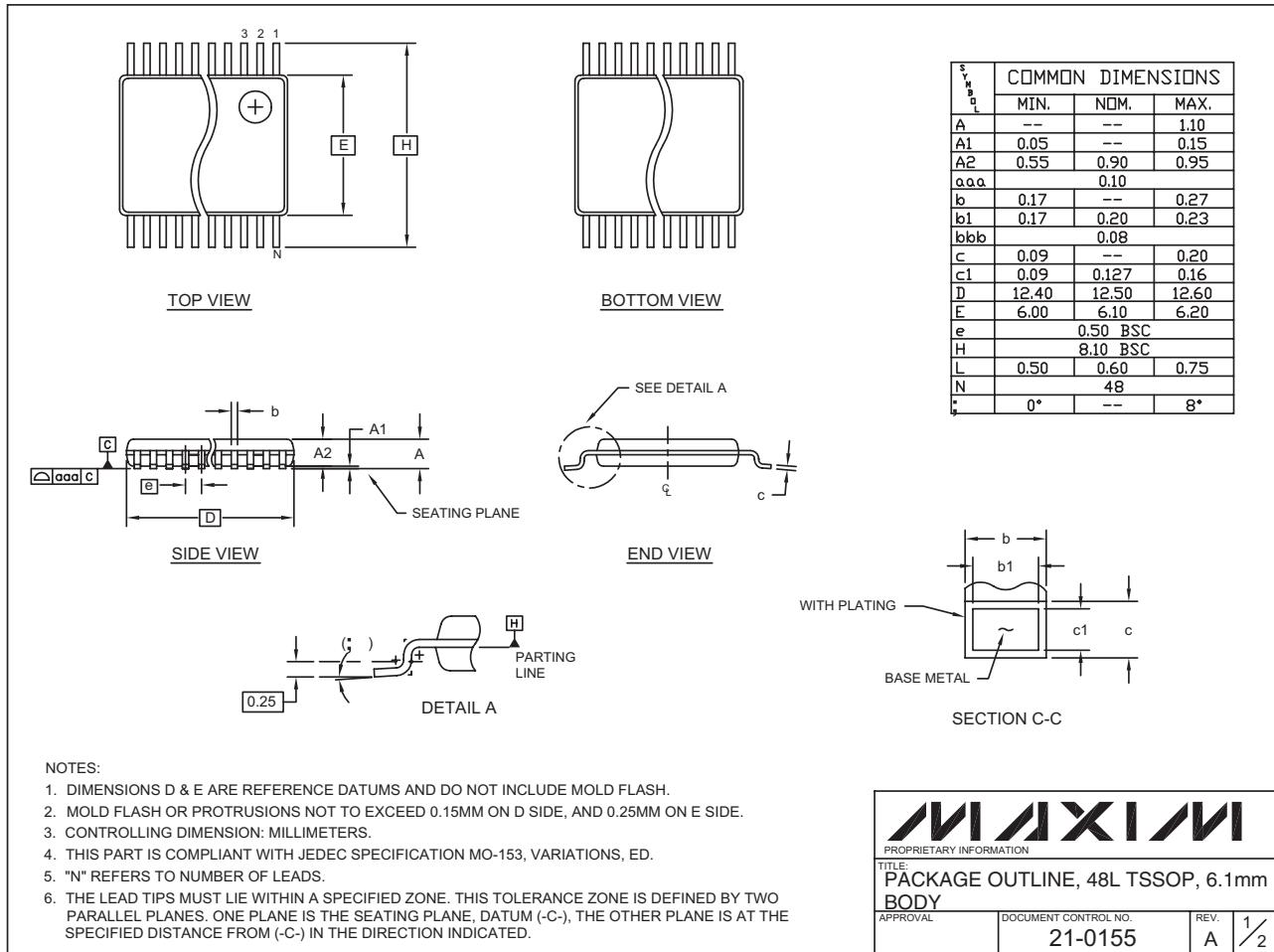
# Programmable DC-Balance 21-Bit Deserializers

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

48L TSSOP.EPS

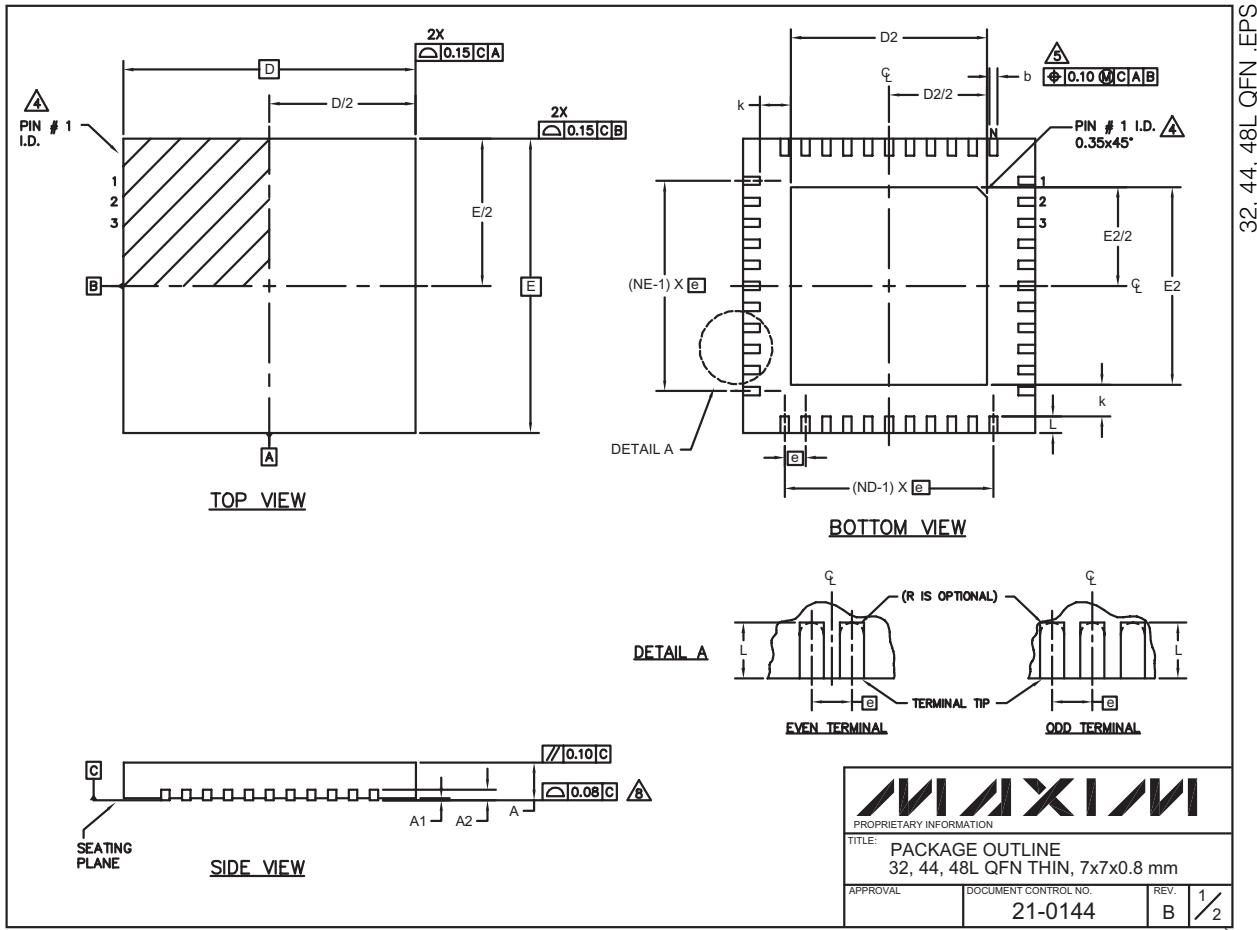
MAX9210/MAX9212/MAX9214/MAX9216



# Programmable DC-Balance 21-Bit Deserializers

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).



# Programmable DC-Balance 21-Bit Deserializers

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

COMMON DIMENSIONS												EXPOSED PAD VARIATIONS							
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1)			D2	E2	JEDEC MO220 REV. C				
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	4.55	4.70	4.85	4.55	4.70	4.85	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	4.55	4.70	4.85	4.55	4.70	4.85	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			WKKD-1		WKKD-2				
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	4.20	4.30	4.40	4.20	4.30	4.40	
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	-		-				
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	-		-				
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			-		-				
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	-		-				
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	-		-				
N	32			44			48			44			-		-				
ND	8			11			12			10			-		-				
NE	8			11			12			12			-		-				

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.



PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE  
32, 44, 48L QFN THIN, 7x7x0.8 mm

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	21-0144	B / 2

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