19-2808; Rev 0; 4/03

MAXIM

Single LVDS/Anything-to-LVPECL Translator

MAX9375

General Description

The MAX9375 is a fully differential, high-speed, anything-to-LVPECL translator designed for signal rates up to 2GHz. The MAX9375's extremely low propagation delay and high speed make it ideal for various high-speed network routing and backplane applications.

The MAX9375 accepts any differential input signal within the supply rails and with minimum amplitude of 100mV. Inputs are fully compatible with the LVDS, LVPECL, HSTL, and CML differential signaling standards. Outputs are LVPECL and have sufficient current to drive 50Ω transmission lines.

The MAX9375 is available in an 8-pin μMAX package and operates from a single +3.3V supply over the -40°C to +85°C temperature range.

Features

- ♦ **Guaranteed 2GHz Switching Frequency**
- ♦ **Accepts LVDS/LVPECL/Anything Inputs**
- ♦ **421ps (typ) Propagation Delays**
- ♦ **30ps (max) Pulse Skew**
- ♦ **2ps$_{RMS}$ (max) Random Jitter**
- ♦ **Minimum 100mV Differential Input to Guarantee AC Specifications**
- ♦ **Temperature-Compensated LVPECL Output**
- ♦ **+3.0V to +3.6V Power-Supply Operating Range**
- ♦ **>2kV ESD Protection (Human Body Model)**

Applications

Backplane Logic Standard Translation

LAN

WAN

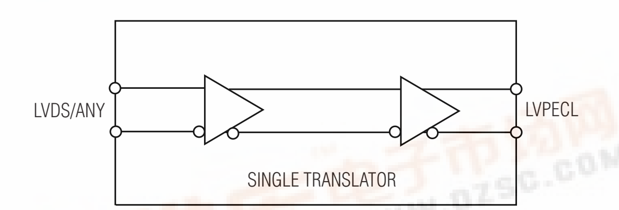
DSLAM

DLC

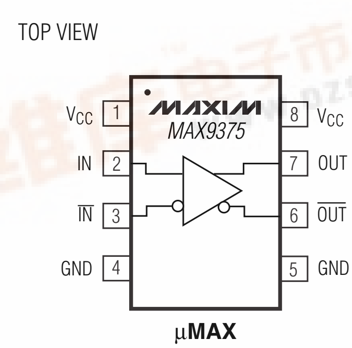
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9375EUA	-40°C to +85°C	8 μMAX

Functional Diagram



Pin Configuration



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +4.1V
Inputs (IN, $\overline{IN}$) ....-0.3V to (V_{CC} + 0.3V)
IN to $\overline{IN}$ ....±3.0V
Continuous Output Current 50mA
Surge Output Current 100mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX (derate 5.9mW/°C above +70°C) 470.6mW
θ_{JA} in Still Air ....+170°C/W

Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
ESD Protection
Human Body Model (IN, $\overline{IN}$, OUT, $\overline{OUT}$) ....≥ 2kV
Soldering Temperature (10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 3.0V, input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage V_{CM} = 0.05V to (V_{CC} - 0.05V), LVPECL outputs terminated with 50Ω ±1% to V_{CC} - 2.0V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL INPUTS (IN, $\overline{IN}$)												
Differential Input Threshold	V_{THD}		-100		+100	-100		+100	-100		+100	mV
Input Current	I_{IN}, $I_{\overline{IN}}$	V_{IN}, $V_{\overline{IN}}$ = V_{CC} or 0V	-20		+20	-20		+20	-20		+20	µA
Input Common-Mode Voltage	V_{CM}	Figure 1	0.05		V_{CC} - 0.05	0.05		V_{CC} - 0.05	0.05		V_{CC} - 0.05	V
LVPECL OUTPUTS (OUT, $\overline{OUT}$)												
Single-Ended Output High Voltage	V_{OH}		V_{CC} - 1.085	V_{CC} - 1.017	V_{CC} - 0.880	V_{CC} - 1.025	V_{CC} - 0.983	V_{CC} - 0.880	V_{CC} - 1.025	V_{CC} - 0.966	V_{CC} - 0.880	V
Single-Ended Output Low Voltage	V_{OL}		V_{CC} - 1.830	V_{CC} - 1.753	V_{CC} - 1.620	V_{CC} - 1.810	V_{CC} - 1.710	V_{CC} - 1.620	V_{CC} - 1.810	V_{CC} - 1.692	V_{CC} - 1.620	V
Differential Output Voltage	V_{OH} - V_{OL}		595	725		595	725		595	725		mV
POWER SUPPLY												
Supply Current	I_{CC}	All pins open except V_{CC}, GND		10	18		12	18		14	18	mA

AC ELECTRICAL CHARACTERISTICS

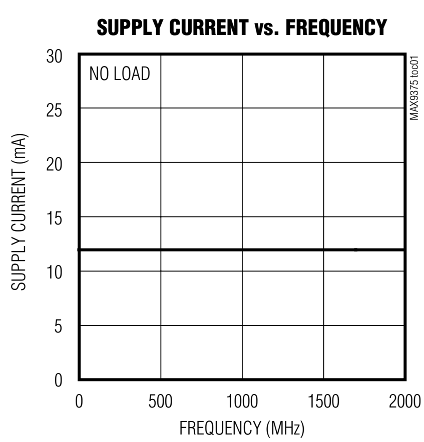
(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input frequency ≤ 1.34GHz, differential input transition time = 125ps (20% to 80%), input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage V_{CM} = 0.05V to (V_{CC} - 0.05V), outputs terminated with 50Ω ±1% to V_{CC} - 2.0V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Note 4)

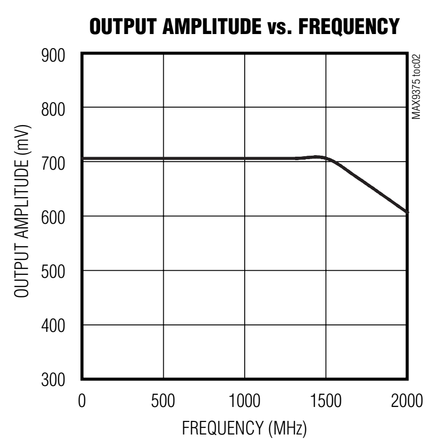
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 250mV	2.0	2.5		GHz
Propagation Delay Low to High	t_{PLH}	Figure 2	250	421	600	ps
Propagation Delay High to Low	t_{PHL}	Figure 2	250	421	600	ps
Pulse Skew $\|t_{PLH}$ -$t_{PHL}\|$	t_{SKEW}	Figure 2 (Note 5)		6	30	ps
Output Low-to-High Transition Time (20% to 80%)	t_R	Figure 2		116	220	ps
Output High-to-Low Transition Time (20% to 80%)	t_F	Figure 2		116	220	ps
Added Random Jitter	t_{RJ}	f_{IN} = 1.34GHz (Note 6)		0.7	2	$ps_{(RMS)}$

Note 1: Measurements are made with the device in thermal equilibrium. All voltages are referenced to ground except V_{THD} and V_{ID}.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters production tested at T_A = +25°C and guaranteed by design and characterization over the full operating temperature range.
Note 4: Guaranteed by design and characterization, not production tested. Limits are set at ±6 sigma.
Note 5: t_{SKEW} is the magnitude difference of differential propagation delays for the same output under the same conditions; t_{SKEW} = $|t_{PHL}$ - $t_{PLH}|$.
Note 6: Device jitter added to the input signal.

Typical Operating Characteristics

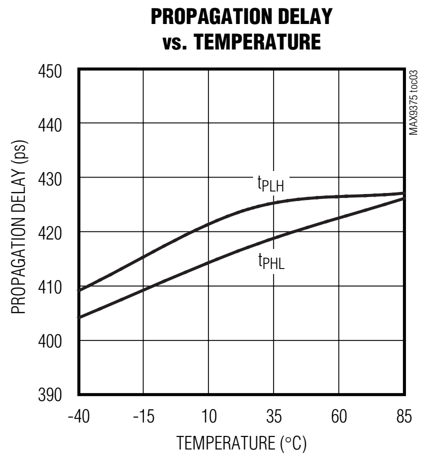
(V_{CC} = +3.3V, differential input voltage $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, input frequency = 500MHz, outputs terminated with 50Ω ±1% to V_{CC} - 2.0V, T_A = +25°C, unless otherwise noted.)

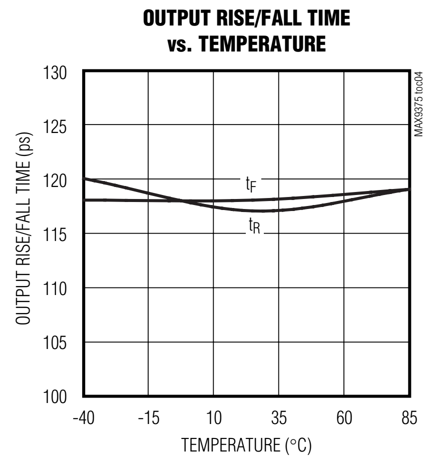




Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, differential input voltage $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, input frequency = 500MHz, outputs terminated with 50Ω ±1% to V_{CC} - 2.0V, T_A = +25°C, unless otherwise noted.)





Detailed Description

The MAX9375 is a fully differential, high-speed, anything-to-LVPECL translator designed for signal rates up to 2GHz. The MAX9375's extremely low propagation delay and high speed make it ideal for various high-speed network routing and backplane applications.

The MAX9375 accepts any differential input signals within the supply rails and with a minimum amplitude of 100mV. Inputs are fully compatible with the LVDS, LVPECL, HSTL, and CML differential signaling standards. Outputs are LVPECL and have sufficient current to drive 50Ω transmission lines.

Inputs

Inputs have a wide common-mode range of 0.05V to (V_{CC} - 0.05V), which accommodates any differential signals within rails, and requires a minimum of 100mV to switch the outputs. This allows the MAX9375 inputs to support virtually any differential signaling standard.

LVPECL Outputs

The MAX9375 outputs are emitter followers that require external resistive paths to a voltage source (V_T = V_{CC} - 2.0V typ) more negative than worst-case V_{OL} for proper static and dynamic operation. When properly terminated, the outputs generate steady-state voltage levels, V_{OL} or V_{OH} with fast transition edges between state levels. Output current always flows into the termination during proper operation.

Pin Description

PIN	NAME	FUNCTION
1, 8	V_{CC}	Positive Supply. Bypass from V_{CC} to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	IN	LVDS/Anything Noninverting Input
3	$\overline{\text{IN}}$	LVDS/Anything Inverting Input
4, 5	GND	Power Supply Ground Connection
6	$\overline{\text{OUT}}$	Differential LVPECL Inverting Output. Terminate with 50Ω ±1% to V_{CC} - 2V.
7	OUT	Differential LVPECL Noninverting Output. Terminate with 50Ω ±1% to V_{CC} - 2V.

Applications Information

Output Termination

Terminate the outputs with 50Ω to (V_{CC} - 2V) or use equivalent Thevenin terminations. Terminate OUT and $\overline{OUT}$ with identical termination on each for low-output distortion. When a single-ended signal is taken from the differential output, terminate both OUT and $\overline{OUT}$. Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings*. Under all operating conditions, the device's total thermal limits should be observed.

Supply Bypassing

Bypass V_{CC} to ground with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors. Place the capacitors as close to the device as possible with the 0.01µF capacitor closest to the device pins.

Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

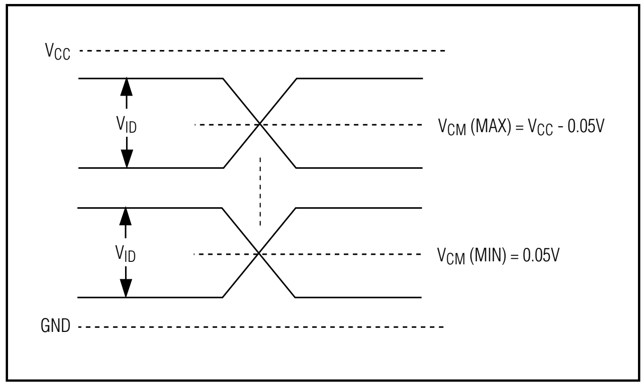


Figure 1. Input Definitions

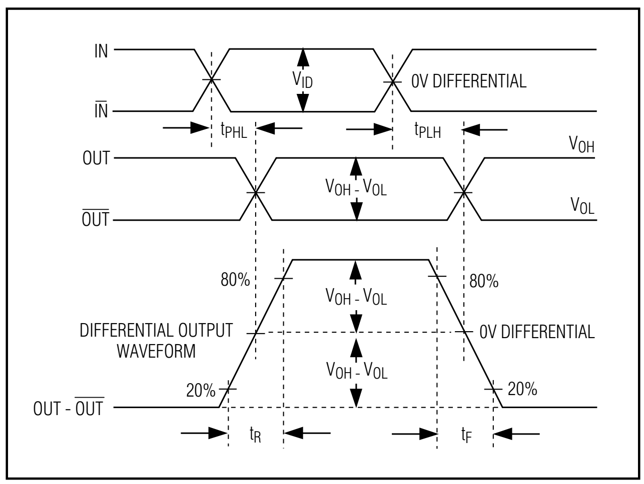


Figure 2. Differential Input-to-Output Propagation Delay Timing Diagram

Chip Information

TRANSISTOR COUNT: 614

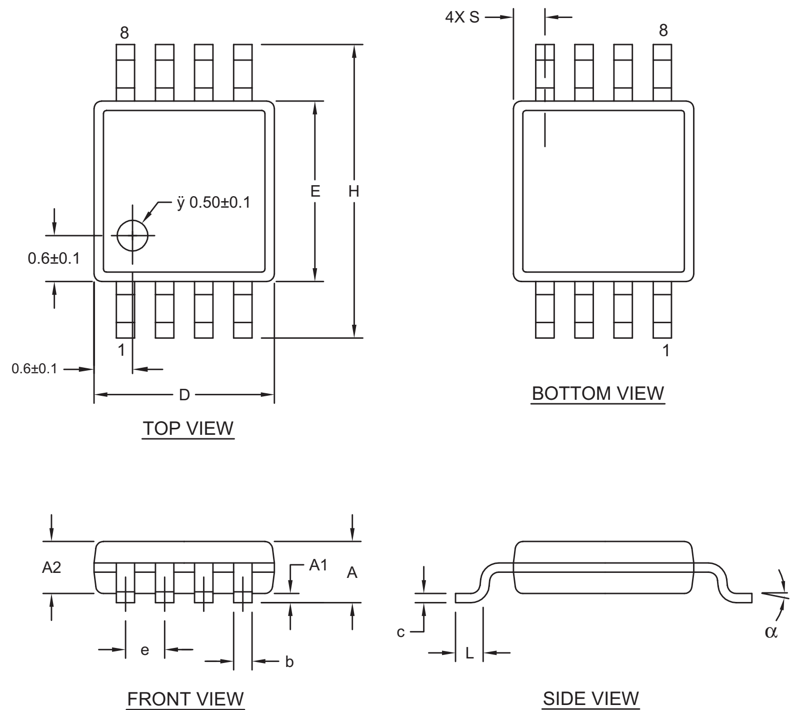
PROCESS: Bipolar

Single LVDS/Anything-to-LVPECL Translator

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8LUMAXD.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0∞	6∞	0∞	6∞
S	0.0207 BSC		0.5250 BSC	

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1