

1:2 Differential PECL/ECL/LVPECL/LVECL Clock and Data Driver

General Description

The MAX9320B low-skew, 1-to-2 differential driver is designed for clock and data distribution. The input is reproduced at two differential outputs. The differential input can be adapted to accept single-ended inputs by applying an external reference voltage.

The MAX9320B features ultra-low propagation delay (208ps), part-to-part skew (20ps), and output-to-output skew (6ps) with 30mA maximum supply current, making this device ideal for clock distribution. For interfacing to differential PECL and LVPECL signals, this device operates over a +3.0V to +5.5V supply range, allowing high-performance clock or data distribution in systems with a nominal 3.3V or 5V supply. For differential ECL and LVECL operation, this device operates from a -3.0V to -5.5V supply.

The MAX9320B is offered in industry-standard 8-pin TSSOP and SO packages.

Applications

- Precision Clock Distribution
- Low-Jitter Data Repeater
- Protection Switching

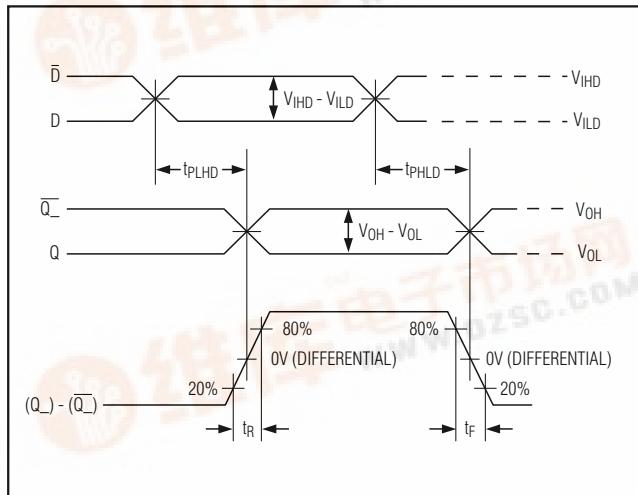


Figure 1. Differential Transition Time and Propagation Delay Timing Diagram

MAXIM

1:2 Differential PECL/ECL/LVPECL/LVECL Clock and Data Driver

Features

- ♦ Improved Second Source of the MC10EP11D
- ♦ +3.0V to +5.5V Differential PECL/LVPECL Operation
- ♦ -3.0V to -5.5V ECL/LVECL Operation
- ♦ Low 22mA Supply Current
- ♦ 20ps Part-to-Part Skew
- ♦ 6ps Output-to-Output Skew
- ♦ 208ps Propagation Delay
- ♦ Minimum 300mV Output at 3GHz
- ♦ Outputs Low for Open Input
- ♦ ESD Protection >2kV (Human Body Model)

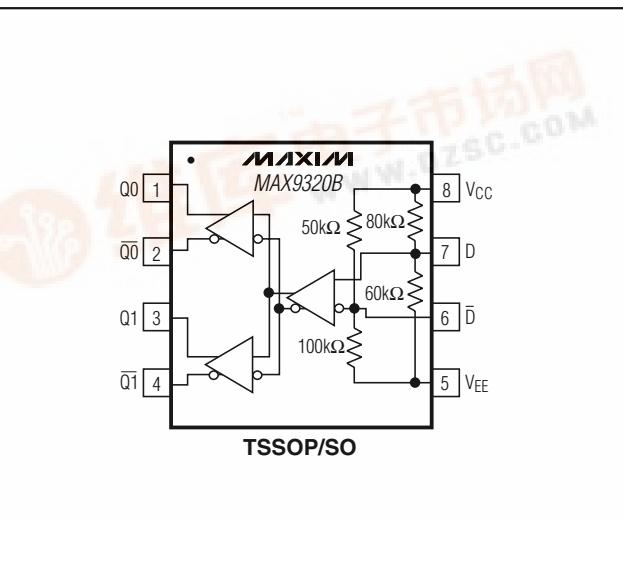
MAX9320B

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9320BESA	-40°C to +85°C	8 SO
MAX9320BEUA*	-40°C to +85°C	8 TSSOP

*Future product—contact factory for availability.

Pin Configuration



1:2 Differential PECL/ECL/LVPECL/LVECL Clock and Data Driver

ABSOLUTE MAXIMUM RATINGS

V _{CC} to V _{EE}	+6V
D or \bar{D}	V _{EE} - 0.3V to V _{CC} + 0.3V
D or \bar{D} with the Other Floating	V _{CC} - 5.0V to V _{CC} + 0.3V
D to \bar{D}	$\pm 3.0V$
Continuous Output Current	50mA
Surge Output Current	100mA
Continuous Output Power Dissipation (T _A = +70°C)	
8-Pin TSSOP (derate 4.5mW/°C above +70°C)	362mW
8-Pin SO (derate 5.9mW/°C above +70°C)	471mW
Junction-to-Ambient Thermal Resistance in Still Air	
8-Pin TSSOP	+221°C/W
8-Pin SO	+170°C/W

Junction-to-Ambient Thermal Resistance with 500	
LFPM Airflow	
8-Pin TSSOP	+155°C/W
8-Pin SO	+99°C/W
Junction-to-Case Thermal Resistance	
8-Pin TSSOP	+39°C/W
8-Pin SO	+40°C/W
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
ESD Protection	
Human Body Model (D, \bar{D} , Q ₊ , \bar{Q} ₊)	>2kV
Soldering Temperature (10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 3.0V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V. Typical values are at V_{CC} - V_{EE} = 5.0V, V_{IHD} = V_{CC} - 1.0V, V_{I LD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL INPUT (D, \bar{D})												
High Voltage of Differential Input	V _{IHD}		V _{EE} + 1.2	V _{CC}	V _{EE} + 1.2	V _{CC}	V _{EE} + 1.2	V _{CC}	V			
Low Voltage of Differential Input	V _{I LD}		V _{EE}	V _{CC} - 0.1	V _{EE}	V _{CC} - 0.1	V _{EE}	V _{CC} - 0.1	V			
Differential Input Voltage	V _{IHD} - V _{I LD}		0.1	3.0	0.1	3.0	0.1	3.0	V			
Input High Current	I _{IH}			150		150		150	μA			
D Input Low Current	I _{ILD}	V _{CC} - V _{EE} ≤ 3.8V	-100	+100	-100	+100	-100	+100	μA			
		V _{CC} - V _{EE} ≥ 3.8V	-140	+140	-140	+140	-140	+140				
\bar{D} Input Low Current	I _{ILD}	V _{CC} - V _{EE} ≤ 3.8V	-150	+150	-150	+150	-150	+150	μA			
		V _{CC} - V _{EE} ≥ 3.8V	-175	+175	-175	+175	-175	+175				
DIFFERENTIAL OUTPUTS (Q₊, \bar{Q}₊)												
Single-Ended Output High Voltage	V _{OH}	Figure 1	V _{CC} - 1.135	V _{CC} - 0.885	V _{CC} - 1.07	V _{CC} - 0.82	V _{CC} - 1.01	V _{CC} - 0.76	V			

1:2 Differential PECL/ECL/LVPECL/LVECL Clock and Data Driver

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - V_{EE} = 3.0V$ to $5.5V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$. Typical values are at $V_{CC} - V_{EE} = 5.0V$, $V_{IHD} = V_{CC} - 1.0V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Single-Ended Output Low Voltage	V_{OL}	Figure 1	$V_{CC} - 1.935$	$V_{CC} - 1.685$	$V_{CC} - 1.87$	$V_{CC} - 1.62$	$V_{CC} - 1.81$	$V_{CC} - 1.56$	V	V	V	
Differential Output Voltage	$V_{OH} - V_{OL}$	Figure 1	550	550	550	550	550	550	550	550	550	mV
POWER SUPPLY												
Supply Current	I_{EE}	(Note 4)	20	28	20	22	28	20	23	30	20	mA

AC ELECTRICAL CHARACTERISTICS

($V_{CC} - V_{EE} = 3.0V$ to $5.5V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$, input frequency $\leq 1.5GHz$, input transition time = 125ps (20% to 80%), $V_{IHD} = V_{EE} + 1.2V$ to V_{CC} , $V_{ILD} = V_{EE}$ to $V_{CC} - 0.15V$, $V_{IHD} - V_{ILD} = 0.15V$ to $3.0V$. Typical values are at $V_{CC} - V_{EE} = 5.0V$, $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD} , t_{PHLD}	Figure 1	145	220	265	155	208	265	160	203	270	ps
Output-to-Output Skew	t_{SKOO}	(Note 6)	6	30	6	30	6	30	6	30	6	ps
Part-to-Part Skew	t_{SKPP}	(Note 7)	20	120	20	110	20	110	20	110	20	ps
Added Random Jitter	t_{RJ}	$f_{IN} = 1.5GHz$, clock pattern (Note 8)	1.7	2.8	1.7	2.8	1.7	2.8	1.7	2.8	1.7	ps (RMS)
		$f_{IN} = 3.0GHz$, clock pattern (Note 8)	0.6	1.5	0.6	1.5	0.6	1.5	0.6	1.5	0.6	
Added Deterministic Jitter	t_{DJ}	3.0Gbps $2^{23} - 1$ PRBS pattern (Note 8)	57	80	57	80	57	80	57	80	57	ps (P-P)

1:2 Differential PECL/ECL/LVPECL/LVECL Clock and Data Driver

AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} - V_{EE} = 3.0V$ to $5.5V$, outputs loaded with $50\Omega \pm 1\%$ to $V_{CC} - 2V$, input frequency $\leq 1.5\text{GHz}$, input transition time = 125ps (20% to 80%), $V_{IHD} = V_{EE} + 1.2V$ to V_{CC} , $V_{ILD} = V_{EE}$ to $V_{CC} - 0.15V$, $V_{IHD} - V_{ILD} = 0.15V$ to $3.0V$. Typical values are at $V_{CC} - V_{EE} = 5.0V$, $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Switching Frequency	f _{MAX}	V _{OH} - V _{OL} $\geq 300\text{mV}$, clock pattern, Figure 1	3.0			3.0			3.0			GHz
		V _{OH} - V _{OL} $\geq 550\text{mV}$, clock pattern, Figure 1		2.0			2.0			2.0		
Output Rise/Fall Time (20% to 80%)	t _R , t _F	Figure 1	50	95	120	50	98	120	50	105	120	ps

Note 1: Measurements are made with the device in thermal equilibrium.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 3: DC parameters production tested at $T_A = +25^\circ\text{C}$. Guaranteed by design and characterization over the full operating temperature range.

Note 4: All pins open except V_{CC} and V_{EE}.

Note 5: Guaranteed by design and characterization. Limits are set at ± 6 sigma.

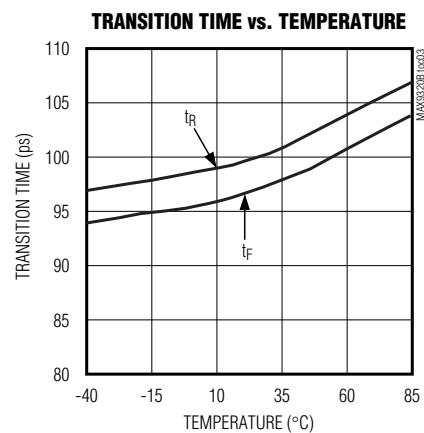
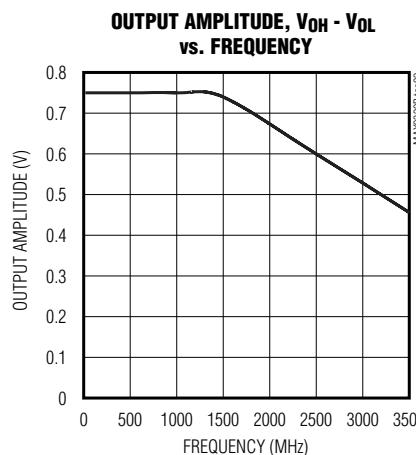
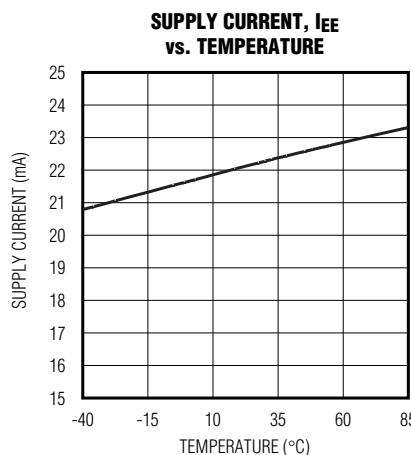
Note 6: Measured between outputs of the same part at the signal crossing points for a same-edge transition.

Note 7: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.

Note 8: Device jitter added to the input signal.

Typical Operating Characteristics

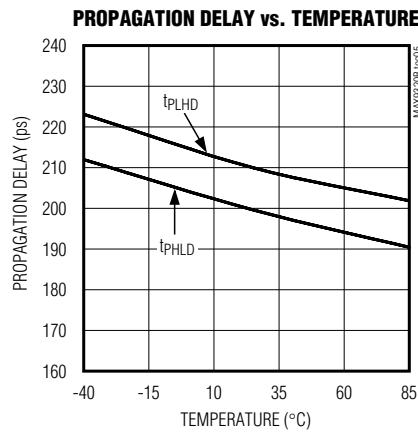
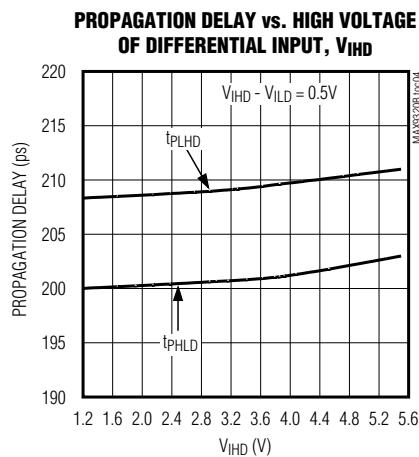
($V_{CC} = 5V$, $V_{EE} = 0$, input transition time = 125ps (20% to 80%), $V_{IHD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$, $f_{IN} = 1.5\text{GHz}$, outputs loaded with 50Ω to $V_{CC} - 2V$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



1:2 Differential PECL/ECL/LVPECL/LVECL Clock and Data Driver

Typical Operating Characteristics (continued)

($V_{CC} = 5V$, $V_{EE} = 0$, input transition time = 125ps (20% to 80%), $V_{IHLD} = V_{CC} - 1V$, $V_{ILD} = V_{CC} - 1.5V$, $f_{IN} = 1.5\text{GHz}$, outputs loaded with 50Ω to $V_{CC} - 2V$, $TA = +25^\circ\text{C}$, unless otherwise noted.)



MAX9320B

Pin Description

PIN	NAME	FUNCTION
1	Q_0	Noninverting Q_0 Output. Typically terminate with 50Ω resistor to $V_{CC} - 2V$.
2	$\overline{Q_0}$	Inverting Q_0 Output. Typically terminate with 50Ω resistor to $V_{CC} - 2V$.
3	Q_1	Noninverting Q_1 Output. Typically terminate with 50Ω resistor to $V_{CC} - 2V$.
4	$\overline{Q_1}$	Inverting Q_1 Output. Typically terminate with 50Ω resistor to $V_{CC} - 2V$.
5	V_{EE}	Negative Supply Voltage
6	\overline{D}	Inverting Differential Input. $50\text{k}\Omega$ pullup to V_{CC} and $100\text{k}\Omega$ pulldown to V_{EE} .
7	D	Noninverting Differential Input. $80\text{k}\Omega$ pullup to V_{CC} and $60\text{k}\Omega$ pulldown to V_{EE} .
8	V_{CC}	Positive Supply Voltage. Bypass from V_{CC} to V_{EE} with $0.1\mu\text{F}$ and $0.01\mu\text{F}$ ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

1:2 Differential PECL/ECL/LVPECL/LVECL Clock and Data Driver

Detailed Description

The MAX9320B low-skew, 1-to-2 differential driver is designed for clock and data distribution. For interfacing to differential PECL and LVPECL signals, this device operates over a +3.0V to +5.5V supply range, allowing high-performance clock and data distribution in systems with a nominal 3.3V or 5V supply. For differential ECL and LVECL operation, this device operates from a -3.0V to -5.5V supply.

Inputs

The maximum magnitude of the differential input from D to \overline{D} is 3.0V. This limit also applies to the difference between any reference voltage input and a single-ended input.

The differential inputs have bias resistors that drive the outputs to a differential low when the inputs are open. The inverting input, \overline{D} , is biased with a $50\text{k}\Omega$ pullup to VCC and a $100\text{k}\Omega$ pulldown to VEE. The noninverting input, D, is biased with an $80\text{k}\Omega$ pullup to VCC and a $60\text{k}\Omega$ pulldown to VEE.

Specifications for the high and low voltages of the differential input (VIHD and VILD) and the differential input voltage (VIHD - VILD) apply simultaneously (VILD cannot be higher than VIHD).

Outputs

Output levels are referenced to VCC and are considered PECL/LVPECL or ECL/LVECL, depending on the level of the VCC supply. With VCC connected to a positive supply and VEE connected to GND, the outputs are PECL/LVPECL. The outputs are ECL/LVECL when VCC is connected to GND and VEE is connected to a negative supply.

A differential input of at least $\pm 100\text{mV}$ switches the outputs to the VOH and VOL levels specified in the *DC Electrical Characteristics* table.

Applications Information

Supply Bypassing

Bypass VCC to VEE with high-frequency surface-mount ceramic $0.1\mu\text{F}$ and $0.01\mu\text{F}$ capacitors in parallel as close to the device as possible, with the $0.01\mu\text{F}$ value capacitor closest to the device. Use multiple parallel ground vias for low inductance.

Traces

Input and output trace characteristics affect the performance of the MAX9320B. Connect each signal of a differential input or output to a 50Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

Output Termination

Terminate outputs through 50Ω to VCC - 2V or use an equivalent Thevenin termination. Terminate both outputs and use the same termination on each for the lowest output-to-output skew. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q0 is used as a single-ended output, terminate both Q0 and $\overline{Q0}$.

Chip Information

TRANSISTOR COUNT: 182

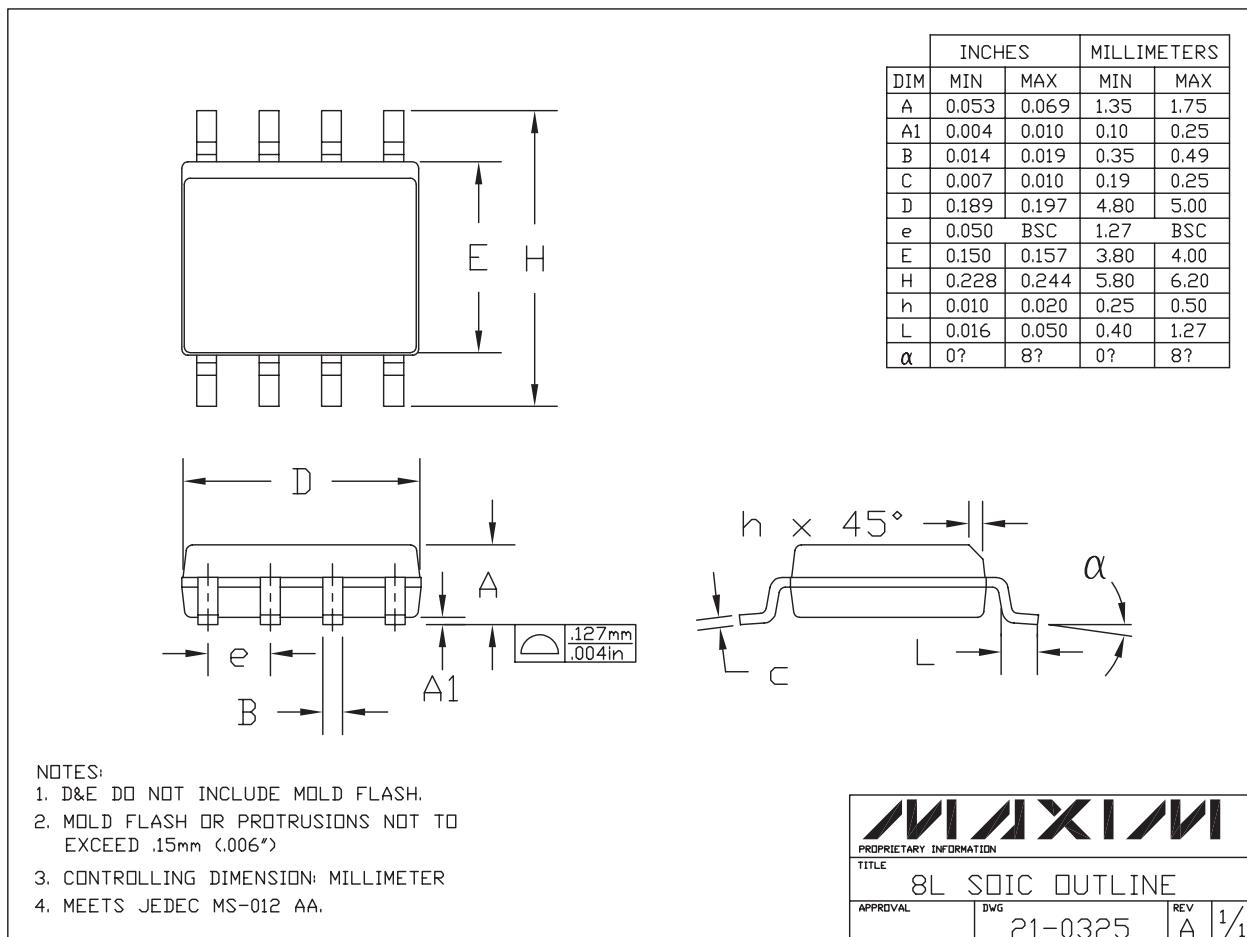
1:2 Differential PECL/ECL/LVPECL/LVECL Clock and Data Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX9320B

MAX9320B, 3x3 EPS



Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.