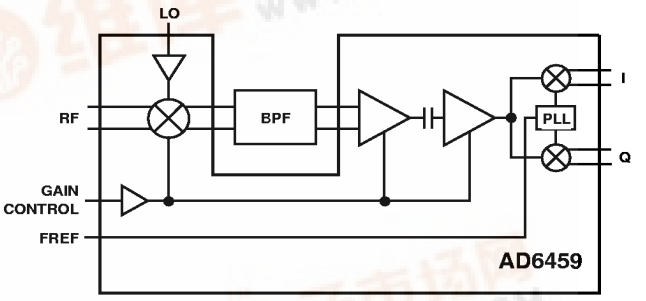
GSM 3 V Receiver IF Subsystem

AD6459

FEATURES

- Fully Compliant with Standard and Enhanced GSM Specification
  - –11 dBm Input 1 dB Compression Point
  - 0 dBm Input Third Order Intercept
  - 10 dB SSB Noise Figure (50 Ω)
  - DC-500 MHz RF and LO Bandwidths
- Linear IF Amplifier
  - Linear-in-dB and Stable over Temperature
- Voltage Gain Control
- Quadrature Demodulator
  - On-Board Phase-Locked Quadrature Oscillator
  - Demodulates IFs from 5 MHz to 50 MHz
- Low Power
  - 8 mA at Midgain
  - 2 μA Sleep Mode Operation
  - 2.7 V to 5.5 V Operation
- Interfaces to AD7013, AD7015 and AD6421 Baseband Converters
- 20-Lead SSOP

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD6459 is a 3 V, low power receiver IF subsystem for operation at input frequencies as high as 500 MHz and IFs from 5 MHz up to 50 MHz. It is optimized for operation in GSM, DCS1800 and PCS1900 receivers. It consists of a mixer, an IF amplifier, I and Q demodulators, a phase-locked quadrature oscillator, a precise AGC subsystem, and a biasing system with external power-down.

The AD6459's low noise, high intercept mixer is a doubly-balanced Gilbert-Cell type. It has a nominal –11 dBm input-referred 1 dB compression point and a 0 dBm input-referred third-order intercept. The mixer section of the AD6459 also includes a local oscillator (LO) preamplifier, which lowers the required LO drive to –16 dBm.

The gain control input accepts an external gain-control voltage input from an external AGC detector or a DAC. It provides an 80 dB gain range with 27 mV/dB gain scaling.

The I and Q demodulators provide in-phase and quadrature baseband outputs to interface with Analog Devices' AD7013 (IS54, TETRA, MSAT) AD7015 and AD6421 (GSM, DCS1800, PCS1900) baseband converters. An on-board quadrature VCO that is externally phase-locked to the IF signal drives the I and Q demodulators. This locked reference signal is normally provided by an external VCTCXO under the control of the radio's digital processor. The AD6459 can also provide demodulation of N-PSK and N-QAM in many non-TDMA systems when used with external analog carrier recovery systems such as the Costas Loop. Finally, the VCO can be phase-locked to a frequency that is deliberately offset from the IF as in the case of a Beat-Frequency oscillator (BFO) resulting in the product detection of CW or SSB.

The AD6459 uses supply voltages from 2.7 V to 5.5 V over the temperature range of –40°C to +85°C. Operation is enabled by a CMOS logical level; response time is typically < 80 μs. When disabled, the standby current is reduced to 2 μA.

The AD6459 comes in a 20-pin shrink small outline (SSOP) surface mount package.

REV. 0

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AD6459—SPECIFICATIONS (@ T_A = +25°C, V_P = 3.0 V, GREF = 1.2 V, unless otherwise noted)

Model / Parameter	Conditions	AD6459ARS Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
MIXER					
Maximum RF and LO Frequency			500		MHz
AGC Conversion Gain Variation	0.2 V < V_{GAIN} < 2.25 V		–3 to +16		dB
Input 1 dB Compression Point	@ V_{GAIN} = 0.2 V		–11		dBm
Input Third-Order Intercept	@ V_{GAIN} = 0.2 V		0		dBm
SSB Noise Figure[1]	@ Z_S = 50 Ω, F_{RF} = 240 MHz, F_{LO} = 229.3 MHz at –16 dBm		10		dB
Mixer Output Bandwidth at MXOP	@ –3 dB		80		MHz
IF AMPLIFIERS					
AGC Gain Variation	0.2 V < V_{GAIN} <2.25 V		–13 to +46		dB
Input Referred Noise	AC Short Circuit Input		3		nV/√Hz
Input Resistance	@ V_{GAIN} = 0.2 V		5		kΩ
Bandwidth	@ –3 dB		50		MHz
I AND Q DEMODULATORS					
Demodulation Gain			17		dB
Output Voltage Range	Differential, IRXP, IRXN, QRXP, QRXN	0.3		V_P – 0.2	V
Output Voltage Common-Mode Level	(Not Power Supply Dependent)		1.5		V
Output Offset Voltage	Differential, V_{GAIN} = GREF	–150		150	mV
Error in Quadrature	Differential from I to Q, IF = 13 MHz		1.5	3.5	Degree
Amplitude Match	I to Q		0.25		dB
I/Q Output Bandwidth	C_{LOAD} = 10 pF		2		MHz
Output Resistance	Each Pin		4.7		kΩ
GAIN CONTROL					
Total Gain Control Range	Mixer + IF + Demod, 0.2 V < V_{GAIN} <2.25 V		76		dB
Control Voltage Range at GAIN		0.2		2.4	V
Gain Scaling		23	27	32	mV/dB
Gain Law Conformance			±0.5		dB
Bias Current at GREF			0.5		µA
Input Resistance at GAIN			20		kΩ
PLL					
Frequency Range		5		50	MHz
Phase Noise			0.5		Degree rms
Acquisition Time	IF = 19.5 MHz, Using Suggested Filter		80		µs
Input Drive Level (FREF)		100		VPOS	mV
POWER-DOWN INTERFACE					
Logical Threshold	Power Up on Logical High		1.5		V
Input Current for Logical High			75		µA
Turn-On Response Time	To Fully Meet Specifications (PLL Lock)		80		µs
Turn-Off Response time	To 200 µA Supply Current		1		µs
Standby Current			2		µA
POWER SUPPLY					
Supply Range		2.7		5.5	V
Supply Current	@ V_{GAIN} = 1.2 V		8		mA
OPERATING TEMPERATURE					
T_{MIN} to T_{MAX}	Operation to 3.3 V Minimum Supply Voltage	–40		+85	°C
	Operation to 2.7 V Minimum Supply Voltage	–25		+85	°C

NOTES

[1]Including IF noise and using suggested filter, at V_{GAIN} = 0.2 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage VPS1, VPS2 to COM1, COM2 ..... +5.5 V
Internal Power Dissipation[2] ..... 600 mW
Operating Temperature Range ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature, Soldering (60 sec) .....+300°C

NOTES

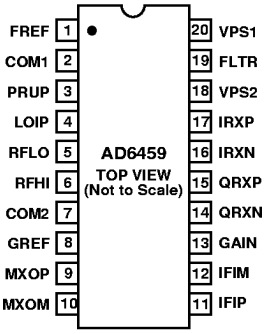
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended rating conditions for extended periods may affect device reliability.

[2]Thermal Characteristics: 20-lead SSOP package: θ_{JA} = 126°C/W.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD6459ARS	–25°C to +85°C for 2.7 V to 5.5 V –40°C to +85°C for 3.3 V to 5.5 V	20-Pin Plastic SSOP	RS-20

PIN CONNECTION
20-Pin SSOP (RS-20)



PIN DESCRIPTIONS

Pin	Pin Label	Description	Function
1	FREF	Frequency Reference Input	Demodulation LO Input. May either be 3 V CMOS input or >100 mV p-p. AC-coupled for lowest stand by current.
2	COM1	Common 1	Ground.
3	PRUP	Power Up Input	CMOS Compatible Power-Up Control; <1.5 V = OFF, >1.5 V = ON.
4	LOIP	Local Oscillator Input	AC-Coupled LO Input. 50 mV p-p drive needed, 500 mV p-p max.
5	RFLO	RF "Low" Input	Mixer Differential Input. AC-coupled.
6	RFHI	RF "High" Input	Mixer Differential Input. AC-coupled.
7	COM2	Common 2	Ground.
8	GREF	Gain Reference Input	High Impedance Input. Sets gain scaling, typically 1.2 V.
9	MXOP	Mixer Output "Plus"	Differential Output of the Mixer. See Figure 22.
10	MXOM	Mixer Output "Minus"	Differential Output of the Mixer. See Figure 22.
11	IFIP	IF Input "Plus"	Differential Input of Variable Gain Amplifier. AC-coupled.
12	IFIM	IF Input "Minus"	Differential Input of Variable Gain Amplifier. AC-coupled.
13	GAIN	Gain Control Input	0.2 V–2.4 V Using 3 V Supply. Max gain at 0.2 V.
14	QRXN	Q Output "Negative"	Differential Q Output. Output resistance 4.7 kΩ.
15	QRXP	Q Output "Positive"	Differential Q Output. Output resistance 4.7 kΩ.
16	IRXN	I Output "Negative"	Differential I Output. Output resistance 4.7 kΩ.
17	IRXP	I Output "Positive"	Differential I Output. Output resistance 4.7 kΩ.
18	VPS2	VPOS Supply 2	Supply Voltage.
19	FLTR	PLL Loop Filter	Series RC Loop Filter. Connected to VPS2.
20	VPS1	VPOS Supply 1	Supply Voltage.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD6459 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

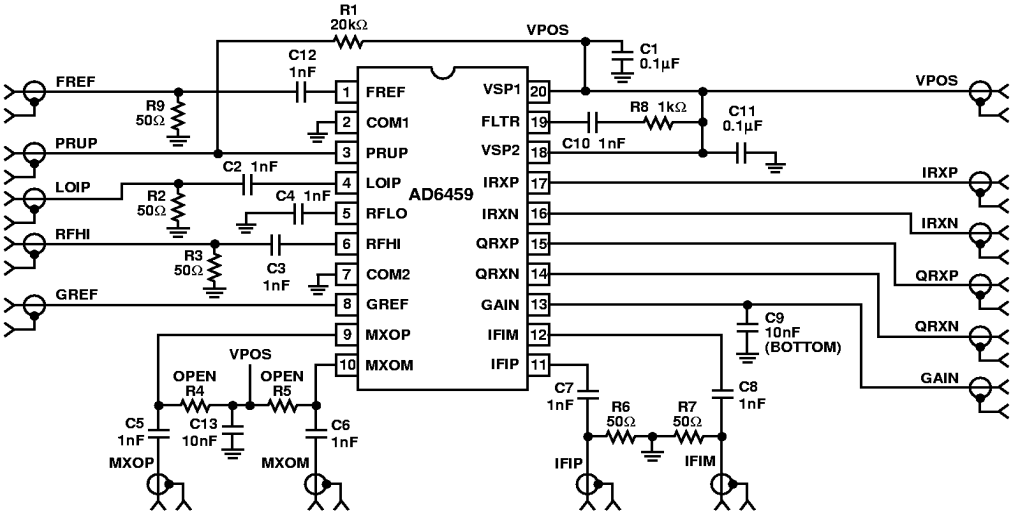


Figure 1. AD6459 Characterization Board

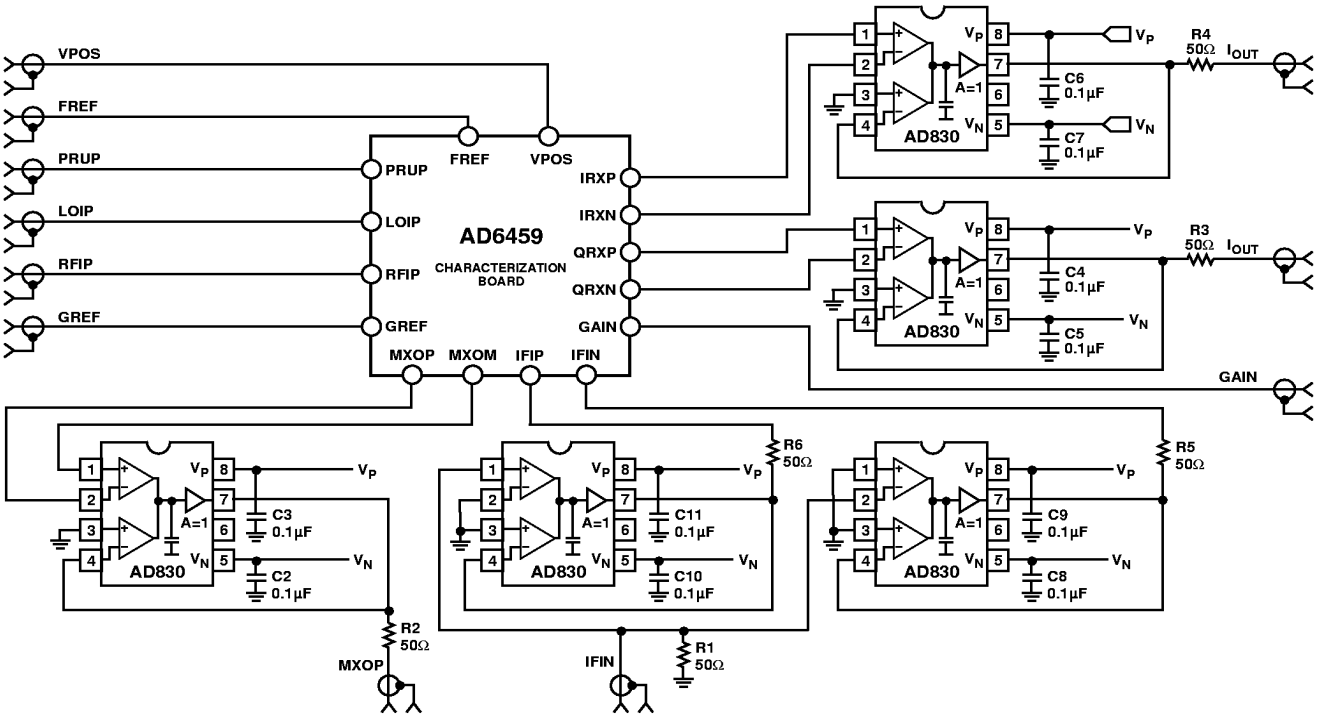


Figure 2. Characterization Test Set

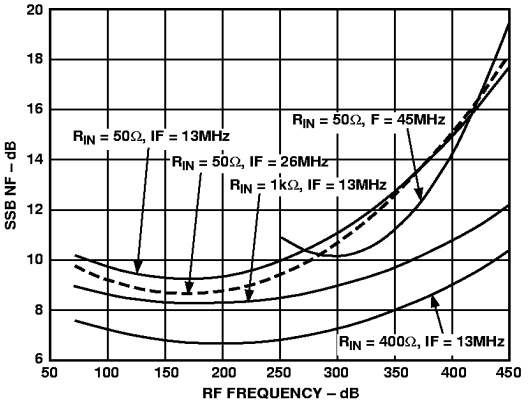


Figure 3. Mixer Noise Figure vs. RF Frequency

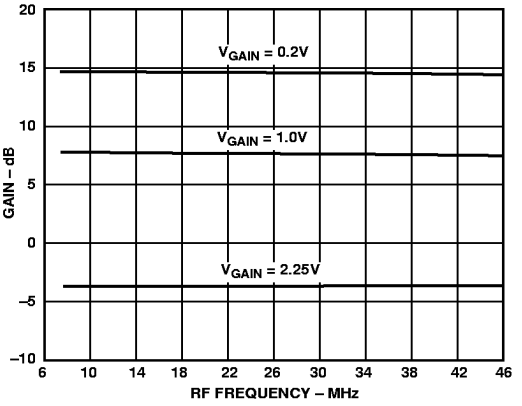


Figure 6. Mixer Conversion Gain vs. IF Frequency, T_A = +25°C, V_{POS} = 2.7 V, V_{REF} = 1.2 V, FRF = 250 MHz

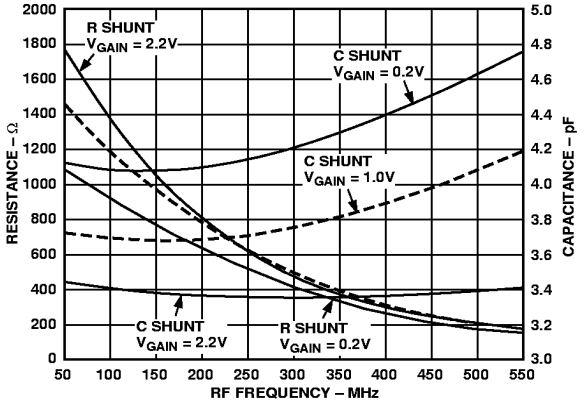


Figure 4. Mixer Input Impedance vs. RF Frequency, V_{POS} = 2.7 V, T_A = +25°C

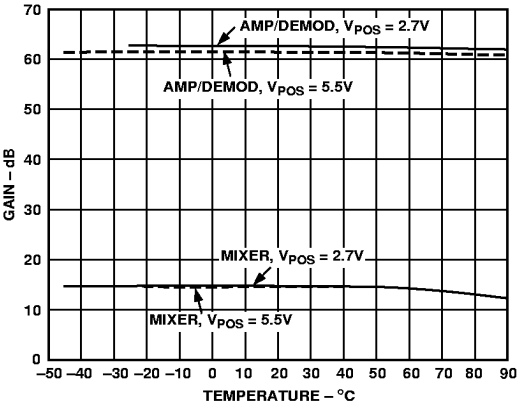


Figure 7. Mixer Conversion Gain and IF Amplifier/ Demodulator Gain vs. Temperature, V_{GAIN} = 0.2 V, V_{REF} = 1.2 V , F_{IF} = 26 MHz, F_{RF} = 250 MHz

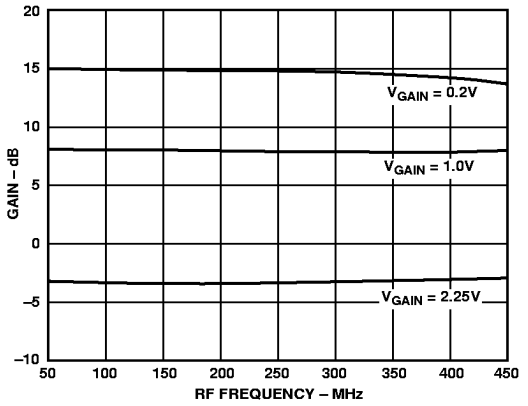


Figure 5. Mixer Conversion Gain vs. RF Frequency, T_A = +25°C, V_{POS} = 2.7 V, V_{REF} = 1.2 V, F_{IF} = 26 MHz

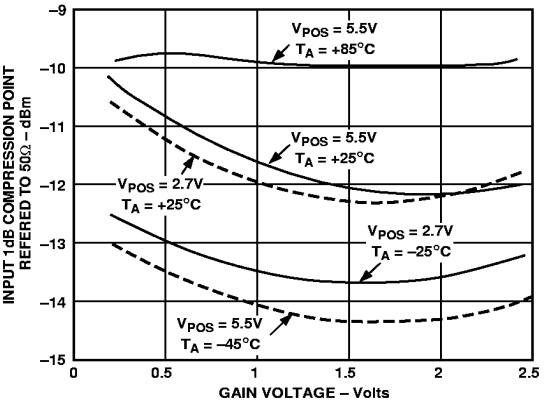


Figure 8. Mixer Input 1 dB Compression Point vs. V_{GAIN}, V_{REF} = 1.2 V, F_{RF} = 250 MHz, F_{IF} = 26 MHz

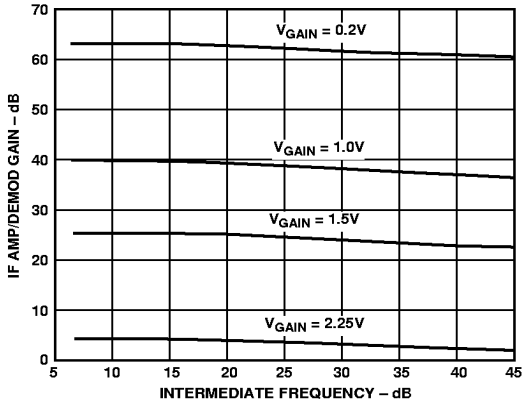


Figure 9. IF Amplifier and Demodulator Gain vs. Frequency, T_A = +25°C, V_{POS} = 2.7 V, V_{REF} = 1.2 V

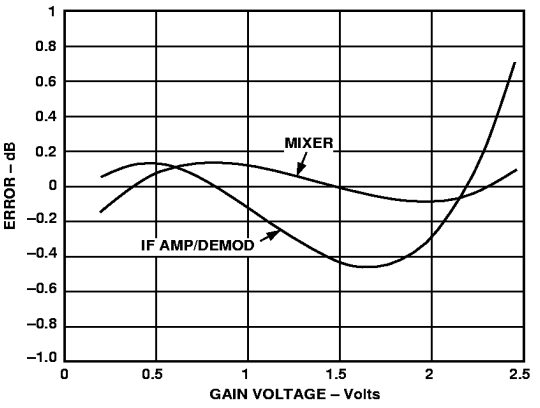


Figure 12. AD6459 Gain Error vs. Gain Control Voltage, Representative Part

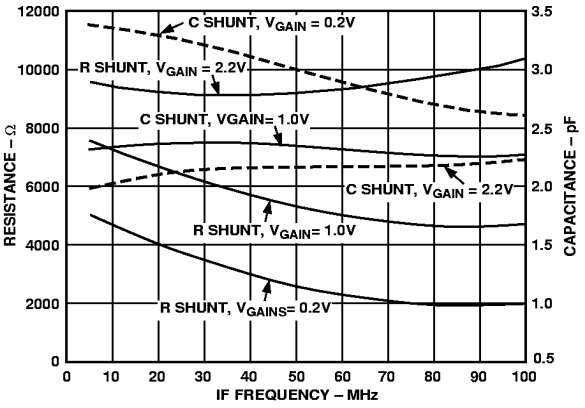


Figure 10. IF Amplifier Input Impedance vs. Frequency, T_A = +25°C, V_{POS} = 2.7 V, V_{REF} = 1.2 V

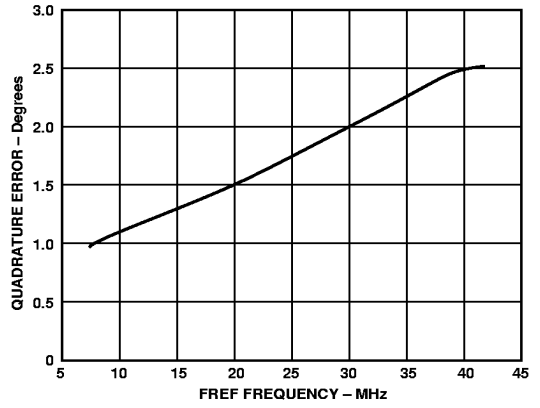


Figure 13. Demodulator Quadrature Error vs. F_{REF} Frequency, T_A = +25°C, V_{POS} = 2.7 V

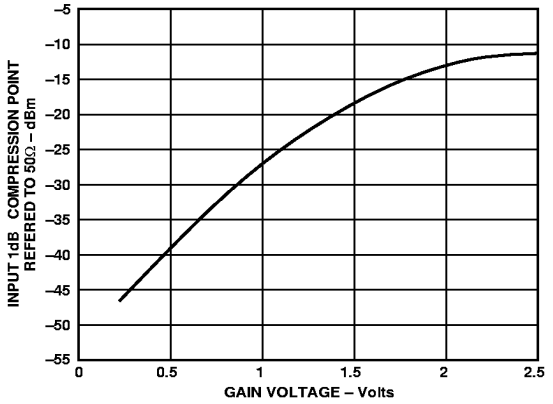


Figure 11. IF Amplifier/Demodulator Input 1 dB Compression Point vs. V_{GAIN}, F_{IF} = 19.5 MHz, V_{REF} = 1.2 V, T_A = +25°C, V_{POS} = 2.7 V

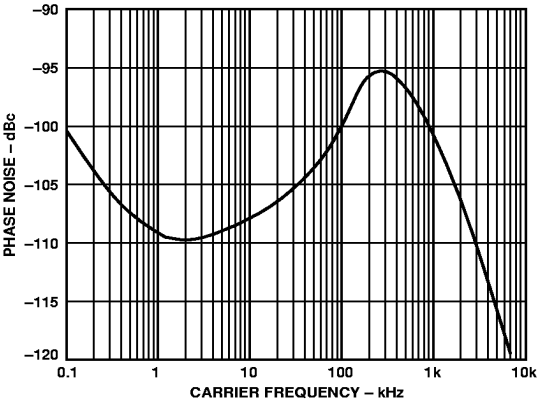


Figure 14. PLL Phase Noise vs. Frequency, V_{POS} = 3 V, C10 = 1 nF, F_{REF} = 13 MHz

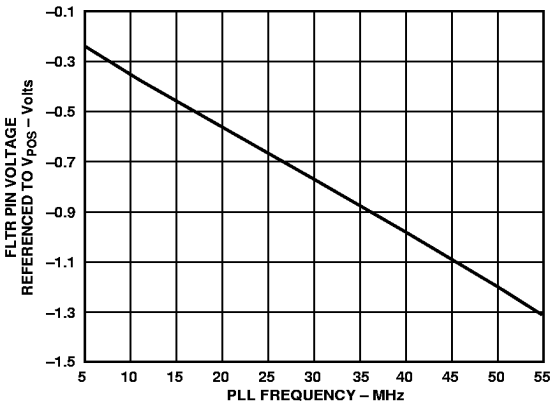


Figure 15. PLL Loop Voltage at FLTR Pin (KVCO) vs. Frequency

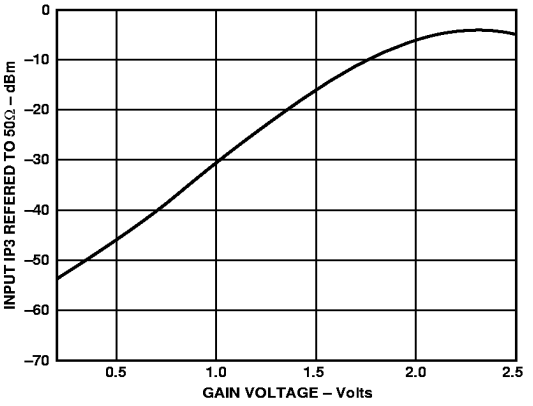


Figure 17. System (Mixer + IF LC Filter + I F Amplifier + Demodulator) IP3 vs. Gain, T_A = +25°C, V_{POS} = 2.7 V, IF = 13 MHz, V_{REF} = 1.2 V

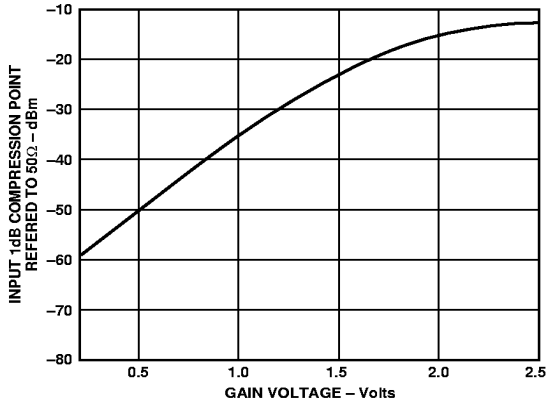


Figure 16. System (Mixer + IF LC Filter +IF Amplifier + Demodulator) 1 dB Compression Point vs. Gain, T_A = +25°C, V_{POS} = 2.7 V, F_{IF} = 13 MHz, V_{REF} = 1.2 V

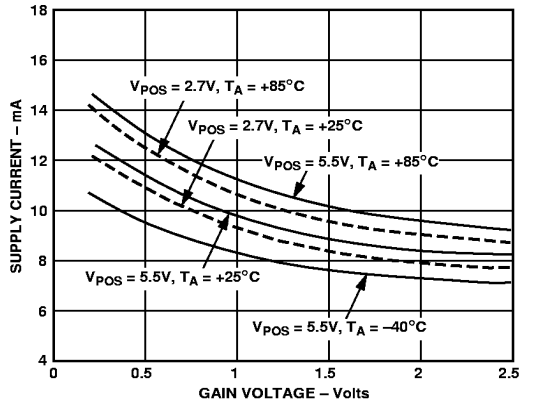


Figure 18. Power Supply Current vs. Gain Control Voltage, V_{REF} = 1.2 V

PRODUCT OVERVIEW

The AD6459 provides most of the active circuitry required to realize a complete low power, single-conversion superheterodyne receiver, or the latter part of a double-conversion receiver, at input frequencies up to 500 MHz, with an IF from 5 MHz to 50 MHz. The internal I/Q demodulators, and their associated phase-locked loop, support a wide variety of modulation modes, including n-PSK, n-QAM and GMSK. A single positive supply voltage of 3 V is required (2.7 V minimum, 5.5 V maximum) at a typical supply current of 8 mA at midgain. In the following discussion, V_{POS} will be used to denote the power supply voltage, which will be normally assumed to be 3 V.

Figure 20 shows the main sections of the AD6459. It consists of a variable-gain UHF mixer and a linear two-stage IF strip, which together provide a calibrated voltage-controlled gain range of more than 76 dB, followed by dual quadrature demodulators. These are driven by inphase and quadrature clocks that are generated by a Phase-Locked Loop (PLL), which is locked to a corrected external reference. A CMOS-compatible power-down interface completes the AD6459.

Mixer

The UHF mixer is an improved Gilbert-cell design and can operate from low frequencies (it is internally dc-coupled) up to an RF input of 500 MHz. The dynamic range at the input of the mixer is determined, at the upper end, by the maximum input signal level of ±90 mV (–11 dBm in 50 Ω between RFHI and RFLO) up to which the mixer remains essentially linear, and at the lower end, by the noise level. It is customary to define the linearity of a mixer in terms of its 1 dB gain-compression point and third-order intercept, which for the AD6459 are –11 dBm and 0 dBm, respectively, in a 50 Ω system.

The mixer's RF input port is differential; that is, pin RFLO is functionally identical to RFHI, and these nodes are internally biased. The RF port can be modeled as a parallel RC circuit as shown in Figure 19.

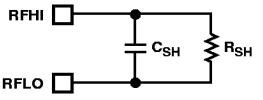


Figure 19. Mixer Port Modeled as a Parallel RC Network

The local oscillator (LO) input is internally biased at V_P–0.8 V and must be ac coupled. The LO interface includes a preamplifier that minimizes the drive requirements, thus simplifying the oscillator design and reducing LO leakage from the RF port. The LO requires a single-sided drive of ±50 mV, or –16 dBm in a 50 Ω system. For operation above 300 MHz, noise figure can be improved by increasing the LO level.

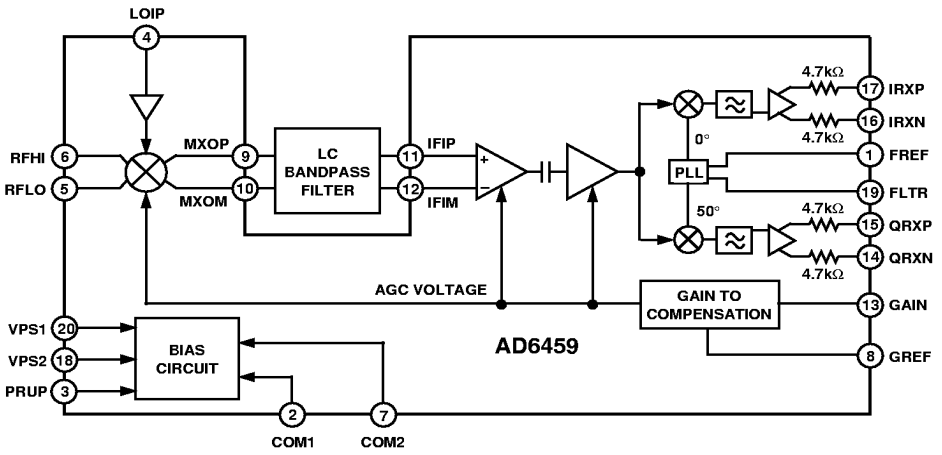


Figure 20. Functional Block Diagram

The output of the mixer is differential. The nominal conversion gain is specified for operation into a 19.5 MHz LC IF bandpass filter as shown in Figure 21 and Table I.

The conversion gain is measured between the mixer input and the input of this filter and varies between –5 dB and +15 dB.

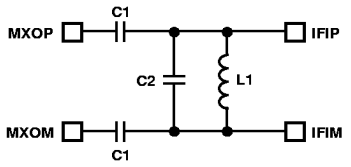


Figure 21. Suggested IF Filter Inserted Between the Mixer's Output Port and the Amplifier's Input Port

Table I. Filter Component Values for Selected Frequencies

Frequency	C1	L1	C2
13 MHz	27 pF	0.82 µH	180 pF
19.5 MHz	27 pF	0.56 µH	110 pF
26 MHz	22 pF	0.39 µH	82 pF
40 MHz	22 pF	0.12 µH	100 pF

The maximum permissible signal level between MXOP and MXOM is determined by the maximum gain control voltage.

The mixer output port, having pull-up resistors of 250 Ω to V_{POS}, is shown in Figure 22.

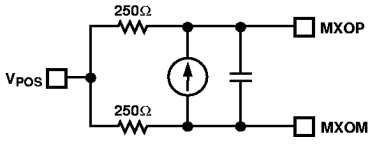


Figure 22. Mixer Output Port

IF Amplifier

Most of the gain in the AD6459 is provided by the IF amplifier strip, which comprises two stages. Both are fully differential and each has a gain span of 26 dB for the AGC voltage range of 0.2 V to 2.25 V. Thus, in conjunction with the variable gain of the mixer, the total gain span is 76 dB. The overall IF gain varies from –13 dB to 45 dB for the nominal AGC voltage of 0.2 V to 2.25 V. Maximum gain is at V_{GAIN} = 0.2 V.

The IF input is differential, at IFIP and IFIM. Figure 23 shows a simplified schematic of the IF interface modeled as parallel RC network.

The IF's small-signal bandwidth is approximately 50 MHz from IFIP and IFIM through the demodulator.

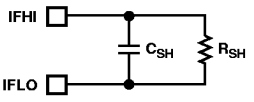


Figure 23. IF Amplifier Port Modeled as a Parallel RC Network

Gain Scaling

The AD6459's overall gain, expressed in decibels, is linear with respect to the AGC voltage V_{GAIN} at pin GAIN. The gain of all sections is maximum when V_{GAIN} is 0.2 V and falls off as the bias is increased to V_{GAIN} = 2.25 V. The gain is independent of the power supply voltage. The gain of all stages changes simultaneously. The AD6459's gain scaling is also temperature compensated.

Note that GAIN pin of the AD6459 is an input driven by an external low impedance voltage source, normally a DAC, under the control of the radio's digital processor.

The gain-control scaling is directly proportional to the reference voltage applied to the pin GREF and is independent of the power supply voltage. When this input is set to the nominal value of 1.2 V, the scale is nominally 27 mV/dB (37 dB/V). Under these conditions, 76 dB of gain range (mixer plus IF) corresponds to a control voltage of $0.2\ V \le V_{GAIN} \le 2.25\ V$. The final centering of this 2.05 V range depends on the insertion losses of the IF filters used.

Pin GREF can be tied to an external voltage reference (V_{REF}) provided, for example, by an AD1580 (1.21 V) voltage reference.

When using the Analog Devices AD7013 (IS54, TETRA, and satellite receiver applications) and AD7015 or AD6421 (GSM, DCS1800, PCS1900) baseband converters, the external reference may also be provided by the reference output of the baseband converters. The interface between the AD6459 and the AD6421 baseband converter is shown in Figure 24. The AD7015 baseband converter provides a V_R of 1.23 V. An auxiliary DAC in the AD7015 can be used to generate the AGC voltage. Since it uses the same reference voltage, the numerical input to this DAC provides an accurate RSSI value in digital form, no longer requiring the reference voltage to have high absolute accuracy.

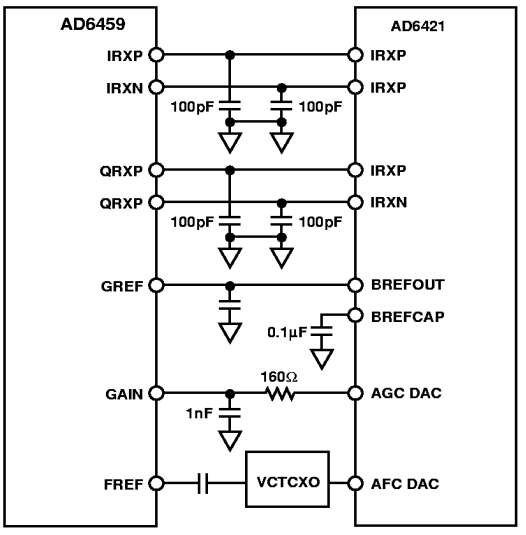


Figure 24. Interfacing the AD6459 to the AD6421 Baseband Converter

I/Q Demodulators

Both demodulators (I and Q) receive their inputs internally from the IF amplifiers. Each demodulator comprises a full-wave synchronous detector followed by an 8 MHz, two-pole low-pass filter, producing differential outputs at pins IRXP and IRXN, and QRXP and QRXN. Using the I and Q demodulators for IFs above 50 MHz is precluded by the 5 MHz to 50 MHz range of the PLL used in the demodulator section.

The I and Q outputs are differential and can swing up to 2.2 V p-p at the low supply voltage of 2.7 V. They are nominally centered at 1.5 V, independent of power supply. They can therefore directly drive the RX ADCs in the AD7015 baseband converter, which require an amplitude of 1.23 V to fully load them when driven by a differential signal. The conversion gain of the I and Q demodulators is 17 dB.

For IFs of less than 8 MHz, the on-chip low-pass filters (8 MHz cutoff) do not adequately attenuate the IF or feedthrough products; thus, the maximum input voltage must be limited to allow sufficient headroom at the I and Q outputs for not only the desired baseband signal but also the unattenuated higher-order demodulation products. These products can be removed by an external low-pass filter. A simple 1-pole RC filter with its corner above the modulation bandwidth is sufficient to attenuate undesired outputs. The design of the RC filter is eased by the 4.7 kΩ resistor integrated at each I and Q output pin.

Phase-Locked Loop

The demodulators are driven by quadrature signals that are provided by a variable-frequency quadrature oscillator (VFQO), phase-locked to a reference signal applied to pin FREF. When this signal is at the IF, inphase and quadrature baseband outputs are generated at the I output (IRXP and IRXN) and Q output (QRXP and QRXN), respectively. The quadrature accuracy of this VFQO is typically within ±1.5° at 19.5 MHz. A simplified diagram of the FREF input is shown in Figure 25.

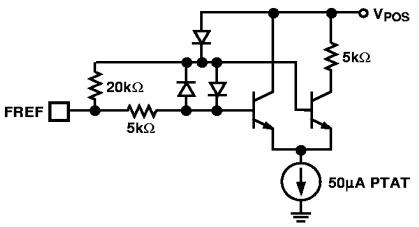


Figure 25. Simplified Schematic of the FREF interface

The VFQO operates from 5 MHz to 50 MHz and is controlled by the voltage between VPOS and FLTR. In normal operation a series RC network, forming the PLL loop filter, is connected from FLTR to V_{POS}. The use of an integral sample-hold system ensures that the frequency-control voltage on pin FLTR remains held during power-down, so reacquisition of the carrier occurs in less than 80 µs.

In practice, the probability of a phase mismatch at power-up is high, so the worst case linear settling period to full lock needs to be considered in making filter choices. This is typically < 80 µs for a quadrature phase error of ±3° at an IF of 19.5 MHz. Note that the VFQO always provides quadrature between its own I and Q outputs, but the phasing between it and the reference carrier will swing around the final value during the PLL's settling time.

Bias System

The AD6459 operates from a single supply (V_{POS}) usually 3 V, at a typical supply current of 8 mA at midgain and T_A = +25°C, corresponding to a power consumption of 24 mW. Any voltage from 2.7 V to 5.5 V may be used.

The bias system includes a fast-acting active high CMOS-compatible power-up switch, allowing the part to idle at 2 µA when disabled. Biasing is generally proportional-to-absolute-temperature (PTAT) to ensure stable gain with temperature. Other special biasing techniques are used to ensure very accurate gain, stable over the full temperature range.

USING THE AD6459

In this section, we will focus on a few areas of special importance and include a few general application tips. As with any wideband high gain component, great care is needed in PC board layout. The location of the particular grounding points must be considered with due regard to the possibility of unwanted signal coupling.

The high sensitivity of the AD6459 leads to the possibility that unwanted local EM signals may have an effect on the performance. During system development, carefully-shielded test assemblies should be used. The best solution is to use a fully enclosed box enclosing all components with the minimum number of needed signal connectors (RF, LO, I and Q outputs) in miniature coax form.

Gain Distribution

As with all receivers, the most critical decisions in effectively using the AD6459 relate to the partitioning of gain between the various subsections (Mixer, IF Amplifier/Demodulator) and the placement of filters to achieve the highest overall signal-to-noise ratio and lowest intermodulation distortion.

Figure 26 shows an example of the main RF/IF signal path at maximum and minimum signal levels.

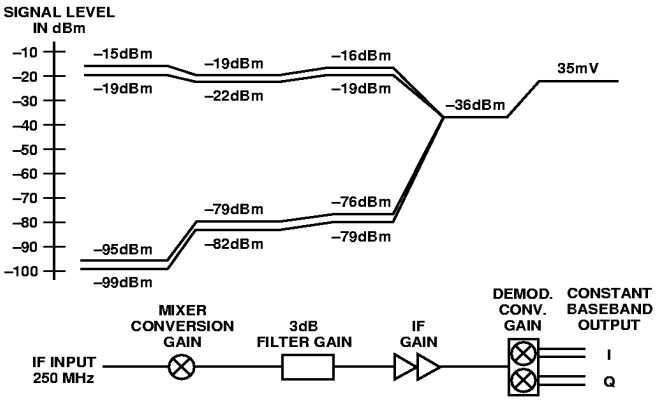


Figure 26. Signal Levels and Gain, Showing 76 dB Typical and 80 dB Maximum Range in an Example Application

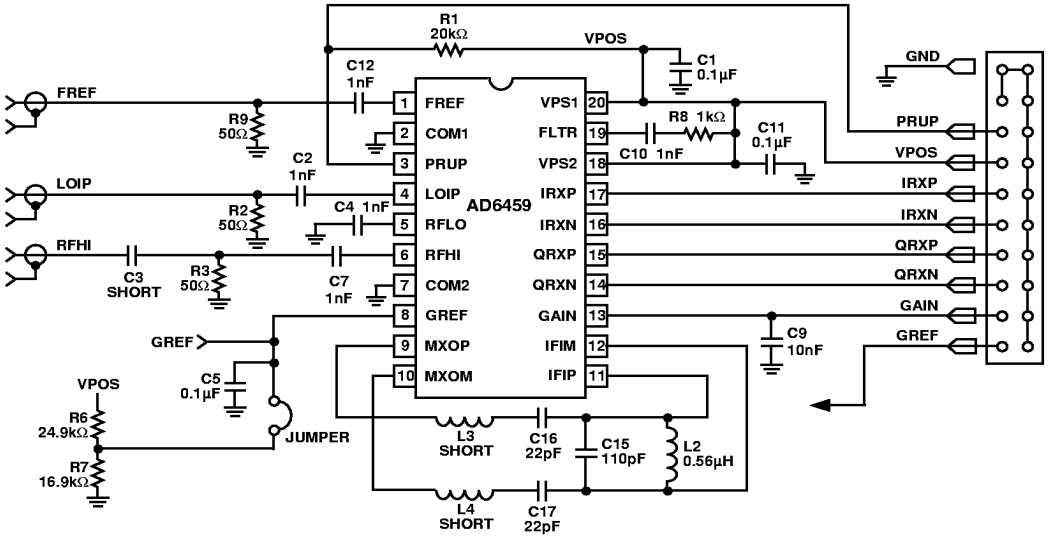


Figure 27. Evaluation Board as Received with 19.5 MHz Filter

Table II. AD6459 Evaluation Board Input and Output Connection

Reference Designation	Connector Type	Description	Coupling	Approximate Signal Level	Comments
RFHI	SMA	RF Input	AC	–11 dBm max	Input Is Terminated in 50 Ω
LOIP	SMA	LO Input	AC	500 mV p-p max	Input Is Terminated in 50 Ω
FREF	SMA	Demodulator Reference Input	AC	100 mV p-p min	Input Is Terminated in 50 Ω
MXOP	SMA	Mixer Output	NA	NA	Not Connected for Unbalanced Output Use XFMR
IFIP	SMA	IF Input	NA	NA	Not Connected for Unbalanced Output Use XFMR
J1	Jumper	On-Board GREF Bias	DC	0.4 V_{POS}	Two Resistors Divider
GREF	J2-1	External Reference Input	DC	1.2 V dc	Gain Scaling Reference from External ADC
GAIN	J2-2	Gain Bias Input	DC	0.2 V to 2.4 V dc	Maw Gain at 0.2 V
QRXN	J2-3	Q-Negative Output	DC–2 MHz	NA	Z Series = 4.7 kΩ
QRXP	J2-4	Q-Positive Output	DC–2 MHz	NA	Z Series = 4.7 kΩ
IRXN	J2-5	I-Negative Output	DC-2 MHz	NA	Z Series = 4.7 kΩ
IRXP	J2-6	I-Positive Output	DC-2 MHz	NA	Z Series = 4.7 kΩ
VPOS	J2-7	Power Supply Positive Input	DC	2.7 V to 5.5 V	Supply Voltage
PRUP	J2-8	Power Up	DC-2 MHz	CMOS	If Left Unconnected, Board Is Active
GND	J2-J9	Ground	DC	0 V	NA
GND	J2-10	Ground	DC	0 V	NA

AD6459 EVALUATION BOARD

The AD6459 evaluation board (Figure 27) consists of a AD6459, ground plane, I/O connectors, and a 19.5 MHz band pass filter. The RF, LO and FREF ports are terminated in 50 Ω to provide a broadband match or external signal generators.

The board provides SMA connectors for the RF, LO, demodulator reference, mixer output and IF input signals. The MXOP and IFIP connectors are left unconnected and are provided as a testing convenience. Footprints for broadband matching transformers and matching components are also provided to aid in stage breakout testing.

The remaining low frequency signals, including the I and Q interface, bias and power connections are made via a dual row pin header that acts as an Interface Connector located along the edges of the board. An on-board gain-reference 1.2 V biasing option is provided via a single jumper, J1. The evaluation board will not function without this jumper unless an external bias GREF is provided from an external reference that is normally provided by the associated ADC.

Full Path Configuration

As received, the board is configured for full-path evaluation from RFHI to the I and Q outputs. The one-pole LC resonant circuit provided represents a simple, yet balanced, IF bandpass filtering approach. The filter supplied is centered at 19.5 MHz, a common GSM intermediate frequency. Table I highlights the filter component values for other IF frequencies. RFHI and RFLO are true differential inputs, however for testing convenience, the RFLO terminal of the AD6459 is ac referenced to ground on the evaluation board. The GAIN bias input, which is bypassed with a 10 nF capacitor, is brought out to the interface connector. The PRUP input is provided with a 20 kΩ pull up resistor to V_{POS} that activates the board.

The four differential I and Q outputs are brought out unconditioned, directly to the interface connector. A high impedance, high bandwidth FET-type probe should be used when measuring the I and Q ports. Excessive capacitive or resistive loading of these ports will severely limit the video bandwidth and signal swing. The demodulator PLL filter installed on the evaluation board (R8, C10) can accommodate the full VFQO lock range specified.

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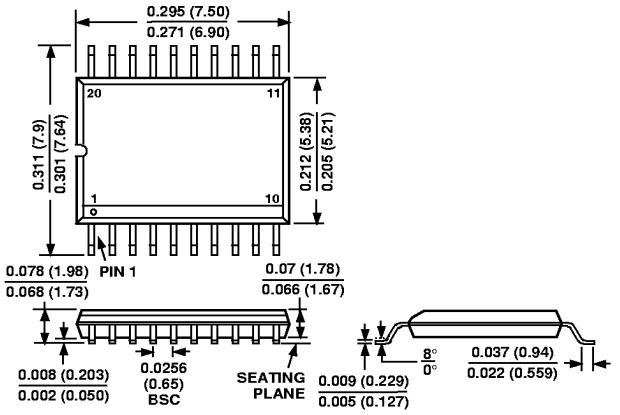
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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