19-1647; Rev 1; 6/00

MAXIM

MAX1711 Voltage Positioning Evaluation Kit

Evaluates: MAX1711

General Description

The MAX1711 evaluation kit (EV kit) demonstrates the high-power, dynamically adjustable notebook CPU application circuit with voltage positioning. Voltage positioning decreases CPU power consumption and reduces output capacitance requirements. This DC-DC converter steps down high-voltage batteries and/or AC adapters, generating a precision, low-voltage CPU core V_{CC} rail.

The MAX1711 EV kit provides a digitally adjustable 0.925V to 2V output voltage from a 7V to 24V battery input range. It delivers sustained output current of 12A and 14.1A peaks, operating at a 550kHz switching frequency, and has superior line- and load-transient response. The MAX1711 EV kit is designed to accomplish output voltage transitions in a controlled amount of time with limited input surge current.

This EV kit is a fully assembled and tested circuit board.

Ordering Information

PART	TEMP. RANGE	IC PACKAGE
MAX1711EVKIT	0°C to +70°C	24 QSOP

Quick-PWM is a trademark of Maxim Integrated Products.

Features

- ♦ Output Voltage Positioned
- ♦ Reduces CPU Power Consumption
- ♦ Lowest Number of Output Capacitors (only 4)
- ♦ High Speed, Accuracy, and Efficiency
- ♦ Fast-Response Quick-PWM™ Architecture
- ♦ 7V to 24V Input Voltage Range
- ♦ 0.925V to 2V Output Voltage Range
- ♦ 12A Load-Current Capability (14.1A peak)
- ♦ 550kHz Switching Frequency
- ♦ Power-Good Output
- ♦ 24-Pin QSOP Package
- ♦ Low-Profile Components
- ♦ Fully Assembled and Tested

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C4, C20	5	10µF, 25V ceramic capacitors Taiyo Yuden TMK432BJ106KM, Tokin C34Y5U1E106Z, or United Chemi-Con/Marcon THCR50E1E106ZT
C5, C6, C7, C16	4	220µF, 2.5V, 25mΩ low-ESR polymer capacitors Panasonic EEFUEOE 221R
C8	1	10µF, 6.3V ceramic capacitor Taiyo Yuden JMK325BJ106MN or TDK C3225X5R1A106M
C9	1	0.1µF ceramic capacitor
C10	0	0.01µF ceramic capacitor (not installed)
C11, C12	2	0.22µF ceramic capacitors
C13	0	0.1µF ceramic capacitor (not installed)
C14	1	470pF ceramic capacitor
C15	1	1µF ceramic capacitor
C18	1	1000pF ceramic capacitor
D1	1	2A Schottky diode SGS-Thomson STPS2L25U or Nihon EC31QS03L

DESIGNATION	QTY	DESCRIPTION
D2	1	100mA Schottky diode Central Semiconductor CMPSH-3
D3	1	1A Schottky diode Motorola MBRS130LT3, International Rectifier 10BQ040, or Nihon EC10QS03
D4	1	200mA switching diode Central Semiconductor CMPD2838
J1	1	Scope-probe connector Berg Electronics 33JR135-1
JU1	1	2-pin header
JU3–9	0	Not installed
L1	1	0.47µH power inductor Sumida CEP 125 series 4712-T006
N1	1	N-channel MOSFET (SO-8) International Rectifier IRF7811 or IRF7811A
N2, N3	2	N-channel MOSFET (SO-8) International Rectifier IRF7805 or IRF7811 or IRF 7811A

MAX1711 Voltage Positioning Evaluation Kit

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
N4, N5 (not installed)	0	N-channel MOSFETs Motorola 2N7002 or Central Semiconductor 2N7002
R1	1	20Ω ±5% resistor
R2	0	Not installed
R3	1	1MΩ ±5% resistor
R4	1	100kΩ ±5% resistor
R6	1	100kΩ ±1% resistor
R9	1	140kΩ ±1% resistor
R10	1	1kΩ ±5% resistor
R11	1	100Ω ±5% resistor
R12	1	0.005Ω ±1%, 1W resistor Dale WSL-2512-R005F
R13	1	1MΩ ±1% resistor
R14	1	10kΩ ±1% resistor
SW1	1	DIP-10 dip switch
SW2	1	Momentary switch, normally open Digi-Key P8006/7S
U1	1	MAX1711EEG (24-pin QSOP)
U2 (not installed)	0	Exclusive-OR gate (5-Pin SSOP) Toshiba TC4S30F
None	1	Shunt (JU1)
None	1	MAX1711 PC board
None	1	MAX1711 data sheet

Recommended Equipment

- 7V to 24V, >20W power supply, battery, or notebook AC adapter
- DC bias power supply, 5V at 100mA
- Dummy load capable of sinking 14.1A
- Digital multimeter (DMM)
- 100MHz dual-trace oscilloscope

Quick Start

1) Ensure that the circuit is connected correctly to the supplies and dummy load prior to applying power.
2) Ensure that the shunt is connected at JU1 ($\overline{SHDN}$ = V_{CC}).
3) Set switch SW1 per Table 1 to achieve the desired output voltage.
4) Connect +5V or ground to the AC Present pad to disable the transition detector circuit. See the *Dynamic Output Voltage Transitions* section for more information regarding the transition detector circuit.

Component Suppliers

SUPPLIER	PHONE	FAX
Central Semiconductor	516-435-1110	516-435-1824
Dale-Vishay	402-564-3131	402-563-6418
Fairchild	408-721-2181	408-721-1635
International Rectifier	310-322-3331	310-322-3332
Kemet	408-986-0424	408-986-1442
Motorola	602-303-5454	602-994-6430
Nihon	847-843-7500	847-843-2798
Panasonic	714-373-7939	714-373-7183
Sanyo	619-661-6835	619-661-1055
SGS-Thomson	617-259-0300	617-259-9442
Sumida	708-956-0666	708-956-0702
Taiyo Yuden	408-573-4150	408-573-4159
TDK	847-390-4373	847-390-4428
Tokin	408-432-8020	408-434-0375

Note: *Please indicate that you are using the MAX1711 when contacting these component suppliers.*

5) Turn on battery power prior to +5V bias power; otherwise, the output UVLO timer will time out and the FAULT latch will be set, disabling the regulator until +5V power is cycled or shutdown is toggled (**press the RESET button**).
6) Observe the output with the DMM and/or oscilloscope. Look at the LX switching-node and MOSFET gate-drive signals while varying the load current.

Detailed Description

This 14A buck-regulator design is optimized for a 550kHz frequency and output voltage settings around 1.6V. At V_{OUT} = 1.6V, inductor ripple is approximately 35%, with a resulting pulse-skipping threshold at roughly I_{LOAD} = 2.2A.

Setting the Output Voltage

Select the output voltage using the D0–D4 pins. The MAX1711 uses an internal 5-bit DAC as a feedback resistor voltage divider. The output voltage can be digitally set from 0.925V to 2V using the D0–D4 inputs. Switch SW1 sets the desired output voltage. See Table 1.

Table 1. MAX1710/1711 Output Voltage Adjustment Settings

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
1	1	0	0	0	1.60
1	1	0	0	1	1.55
1	1	0	1	0	1.50
1	1	0	1	1	1.45
1	1	1	0	0	1.40
1	1	1	0	1	1.35
1	1	1	1	0	1.30
0	1	1	1	1	Shutdown
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	Shutdown

Voltage Positioning

The MAX1711 EV kit uses voltage positioning to minimize the output capacitor requirements of the Intel Coppermine CPU's transient voltage specification (-7.5% to +7.5%). The output voltage is initially set slightly high (1.25%) and then allowed to regulate lower as the load current increases. R13 and R14 set the initial output voltage 20mV high, and R12 (5mΩ) causes the output voltage to drop with increasing load (60mV or about 4% of 1.6V at 12A).

Setting the output voltage high allows a larger step-down when the output current increases suddenly, and regulating at the lower output voltage under load allows a larger step-up when the output current suddenly decreases. Allowing a larger step size means that the output capacitance can be reduced and the capacitor's ESR can be increased. If voltage positioning is not used, one additional output capacitor is required to meet the same transient specification.

Reduced power consumption at high load currents is an additional benefit of voltage positioning. Because the output voltage is reduced under load, the CPU draws less current. This results in lower power dissipation in the CPU, though some extra power is dissipated in R12. For a 1.6V, 12A nominal output, reducing the output voltage 2.75% (1.25% - 4%) gives an output voltage of 1.556V and an output current of 11.67A. So the CPU power consumption is reduced from 19.2W to 18.16W. The additional power consumption of R12 is $5m\Omega \cdot 11.7A^2 = 0.68W$, and the overall power savings is 19.2 – (18.16 + 0.68) = 0.36W. In effect, 1W of CPU dissipation is saved and the power supply dissipates much of the savings, but both the net savings and the transfer of dissipation away from the hot CPU are beneficial.

Dynamic Output Voltage Transitions

If the DAC inputs (D0–D4) are changed, the output voltage will change accordingly. However, under some circumstances, the output voltage transition may be slower than desired. All transitions to a higher voltage will occur very quickly, with the circuit operating at the current limit set by the voltage at the ILIM pin. Transitions to a lower output voltage require the circuit or the load to sink current. If $\overline{SKIP}$ is held low (PFM mode), the circuit won't sink current, so the output voltage will decrease only at the rate determined by the load current. This is often acceptable, but some applications require output voltage transitions to be completed within a set time limit.

Powering CPUs with Intel's Geyserville technology is such an application. The specification requires that output voltage transitions occur within 100µs after a DAC code change. This fast transition timing means that the regulator circuit must sink as well as source current.

The simplest way of meeting this requirement is to use the MAX1711's fixed-frequency PWM mode (set $\overline{SKIP}$ high), allowing the regulator to sink or source currents equally. This EV kit is shipped with $\overline{SKIP}$ set high. Although this results in a V_{DD} quiescent current to 20mA or more, depending on the MOSFETs and

switching frequency used, it is often an acceptable choice. A similar but more clever approach is to use PWM mode only during transitions. This approach allows the regulator to sink current when needed and to operate with low quiescent current the rest of the time, but it requires that the system know when the transitions will occur. Any system with a changing output voltage must know when its output voltage changes occur. Usually, it is the system that initiates the transition, either by driving the DAC inputs to new levels or by selecting new DAC inputs with a digital mux. While it is possible for the regulator to recognize transitions by watching for DAC code changes, the glue logic needed to add that feature to existing controllers is unnecessarily complicated (refer to the MAX1710/MAX1711 data sheet, Figure 10). It is easier to use the chipset signal that selects DAC codes at the mux, or some other system signal to inform the regulator that a code change is occurring.

For easy modification, the MAX1711 EV kit is designed to use an external chipset signal to indicate DAC code transitions (install U2, R2, C10, C13; short JU9 and cut JU10). This signal connects to the EV kit's AC Present pad and should have 5V logic levels. Logic edges on AC Present are detected by exclusive-OR gate U2, which generates a 60µs pulse on each edge (determined by R2 and C10). These pulses drive $\overline{SKIP}$, allowing the regulator to sink current during transitions.

Because U2 is powered by V_{CC} (5V), the signal connected to AC Present must have 5V logic levels so that U2's output pulses will be symmetric for positive- and negative-going transitions. If the signal that's available to drive AC Present has a different logic level, either level-shift the signal or lift U2's supply pin and power it from the appropriate supply rail.

In addition to controlling $\overline{SKIP}$, the pulses from U2 have two other functions, which are optional. U2's output drives the gates of two small-signal MOSFETs, N4 and N5 (not installed). N4 is used to temporarily reduce the circuit's current limit, in effect soft-starting the regulator. This reduces the battery surge current, which otherwise would discharge (upward transitions) or charge (downward transitions) the regulator input (battery) at a rate determined by the regulator's maximum current limit. N5 pulls down on PGOOD during transitions, indicating that the output voltage is in transition.

Load-Transient Measurement

One interesting experiment is to subject the output to large, fast load transients and observe the output with an oscilloscope. This necessitates careful instrumentation of the output, using the supplied scope-probe jack. Accurate measurement of output ripple and load-transient response invariably requires that ground clip leads be completely avoided and that the probe hat be removed to expose the GND shield, so the probe can be plugged directly into the jack. Otherwise, EMI and noise pickup will corrupt the waveforms.

Most benchtop electronic loads intended for power-supply testing are unable to subject the DC-DC converter to ultra-fast load transients. Emulating the supply current di/dt at the CPU VCORE pins requires at least 10A/µs load transients. One easy method for generating such an abusive load transient is to solder a MOSFET, such as an MTP3055 or 12N05 directly across the scope-probe jack. Then drive its gate with a strong pulse generator at a low duty cycle (10%) to minimize heat stress in the MOSFET. Vary the high-level output voltage of the pulse generator to adjust the load current.

To determine the load current, you might expect to insert a meter in the load path, but this method is prohibited here by the need for low resistance and inductance in the path of the dummy-load MOSFET. There are two easy alternative methods for determining how much load current a particular pulse-generator amplitude is causing. The first and best is to observe the inductor current with a calibrated AC current probe, such as a Tektronix AM503. In the buck topology, the load current is equal to the average value of the inductor current. The second method is to first put on a static dummy load and measure the battery current. Then, connect the MOSFET dummy load at 100% duty momentarily, and adjust the gate-drive signal until the battery current rises to the appropriate level (the MOSFET load must be well heatsinked for this to work without causing smoke and flames).

Efficiency Measurements and Effective Efficiency

Testing the power conversion efficiency POUT/PIN fairly and accurately requires more careful instrumentation than might be expected. One common error is to use inaccurate DMMs. Another is to use only one DMM, and move it from one spot to another to measure the various input/output voltages and currents. This second error usually results in changing the exact conditions applied to the circuit due to series resistance in the ammeters. It's best to get four 3-1/2 digit, or better, DMMs that have been recently calibrated, and monitor V_{BATT}, V_{OUT}, I_{BATT}, and I_{LOAD} simultaneously, using separate test leads directly connected to the input and output PC board terminals. Note that it's inaccurate to test efficiency at the remote V_{OUT} and ground termi-

nals, because doing this incorporates the parasitic resistance of the PC board output and ground buses in the measurement (a significant power loss).

Remember to include the power consumed by the +5V bias supply when making efficiency calculations:

$$\text{Efficiency} = \frac{V_{OUT} \times I_{LOAD}}{(V_{BATT} \times I_{BATT}) + (5V \times I_{BIAS})}$$

The choice of MOSFET has a large impact on efficiency performance. The International Rectifier MOSFETs used were of leading-edge performance for the 12A application at the time this kit was designed. However, the pace of MOSFET improvement is rapid, so the latest offerings should be evaluated.

Once the actual efficiency data has been obtained, some work remains before an accurate assessment of a voltage-positioned circuit can be made. As discussed in the *Voltage Positioning* section, a voltage-positioned power supply can dissipate additional power while reducing system power consumption. For this reason, we use the concept of effective efficiency, which allows the direct comparison of a positioned and nonpositioned circuit's efficiency. Effective efficiency is the efficiency required of a nonvoltage-positioned circuit to equal the total dissipation of a voltage-positioned circuit for a given CPU operating condition.

Calculate effective efficiency as follows:

- Start with the efficiency data for the positioned circuit (V_{IN}, I_{IN}, V_{OUT}, I_{OUT}).
- Model the load resistance for each data point ($R_{LOAD} = V_{OUT} / I_{OUT}$).
- Calculate the output current that would exist for each R_{LOAD} data point in a nonpositioned application ($I_{NP} = V_{NP} / R_{LOAD}$, where V_{NP} = 1.6V in this example).
- Effective efficiency = $(V_{NP} \times I_{NP}) / (V_{IN} \times I_{IN})$ = calculated nonpositioned power output divided by the measured voltage-positioned power input.
- Plot the efficiency data point at the current I_{NP}.

The effective efficiency of the voltage-positioned circuit will be less than that of the nonpositioned circuit at light loads where the voltage-positioned output voltage is higher than the nonpositioned output voltage. It will be greater than that of the nonpositioned circuit at heavy loads where the voltage-positioned output voltage is lower than the nonpositioned output voltage.

Jumper and Switch Settings

Table 2. Jumper JU1 Functions (Shutdown Mode)

SHUNT LOCATION	$\overline{SHDN}$ PIN	MAX1711 OUTPUT
Installed	Connected to V_{CC}	MAX1711 enabled
Not Installed	Connected to GND	Shutdown mode, V_{OUT} = 0

Table 3. Jumpers JU3/JU4/JU5 Functions (Switching-Frequency Selection)

SHUNT LOCATION			TON PIN	FREQUENCY (kHz)
JU3	JU4	JU5		
Installed	Not Installed	Not Installed	Connected to V_{CC}	200
Not Installed	Installed	Not Installed	Connected to REF	400
Not Installed	Not Installed	Installed	Connected to GND	550
Not Installed	Not Installed	Not Installed	Floating	300

IMPORTANT: *Don't change the operating frequency without first recalculating component values because the frequency has a significant effect on the peak current-limit level, MOSFET heating, preferred inductor value, PFM/PWM switchover point, output noise, efficiency, and other critical parameters.*

Table 4. Jumper JU6 Functions (Fixed/Adjustable Current-Limit Selection)

SHUNT LOCATION	ILIM PIN	CURRENT-LIMIT THRESHOLD
Installed	Connected to V_{CC}	100mV
Not Installed	Connected to GND via an external resistor divider, R6/R9. Refer to the Pin Description ILIM section in the MAX1711 data sheet for more information.	Adjustable between 50mV and 200mV

Table 5. Jumpers JU9/JU10 Functions (FBS and FB Integrator Disable Selection)

SHUNT LOCATION		$\overline{SKIP}$ PIN
JU9	JU10	
Installed	Not Installed	Connected to V_{CC}
Not Installed	Installed	Connected to the output of U2

Table 6. Troubleshooting Guide

SYMPTOM	POSSIBLE PROBLEM	SOLUTION
Circuit won't start when power is applied.	Power-supply sequencing: +5V bias supply was applied first.	Press the RESET button.
Circuit won't start when RESET is pressed, +5V bias supply cycled.	Output overvoltage due to shorted high-side MOSFET.	Replace the MOSFET.
	Output overvoltage due to load recovery overshoot.	Reduce the inductor value, raise the switching frequency, or add more output capacitance.
	Overload condition.	Remove the excessive load.
	Broken connection, bad MOSFET, or other catastrophic problem.	Troubleshoot the power stage. Are the DH and DL gate-drive signals present? Is the 2V V_{REF} present?
On-time pulses are erratic or have unexpected changes in period.	VBATT power source has poor impedance characteristic.	Add a bulk electrolytic bypass capacitor across the benchtop power supply, or substitute a real battery.

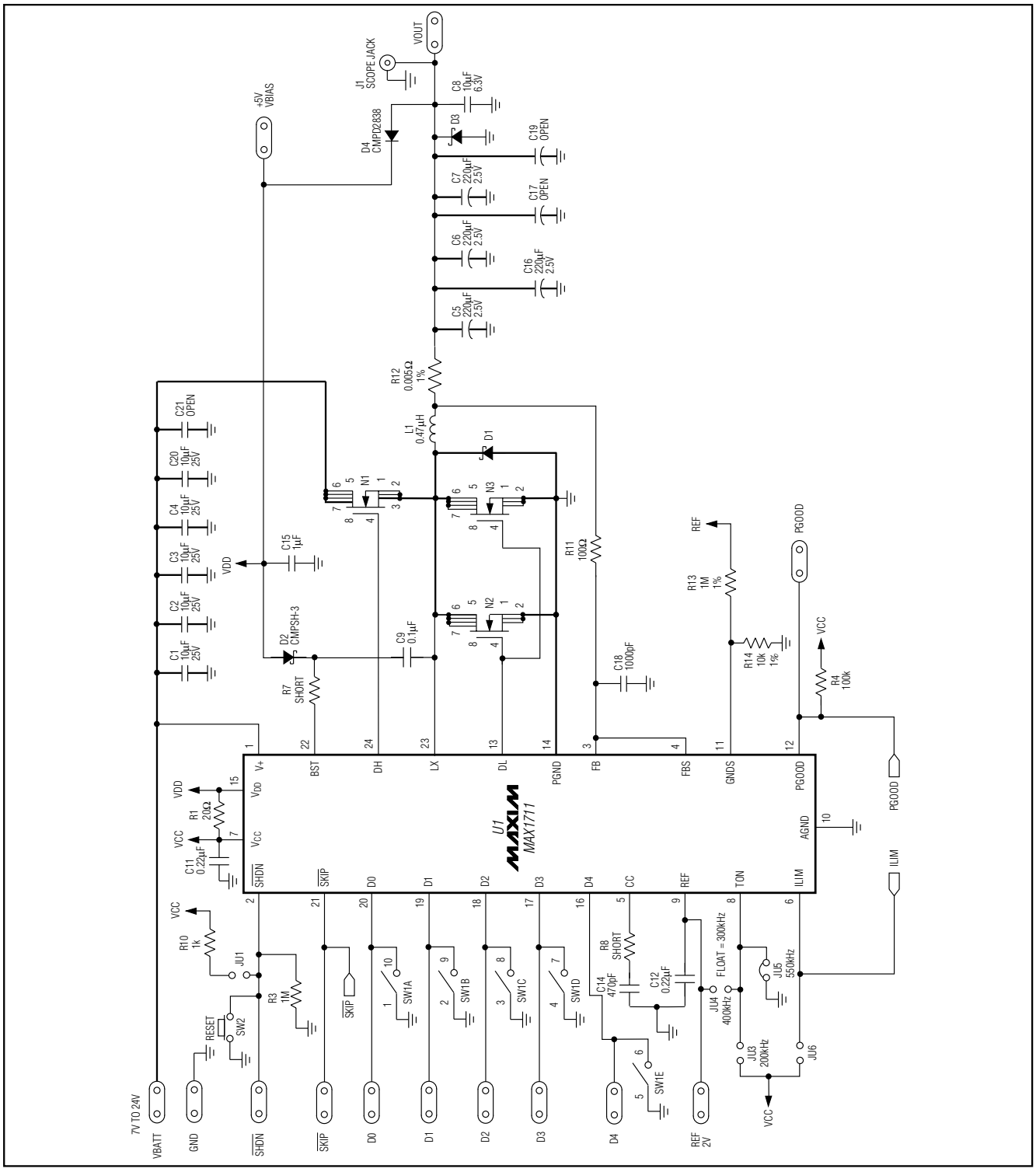

Figure 1. MAX1711 Voltage Positioning EV Kit Schematic

MAX1711 Voltage Positioning Evaluation Kit

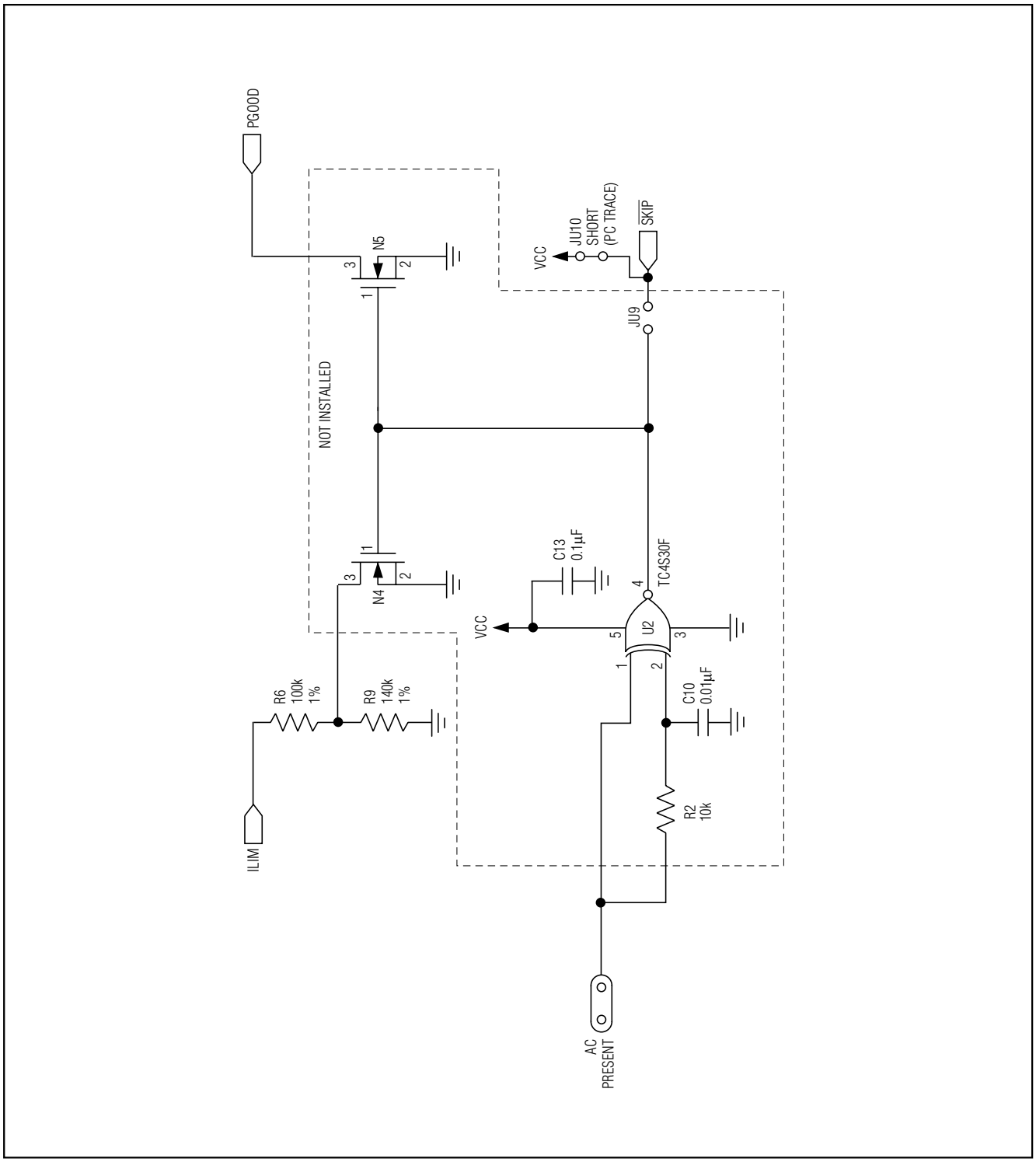

Figure 1. MAX1711 Voltage Positioning EV Kit Schematic (continued)

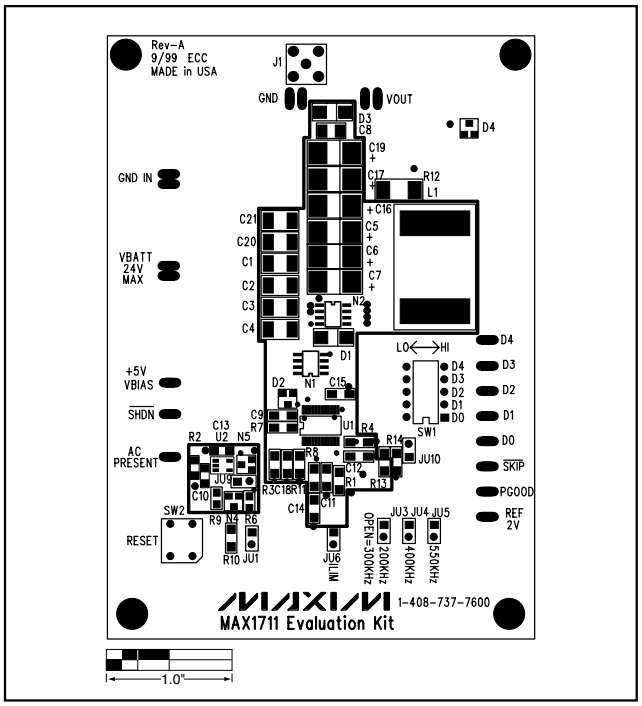

Figure 2. MAX1711 Voltage Positioning EV Kit Component Placement Guide—Component Side

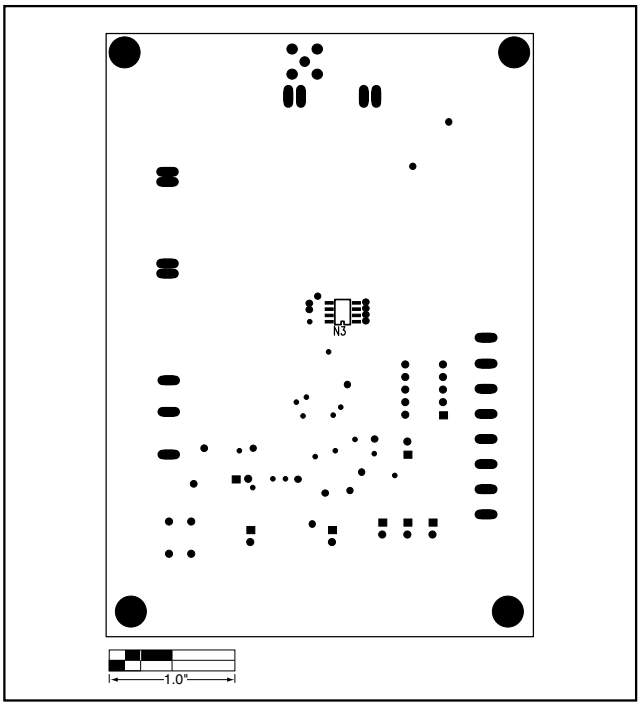

Figure 3. MAX1711 Voltage Positioning EV Kit Component Placement Guide—Solder Side

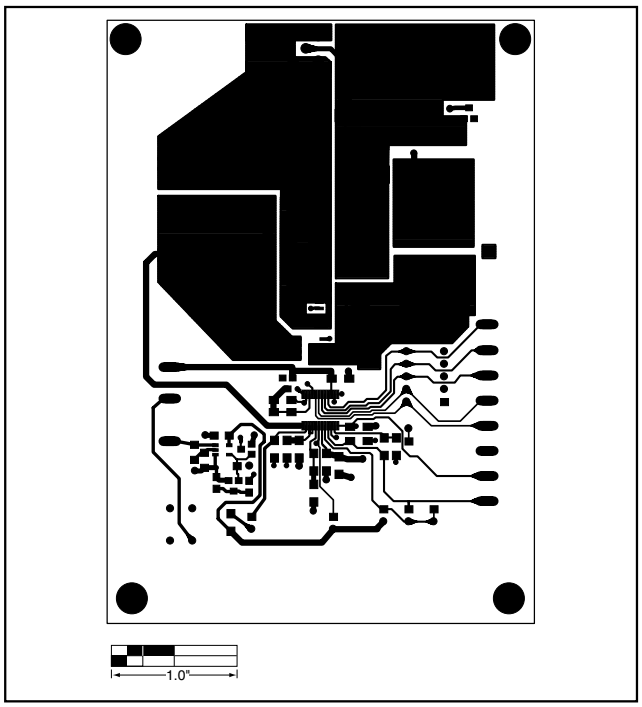

Figure 4. MAX1711 Voltage Positioning EV Kit PC Board Layout—Component Side

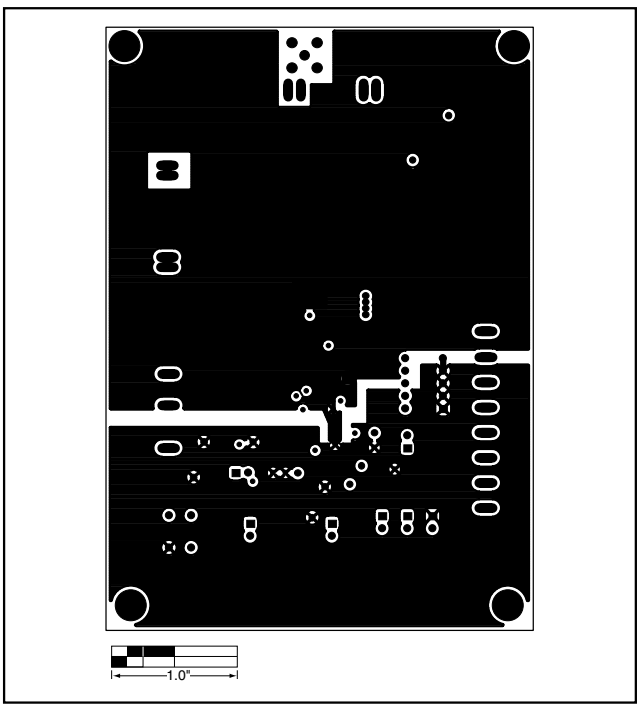

Figure 5. MAX1711 Voltage Positioning EV Kit PC Board Layout—Internal GND Plane (Layer 2)

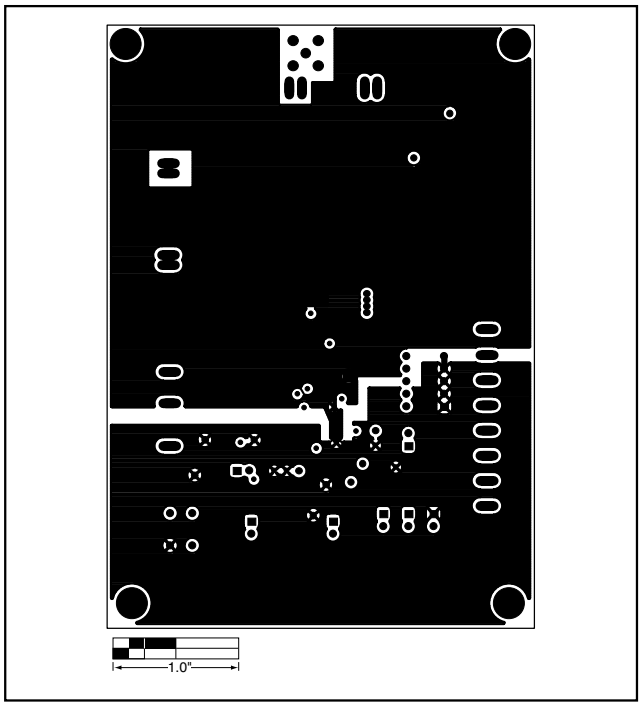

Figure 6. MAX1711 Voltage Positioning EV Kit PC Board Layout—Internal GND Plane (Layer 3)

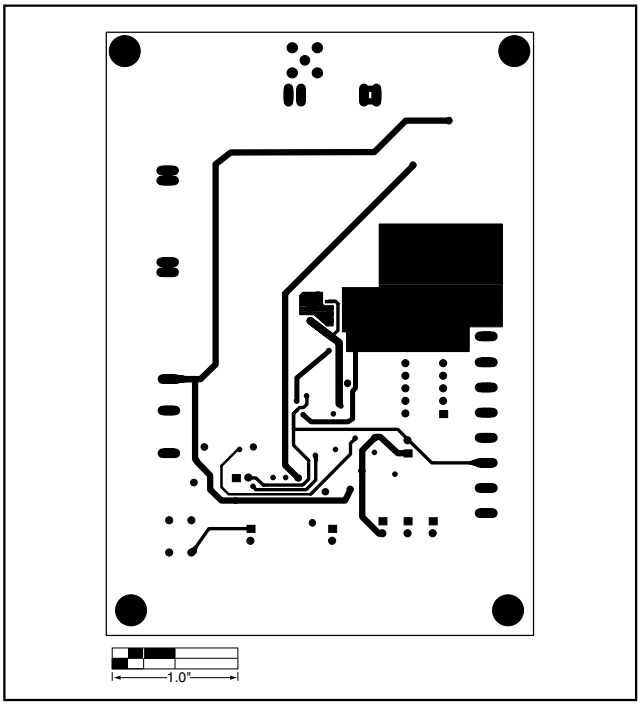

Figure 7. MAX1711 Voltage Positioning EV Kit PC Board Layout—Solder Side