



# DS1558 Watchdog Clock with NV RAM Control

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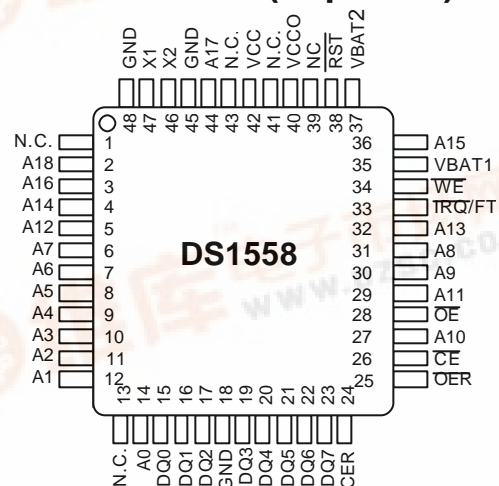
## FEATURES

- Integrated real-time clock (RTC), power-fail control circuit, and NV RAM controller
- Clock registers are accessed identically to the static RAM; these registers are resident in the 16 top RAM locations
- Century register
- Greater than 10 years of timekeeping and data retention in the absence of power with small lithium coin cell(s) and low-leakage SRAM
- Precision power-on reset
- Programmable watchdog timer and RTC alarm
- BCD-coded year, month, date, day, hours, minutes, and seconds with automatic leap-year compensation valid up to the year 2100
- Battery voltage-level indicator flag
- Power-fail write protection allows for  $\pm 10\%$   $V_{CC}$  power-supply tolerance
- Underwriters Laboratory (UL) recognized

## ORDERING INFORMATION

PART	PIN-PACKAGE	$V_{CC}$ (V)	TOP MARK
DS1558Y	48 TQFP	5	DS1558B
DS1558W	48 TQFP	3.3	DS1558D

## PIN ASSIGNMENT (Top View)



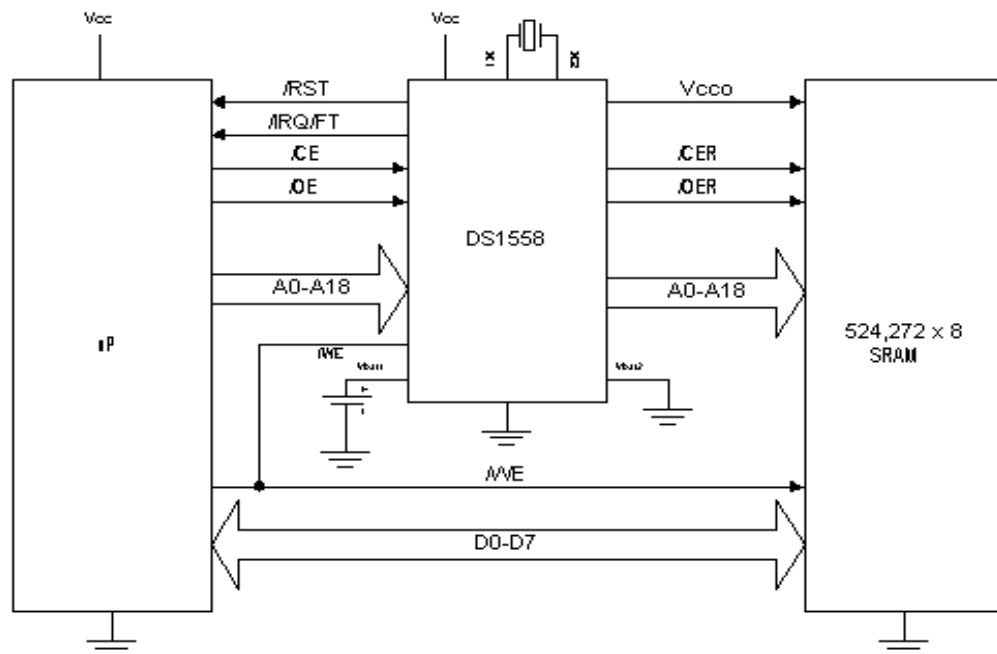
[48-Pin TQFP](#)

## Package Dimension Information

<http://www.maxim-ic.com/TechSupport/DallasPackInfo.htm>

## PIN DESCRIPTION

A0–A18	- Address Input
DQ0–DQ7	- Data Input/Outputs
$\overline{\text{IRQ}}/\text{FT}$	- Interrupt, Frequency-Test Output (Open Drain)
RST	- Power-On Reset Output (Open Drain)
$\overline{\text{CE}}$	- Chip-Enable Input
$\overline{\text{CER}}$	- Chip-Enable RAM
$\overline{\text{OE}}$	- Output-Enable Input
$\overline{\text{OER}}$	- Output-Enable RAM
$\overline{\text{WE}}$	- Write Enable
$V_{CC}$	- Power-Supply Input
$V_{CCO}$	- $V_{CC}$ Out to RAM
GND	- Ground
N.C.	- No Connection
X1, X2	- Crystal Connection
$V_{BAT1}$	- +3V Battery Input
$V_{BAT2}$	- +3V Battery Input



## DESCRIPTION

The DS1558 is a full function, year 2000-compliant (Y2KC), real-time clock/calendar with an RTC alarm, watchdog timer, power-on reset, battery monitor, and NV SRAM controller. User access to all registers within the DS1558 is accomplished with a byte-wide interface as shown in Figure 1. The RTC registers contain century, year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for day of month and leap year are made automatically.

The DS1558 maps the RTC registers into the SRAM address space and constantly monitors  $\overline{\text{A0}}\text{--}\overline{\text{A18}}$ . When any of the upper 16 address locations are accessed, the DS1558 inhibits  $\overline{\text{CER}}$  and  $\overline{\text{OER}}$  to the SRAM, and redirects reads and writes to the RTC registers within the DS1558. The DS1558 can be used with SRAMs up to 524,272 addresses. Smaller SRAMs can be used, provided that the unused upper address lines on the DS1558 are connected to  $\text{V}_{\text{CC}}$ .

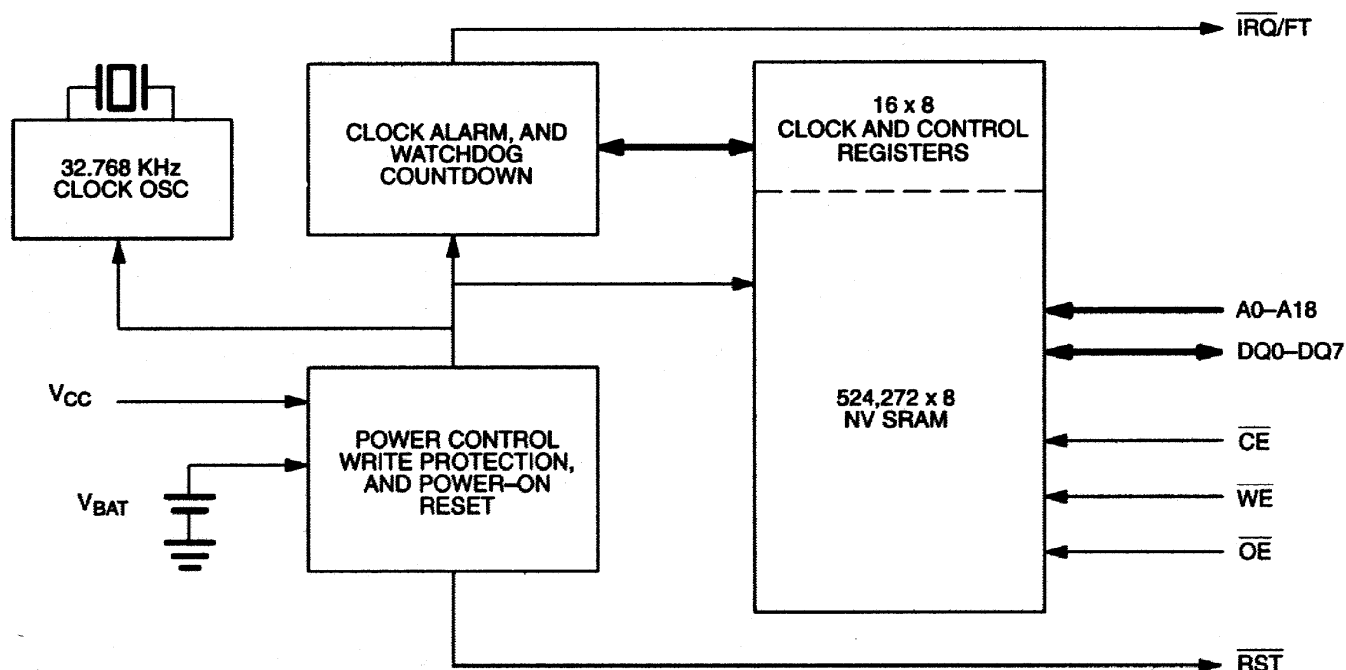
The RTC registers are double-buffered into an internal and external set. The user has direct access to the external set. Clock/calendar updates to the external set of registers can be disabled and enabled to allow the user to access static data. Assuming the internal oscillator is turned on, the internal set of registers is continuously updated; this occurs regardless of external register settings to guarantee that accurate RTC information is always maintained.

The DS1558 has interrupt ( $\overline{\text{IRQ}}/\text{FT}$ ) and reset ( $\overline{\text{RST}}$ ) outputs that can be used to control CPU activity. The  $\overline{\text{IRQ}}/\text{FT}$  interrupt output can be used to generate an external interrupt when the RTC register values match user-programmed alarm values. The interrupt is always available while the device is powered from the system supply, and it can be programmed to occur when in the battery-backed state to serve as a system wake-up. The  $\overline{\text{IRQ}}/\text{FT}$  output can also be used as a CPU watchdog timer. CPU activity is monitored and an interrupt or reset output are activated if the correct activity is not detected within

programmed limits. The DS1558 power-on reset can be used to detect a system power-down or failure and hold the CPU in a safe reset state until normal power returns and stabilizes; the  $\overline{\text{RST}}$  output is used for this function.

The DS1558 also contains its own power-fail circuitry, which automatically protects the data in the clock and SRAM against out-of-tolerance  $V_{\text{CCI}}$  conditions by inhibiting the  $\overline{\text{CE}}$  input when the  $V_{\text{CC}}$  supply enters an out-of-tolerance condition. When  $V_{\text{CCI}}$  goes below the level of  $V_{\text{BAT}}$ , the external battery is switched on to supply energy to the clock and the external SRAM. This feature provides a high degree of data security during unpredictable system operation brought on by low  $V_{\text{CC}}$  levels.

**Figure 1. BLOCK DIAGRAM**



**Note:** Any unused upper address pins must be connected to  $V_{\text{CC}}$  to properly address the RTC.

## SIGNAL DESCRIPTIONS

**A0-A18** – Address inputs for address decode. The DS1558 uses the address inputs to determine whether or not a read or write cycle should be directed to the attached SRAM or to the RTC registers.

**DQ0-DQ7** – Data input/output pins for the RTC registers.

$\overline{\text{IRQ/FT}}$  – This pin is used to output the alarm interrupt or the frequency test signal. It is open drain and requires an external pullup resistor.

$\overline{\text{RST}}$  – This pin is an output used to signal that  $V_{CC}$  is out of tolerance. On power-up,  $\overline{\text{RST}}$  is held low for a period of time to allow the system to stabilize. The RTC and SRAM are not accessible while  $\overline{\text{RST}}$  is active. This pin is open drain and requires an external pullup resistor.

$\overline{\text{CE}}$  – Chip-enable input that is used to access the RTC and the external SRAM.

$\overline{\text{CER}}$  – Chip-enable RAM output.  $\overline{\text{CE}}$  is passed through to  $\overline{\text{CER}}$ , with an added propagation delay. When the signals on A0–A18 match an RTC address,  $\overline{\text{CER}}$  is held high, disabling the SRAM. If  $\overline{\text{OE}}$  is also low, the RTC outputs data on DQ0–DQ7.

$\overline{\text{OE}}$  – Output-enable input that is used to access the RTC and the external SRAM.

$\overline{\text{OER}}$  – Output-enable RAM output.  $\overline{\text{OE}}$  is passed through to  $\overline{\text{OER}}$ , with an added propagation delay. When the signals on A0–A18 match an RTC address,  $\overline{\text{CER}}$  is held high, disabling the SRAM. If  $\overline{\text{CE}}$  is also low, the RTC outputs data on DQ0–DQ7.

$\overline{\text{WE}}$  – Write-enable input that is used to write data to the RTC registers.

$V_{CC}$ , **GND** – DC power is provided to the device on these pins.  $V_{CC}$  is the +5V input. When 5V (or 3.3V for the 3.3V version) is applied within normal limits, the device is fully accessible and data can be written and read. Reads and writes are inhibited when a 3V battery is connected to the device and  $V_{CC}$  is  $V_{TP}$ . However, the timekeeping function continues unaffected by the lower input voltage. As  $V_{CC}$  falls below  $V_{BAT}$ , the RAM and RTC are switched over to the external power supply (nominal 3.0V DC) at  $V_{BAT}$ .

$V_{CC0}$  –  $V_{CC}$  output to RAM. While  $V_{CC}$  is above  $V_{BAT}$ , the external SRAM is powered by  $V_{CC}$ . When  $V_{CC}$  is below the battery level, the SRAM is powered by one of the  $V_{BAT}$  inputs.

**N.C.** – No internal connection.

**X1, X2** – Connections for a standard 32.768kHz quartz crystal. The internal oscillator circuitry is designed for operation with a crystal having a specified load capacitance ( $C_L$ ) of 6pF. For more information about crystal selection and crystal layout considerations, refer to *Application Note 58* “Crystal Considerations with Dallas Real-Time Clocks.” The DS1558 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.

$V_{BAT1}$ ,  $V_{BAT2}$  – Battery inputs for any standard 3V lithium cell or other energy source. Battery voltage must be held between 2.5V and 3.7V for proper operation. UL recognized to ensure against reverse charging current when used with a lithium battery. If only one battery is used, it should be attached to  $V_{BAT1}$ , and  $V_{BAT2}$  should be grounded.

See “Conditions of Acceptability” at <http://www.maxim-ic.com/TechSupport/QA/ntrl.htm>.

**Table 1. OPERATING MODES**

$V_{CC}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ0–DQ7	MODE	POWER
$V_{CC} > V_{PF}$	$V_{IH}$	X	X	High-Z	Deselect	Standby
	$V_{IL}$	X	$V_{IL}$	$D_{IN}$	Write	Active
	$V_{IL}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$	Read	Active
	$V_{IL}$	$V_{IH}$	$V_{IH}$	High-Z	Read	Active
$V_{SO} < V_{CC} < V_{PF}$	X	X	X	High-Z	Deselect	CMOS Standby
$V_{CC} < V_{SO} < V_{PF}$	X	X	X	High-Z	Data Retention	Battery Current

**DATA READ MODE**

The DS1558 is in the read mode whenever  $\overline{CE}$  is low and  $\overline{WE}$  is high. The device architecture allows ripple-through access to any valid address location. Valid data is available at the DQ pins within  $t_{AA}$  after the last address input is stable, provided that  $\overline{CE}$  and  $\overline{OE}$  access times are satisfied. If  $\overline{CE}$  or  $\overline{OE}$  access times are not met, valid data is available at the latter of chip-enable access ( $t_{CEA}$ ) or at output-enable access time ( $t_{OEA}$ ). The state of the data input/output pins (DQ) is controlled by  $\overline{CE}$  and  $\overline{OE}$ . If the outputs are activated before  $t_{AA}$ , the data lines are driven to an intermediate state until  $t_{AA}$ . If the address inputs are changed while  $\overline{CE}$  and  $\overline{OE}$  remain valid, output data remains valid for output-data hold time ( $t_{OH}$ ), but then goes indeterminate until the next address access.

**DATA WRITE MODE**

The DS1558 is in the write mode whenever  $\overline{WE}$  and  $\overline{CE}$  are in their active state. The start of a write is referenced to the latter occurring transition of  $\overline{WE}$  or  $\overline{CE}$ . The addresses must be held valid throughout the cycle.  $\overline{CE}$  and  $\overline{WE}$  must return inactive for a minimum of  $t_{WR}$  prior to the initiation of a subsequent read or write cycle. Data in must be valid  $t_{DS}$  prior to the end of the write and remain valid for  $t_{DH}$  afterward. In a typical application, the  $\overline{OE}$  signal is high during a write cycle. However,  $\overline{OE}$  can be active provided that care is taken with the data bus to avoid bus contention. If  $\overline{OE}$  is low prior to  $\overline{WE}$  transitioning low, the data bus can become active with read data defined by the address inputs. A low transition on  $\overline{WE}$  then disables the outputs  $t_{WEZ}$  after  $\overline{WE}$  goes active.

**DATA RETENTION MODE**

The 5V device is fully accessible and data can be written and read only when  $V_{CC}$  is greater than  $V_{PF}$ . However, when  $V_{CC}$  is below the power-fail point  $V_{PF}$  (point at which write protection occurs), the internal clock registers and SRAM are blocked from any access. When  $V_{CC}$  falls below the battery switch point  $V_{SO}$  (battery supply level), device power is switched from the  $V_{CC}$  pin to the backup battery. RTC operation and SRAM data are maintained from the battery until  $V_{CC}$  is returned to nominal levels.

The 3.3V device is fully accessible and data can be written and read only when  $V_{CC}$  is greater than  $V_{PF}$ . When  $V_{CC}$  falls below  $V_{PF}$ , access to the device is inhibited. If  $V_{PF}$  is less than  $V_{SO}$ , the device power is switched from  $V_{CC}$  to the internal backup lithium battery when  $V_{CC}$  drops below  $V_{PF}$ . If  $V_{PF}$  is greater than  $V_{SO}$ , the device power is switched from  $V_{CC}$  to the internal backup lithium battery when  $V_{CC}$  drops below  $V_{SO}$ . RTC operation and SRAM data are maintained from the battery until  $V_{CC}$  is returned to nominal levels.

All control, data, and address signals must be powered down when  $V_{CC}$  is powered down.

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## BATTERY LONGIVITY

The battery lifetime is dependent on the RAM battery standby current and the DS1558 internal clock oscillator current. The total battery current is  $I_{OSC} + I_{CCO}$ . When  $V_{CC}$  is above  $V_{PF}$ ,  $I_{BAT}$  current is less than 50nA. The DS1558 has an internal circuit to prevent battery charging. No external protection components are required, and none should be used. The DS1558 has two battery pins that operate independently; the DS1558 selects the higher of the two inputs. If only one battery is used, the battery should be attached to  $V_{BAT1}$ , and  $V_{BAT2}$  should be grounded.

## INTERNAL BATTERY MONITOR

The DS1558 constantly monitors the battery voltage of the internal battery. The battery-low flag (BLF) bit of the flags register (B4 of 7FFF0h) is not writable and should always be a 0 when read. If a 1 is ever present, both battery inputs are below 1.8V and both the contents of the RTC and RAM are questionable.

## POWER-ON RESET

A temperature-compensated comparator circuit monitors the level of  $V_{CC}$ . When  $V_{CC}$  falls to the power-fail trip point, the  $\overline{RST}$  signal (open drain) is pulled low. When  $V_{CC}$  returns to nominal levels, the  $\overline{RST}$  signal continues to be pulled low for a period of 40ms to 200ms. The power-on reset function is independent of the RTC oscillator and thus is operational whether or not the oscillator is enabled.

## CLOCK OPERATIONS

Table 2 and the following paragraphs describe the operation of the RTC, alarm, and watchdog functions.

**Table 2. DS1558 REGISTER MAP**

ADDRESS	DATA								FUNCTION/RANGE	
	B <sub>7</sub>	B <sub>6</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		
7FFFFh	10 YEAR				YEAR				YEAR	00–99
7FFFEh	X	X	X	10 M	MONTH				MONTH	01–12
7FFFDh	X	X	10 DATE		DATE				DATE	01–31
7FFFCh	X	FT	X	X	X	DAY			DAY	01–07
7FFFBh	X	X	10 HOUR		HOUR				HOUR	00–23
7FFFAh	X	10 MINUTES			MINUTES				MINUTES	00–59
7FFF9h	$\overline{\text{OSC}}$	10 SECONDS			SECONDS				SECONDS	00–59
7FFF8h	W	R	10 CENTURY		CENTURY				CONTROL	00–39
7FFF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	WATCHDOG	—
7FFF6h	AE	Y	ABE	Y	Y	Y	Y	Y	INTERRUPTS	—
7FFF5h	AM4	Y	10 DATE		DATE				ALARM DATE	01–31
7FFF4h	AM3	Y	10 HOURS		HOURS				ALARM HOURS	00–23
7FFF3h	AM2	10 MINUTES			MINUTES				ALARM MINUTES	00–59
7FFF2h	AM1	10 SECONDS			SECONDS				ALARM SECONDS	00–59
7FFF1h	Y	Y	Y	Y	Y	Y	Y	Y	UNUSED	—
7FFF0h	WF	AF	0	BLF	0	0	0	0	FLAGS	—

X = Unused, Read/Writeable Under Write and Read Bit Control

FT = Frequency Test Bit

$\overline{\text{OSC}}$  = Oscillator Start/Stop Bit

W = Write Bit

R = Read Bit

WEN = Watchdog Enable Bit

BMB0–BMB4 = Watchdog Multiplier Bits

RB0–RB1 = Watchdog Resolution Bits

AE = Alarm Flag Enable

Y = Unused, Read/Writeable Without Write and Read Bit Control

ABE = Alarm in Backup-Battery Mode Enable

AM1–AM4 = Alarm Mask Bits

WF = Watchdog Flag

AF = Alarm Flag

0 = Reads as a 0 and Cannot Be Changed

BLF = Battery Low Flag

## CLOCK OSCILLATOR CONTROL

The oscillator can be turned off to minimize current drain from the battery. The  $\overline{\text{OSC}}$  bit is the MSB of the seconds register (B7 of 7FFF9h). Setting  $\overline{\text{OSC}}$  to a 1 stops the oscillator; setting to a 0 starts the oscillator. The initial state of  $\overline{\text{OSC}}$  is not guaranteed. When power is applied for the first time, the  $\overline{\text{OSC}}$  bit should be enabled. Oscillator operation and frequency can be verified by setting the FT bit and monitoring the  $\overline{\text{IRQ}}$ /FT pin for 512Hz.

## OSCILLATOR STARTUP TIME

Oscillator startup times are highly dependent upon crystal characteristics and layout. High ESR and excessive capacitive loads are the major contributors to long startup times. A circuit using a crystal with the recommended characteristics and following the recommended layout usually starts within 1 second.

## READING THE CLOCK

When reading the RTC data, it is recommended to halt updates to the external set of double-buffered RTC registers. This puts the external registers into a static state, allowing data to be read without register values changing during the read process. Normal updates to the internal registers continue while in this state. External updates are halted when a 1 is written into the read bit, B6 of the control register (7FFF8h). As long as a 1 remains in the control register read bit, updating is halted. After a halt is issued, the registers reflect the RTC count (day, date, and time) that was current at the moment the halt command is issued. Normal updates to the external set of registers resume within 1 second after the read bit is set to a 0 for a minimum of 500 $\mu$ s. The read bit must be a 0 for a minimum of 500 $\mu$ s to ensure the external registers are updated.

## SETTING THE CLOCK

The MSB bit, B7, of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the 7FFF8h–7FFFFh registers. After setting the write bit to a 1, RTC registers can be loaded with the desired RTC count (day, date, and time) in 24-hour BCD format. Setting the write bit to a 0 then transfers the values written to the internal RTC registers and allows normal operation to resume.

## CLOCK ACCURACY

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error is added by the crystal-frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit can result in the clock running fast. Refer to *Application Note 58* “Crystal Considerations with Dallas Real-Time Clocks” for detailed information.

## FREQUENCY TEST MODE

The DS1558 frequency test mode uses the open-drain  $\overline{\text{IRQ}}/\text{FT}$  output. With the oscillator running, the  $\overline{\text{IRQ}}/\text{FT}$  output toggles at 512Hz when the FT bit is a 1, the alarm-flag enable bit (AE) is a 0, and the watchdog-enable bit (WDS) is a 1, or the watchdog register is reset (register 7FFF7h = 00h). The  $\overline{\text{IRQ}}/\text{FT}$  output and the frequency test mode can be used as a measure of the actual frequency of the 32.768kHz RTC oscillator. The  $\overline{\text{IRQ}}/\text{FT}$  pin is an open-drain output that requires a pullup resistor for proper operation. The FT bit is cleared to a 0 on power-up.

## USING THE CLOCK ALARM

The alarm settings and control for the DS1558 reside within registers 7FFF2h–7FFF5h. Register 7FFF6h contains two alarm-enable bits: alarm enable (AE) and alarm in backup enable (ABE). The AE and ABE bits must be set as described below for the  $\overline{\text{IRQ}}/\text{FT}$  output to be activated for a matched alarm condition.

The alarm can be programmed to activate on a specific day of the month or repeat every day, hour, minute, or second. It can also be programmed to go off while the DS1558 is in the battery-backed state of operation to serve as a system wake-up. Alarm mask bits AM1–AM4 control the alarm mode. Table 3 shows the possible settings. Configurations not listed in the table default to the once-per-second mode to notify the user of an incorrect alarm setting.

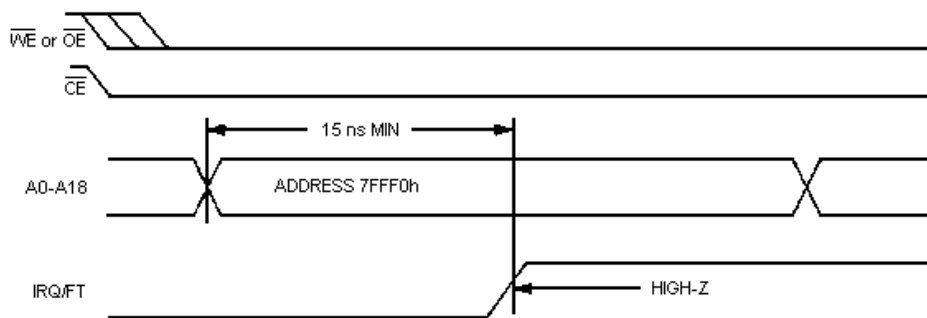
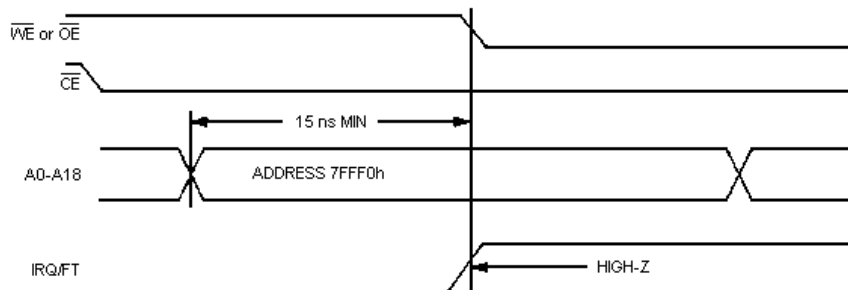


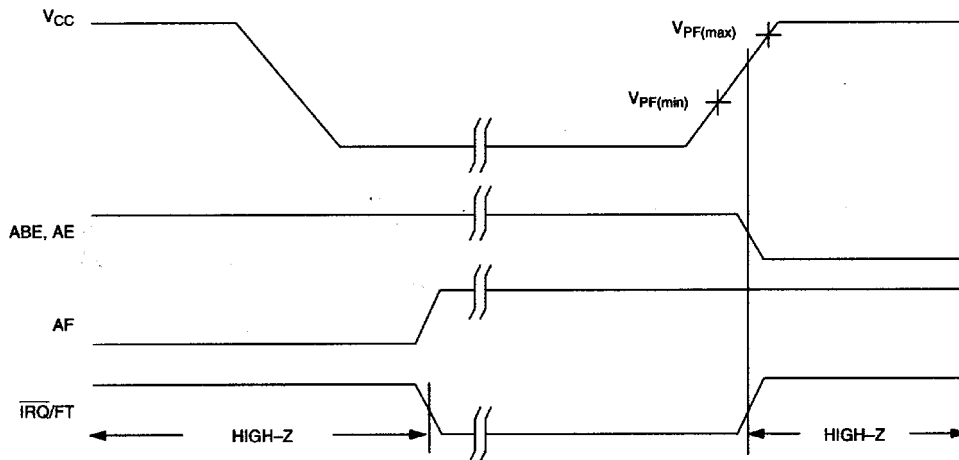
**Table 3. ALARM MASK BITS**

AM4	AM3	AM2	AM1	ALARM RATE
1	1	1	1	Once per second
1	1	1	0	When seconds match
1	1	0	0	When minutes and seconds match
1	0	0	0	When hours, minutes, and seconds match
0	0	0	0	When date, hours, minutes, and seconds match

When the RTC register values match alarm register settings, AF is set to a 1. If AE is also set to a 1, the alarm condition activates the  $\overline{\text{IRQ}}/\text{FT}$  pin. The  $\overline{\text{IRQ}}/\text{FT}$  signal is cleared by a read or write to the flags register (address 7FFF0h). When  $\overline{\text{CE}}$  is active, the  $\overline{\text{IRQ}}/\text{FT}$  signal can be cleared by having the address stable for as short as 15ns and either  $\overline{\text{OE}}$  or  $\overline{\text{WE}}$  active, but is not guaranteed to be cleared unless  $t_{\text{RC}}$  is fulfilled (Figure 2). Once the address has been selected for at least 15ns, the  $\overline{\text{IRQ}}/\text{FT}$  signal can be cleared immediately, but is not guaranteed to be cleared until  $t_{\text{RC}}$  is fulfilled (Figure 3). The alarm flag is also cleared by a read or write to the flags register, but the flag does not change states until the end of the read/write cycle and the  $\overline{\text{IRQ}}/\text{FT}$  signal has been cleared.

The  $\overline{\text{IRQ}}/\text{FT}$  pin can also be activated in the battery-backed mode. The  $\overline{\text{IRQ}}/\text{FT}$  goes low if an alarm occurs and both ABE and AE are set. The ABE and AE bits are cleared during the power-up transition, but an alarm generated during power-up sets AF. Therefore, the AF bit can be read after system power-up to determine if an alarm was generated during the power-up sequence. Figure 4 illustrates alarm timing during the backup-battery mode and power-up states.

**Figure 2. CLEARING IRQ WAVEFORMS ACTIVE****Figure 3. CLEARING IRQ WAVEFORMS**

**Figure 4. BACKUP MODE ALARM WAVEFORMS**

## USING THE WATCHDOG TIMER

The watchdog timer can be used to detect an out-of-control processor. The user programs the watchdog timer by setting the desired amount of timeout into the 8-bit watchdog register (address 7FFF7h). The five watchdog register bits BMB4–BMB0 store a binary multiplier and the two lower-order bits RB1–RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The watchdog timeout value is then determined by the multiplication of the 5-bit multiplier value with the 2-bit resolution value. (For example: writing 00001110 in the watchdog register = 3 x 1 second or 3 seconds.) If the processor does not reset the timer within the specified period, the watchdog flag (WF) is set and a processor interrupt is generated and stays active until either WF is read or the watchdog register (7FFF7h) is read or written.

The MSB of the watchdog register is the watchdog steering bit (WDS). When set to a 0, the watchdog activates the  $\overline{IRQ/FT}$  output when the watchdog times out. WDS should not be written to a 1, and should be initialized to a 0 if the watchdog function is enabled.

The watchdog timer resets when the processor performs a read or write of the watchdog register. The timeout period then starts over. The watchdog timer is disabled by writing a value of 00h to the watchdog register. The watchdog function is automatically disabled upon power-up and the watchdog register is cleared.

## POWER-ON DEFAULT STATES

Upon application of power to the device, the following register bits are set to a 0:

WDS = 0, BMB0–BMB4 = 0, RB0–RB1 = 0, AE = 0, and ABE = 0

All other bits are undefined.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage Range on Any Pin Relative to Ground

-0.3V to +6.0V

Storage Temperature Range

-55°C to +125°C

Soldering Temperature Range

See IPC/JEDEC J-STD-020A

*\*This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.*

**RECOMMENDED DC OPERATING CONDITIONS**(V<sub>CC</sub> = 3.3V ±10% or 5V ±10%, T<sub>A</sub> = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1 Voltage (All Inputs)						
V <sub>CC</sub> = +5V ±10%	V <sub>IH</sub>	2.2		V <sub>CC</sub> + 0.3V	V	1
V <sub>CC</sub> = +3.3V ±10%	V <sub>IH</sub>	2.0		V <sub>CC</sub> + 0.3V	V	1
Logic 0 Voltage (All Inputs)						
V <sub>CC</sub> = +5V ±10%	V <sub>IL</sub>	-0.3		+0.8		1
V <sub>CC</sub> = +3.3V ±10%	V <sub>IL</sub>	-0.3		+0.6		1
Battery Voltage	V <sub>BAT</sub>	2.5	3.3	3.7	V	

**DC ELECTRICAL CHARACTERISTICS**(V<sub>CC</sub> = +3.3V ±10% or +5V ±10%, T<sub>A</sub> = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Supply Current, +5V	I <sub>CC</sub>		6	25	mA	2, 3
Active Supply Current, +3.3V	I <sub>CC</sub>		4	15	mA	2, 3
TTL Standby, +5V ( $\overline{CE} = V_{IH}$ )	I <sub>CC1</sub>		3	6	mA	2, 3
TTL Standby, +3.3V ( $\overline{CE} = V_{IH}$ )	I <sub>CC1</sub>		2	6	mA	2, 3
CMOS Standby Current, +5V ( $\overline{CE} \geq V_{CC} - 0.2V$ )	I <sub>CC2</sub>		2	6	mA	2, 3
CMOS Standby Current, +3.3V ( $\overline{CE} \geq V_{CC} - 0.2V$ )	I <sub>CC2</sub>		1	2	mA	2, 3
Input Leakage Current (Any Input)	I <sub>IL</sub>	-1		+1	μA	
Output Leakage Current (Any Output)	I <sub>OL</sub>	-1		+1	μA	
Output Logic 1 Voltage (I <sub>OUT</sub> = -1.0mA)	V <sub>OH</sub>	2.4			V	1
Output Logic 0 Voltage  I <sub>OUT</sub> = 2.1mA, DQ0–DQ7 Outputs	V <sub>OL1</sub>			0.4	V	1
I <sub>OUT</sub> = 7.0mA, $\overline{IRQ}/FT$ and $\overline{RST}$ Outputs	V <sub>OL2</sub>			0.4	V	1, 5
Write Protection Voltage, +5V	V <sub>PF</sub>	4.25	4.37	4.50	V	1
Write Protection Voltage, +3.3V	V <sub>PF</sub>	2.80	2.88	2.97	V	1
Battery Switchover Voltage, +5V	V <sub>SO</sub>		V <sub>BAT</sub>		V	1
Battery Switchover Voltage, +3.3V	V <sub>SO</sub>		V <sub>PF</sub>		V	1, 4
Battery Current OSC On	I <sub>OSC</sub>		0.3	0.5	μA	6, 7
Battery Current OSC Off	I <sub>BACKUP</sub>			100	nA	7
Output Voltage I <sub>CCO</sub> = 70mA, +5V	V <sub>CC01</sub>	V <sub>CC1</sub> - 0.3			V	
Output Voltage I <sub>CCO</sub> = 40mA, +3.3V	V <sub>CC01</sub>	V <sub>CC1</sub> - 0.3			V	
Output Voltage I <sub>CCO</sub> = 10μA	V <sub>CC02</sub>	V <sub>BAT</sub> - 0.2	V <sub>BAT</sub> - 0.031		V	10

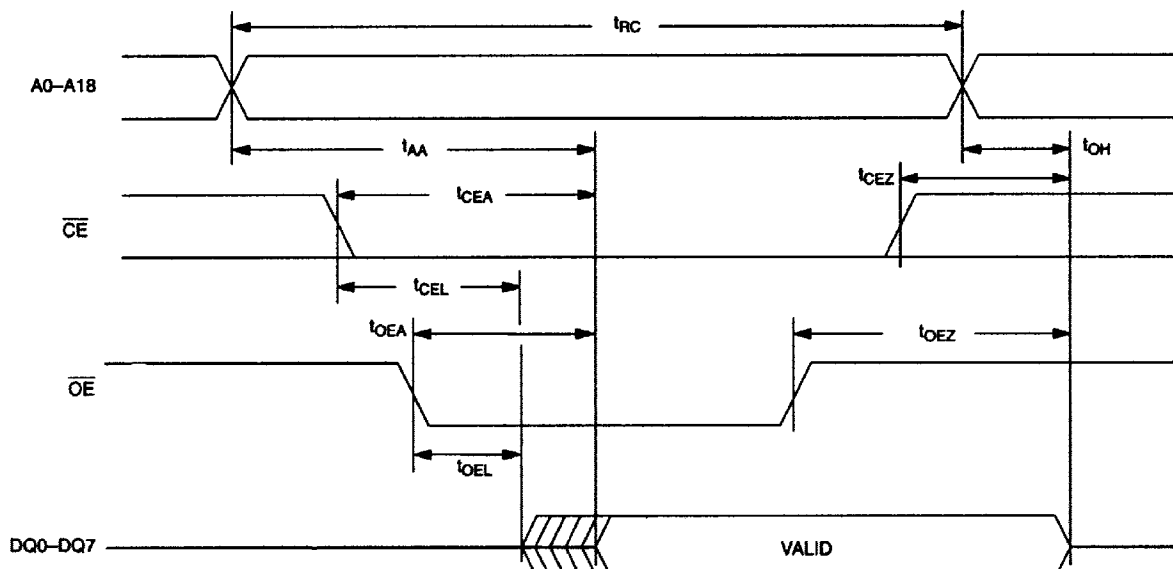
**CRYSTAL SPECIFICATIONS\***

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Nominal Frequency	F <sub>O</sub>		32.768		kHz	
Series Resistance	ESR			45	kΩ	
Load Capacitance	C <sub>L</sub>		6		pF	

\*The crystal, traces, and crystal input pins should be isolated from RF generating signals. Refer to Application Note 58 "Crystal Considerations for Dallas Real-Time Clocks" for additional specifications.

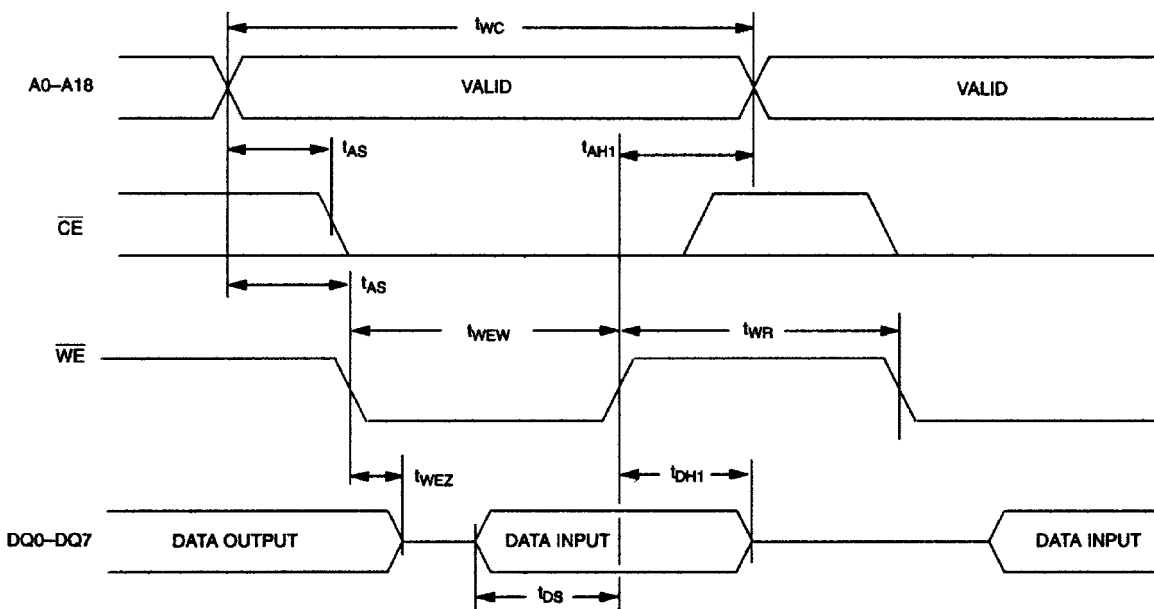
**READ CYCLE, AC CHARACTERISTICS**(V<sub>CC</sub> = +3.3V ±10% or +5V ±10%, T<sub>A</sub> = -40°C to +85°C)

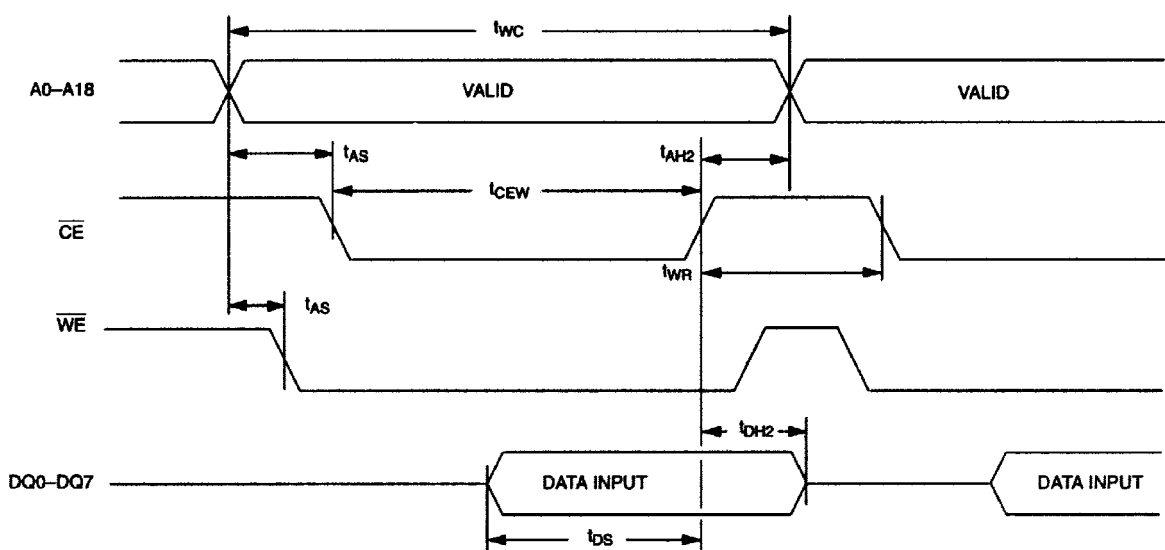
PARAMETER	SYMBOL	V <sub>CC</sub> = +5.5V ±10%		V <sub>CC</sub> = +3.3V ±10%		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Read Cycle Time	t <sub>RC</sub>	70		120		ns	
Address Access Time	t <sub>AA</sub>		70		120	ns	
$\overline{\text{CE}}$ to DQ Low-Z	t <sub>CEL</sub>	5		5		ns	
$\overline{\text{CE}}$ Access Time	t <sub>CEA</sub>		70		120	ns	
$\overline{\text{CE}}$ Data Off Time	t <sub>CEZ</sub>		25		40	ns	
$\overline{\text{OE}}$ to DQ Low-Z	t <sub>OEL</sub>	5		5		ns	
$\overline{\text{OE}}$ Access Time	t <sub>OEA</sub>		35		100	ns	
$\overline{\text{OE}}$ Data Off Time	t <sub>OEZ</sub>		25		35	ns	
Output Hold from Address	t <sub>OH</sub>	5		5		ns	
$\overline{\text{CE}}$ to $\overline{\text{CER}}$ Propagation Delay, +5V	t <sub>CEPD</sub>		15			ns	
$\overline{\text{OE}}$ to $\overline{\text{OER}}$ Propagation Delay, +5V	t <sub>OEPD</sub>		20			ns	
$\overline{\text{CE}}$ to $\overline{\text{CER}}$ Propagation Delay, +3.3V	t <sub>CEPD</sub>		30			ns	
$\overline{\text{OE}}$ to $\overline{\text{OER}}$ Propagation Delay, +3.3V	t <sub>OEPD</sub>		40			ns	

**Figure 5. READ CYCLE TIMING DIAGRAM**

**WRITE CYCLE, AC CHARACTERISTICS**(V<sub>CC</sub> = +3.3V ±10% or +5V ±10%, T<sub>A</sub> = -40°C to +85°C)

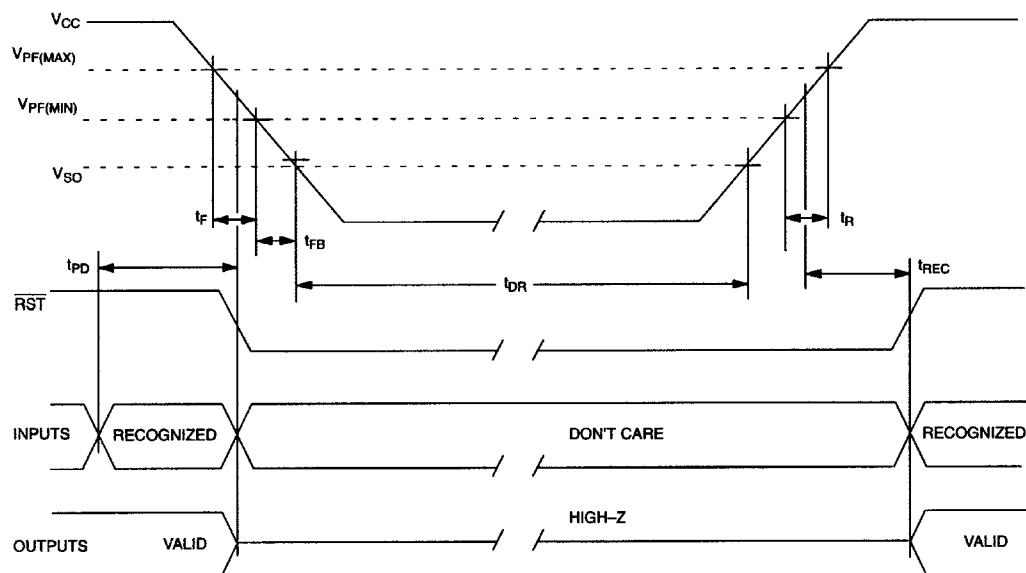
PARAMETER	SYMBOL	V <sub>CC</sub> = +5.0V ±10%		V <sub>CC</sub> = +3.3V ±10%		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Write Cycle Time	t <sub>WC</sub>	70		120		ns	
Address Access Time	t <sub>AS</sub>	0		0		ns	
$\overline{\text{WE}}$ Pulse Width	t <sub>WEW</sub>	50		100		ns	
$\overline{\text{CE}}$ Pulse Width	t <sub>CEW</sub>	60		110		ns	
Data Setup Time	t <sub>DS</sub>	30		80		ns	
Data Hold Time	t <sub>DH1</sub>	5		5		ns	8
Data Hold Time	t <sub>DH2</sub>	5		5		ns	9
Address Hold Time	t <sub>AH1</sub>	5		0		ns	8
Address Hold Time	t <sub>AH2</sub>	5		5		ns	9
$\overline{\text{WE}}$ Data Off Time	t <sub>WEZ</sub>		25		40	ns	
Write Recovery Time	t <sub>WR</sub>	5		10		ns	

**Figure 6. WRITE CYCLE TIMING, WRITE-ENABLE CONTROLLED**

**Figure 7. WRITE CYCLE TIMING, CHIP-ENABLE CONTROLLED**

**POWER-UP/DOWN CHARACTERISTICS** ( $V_{CC} = +5V \pm 10\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

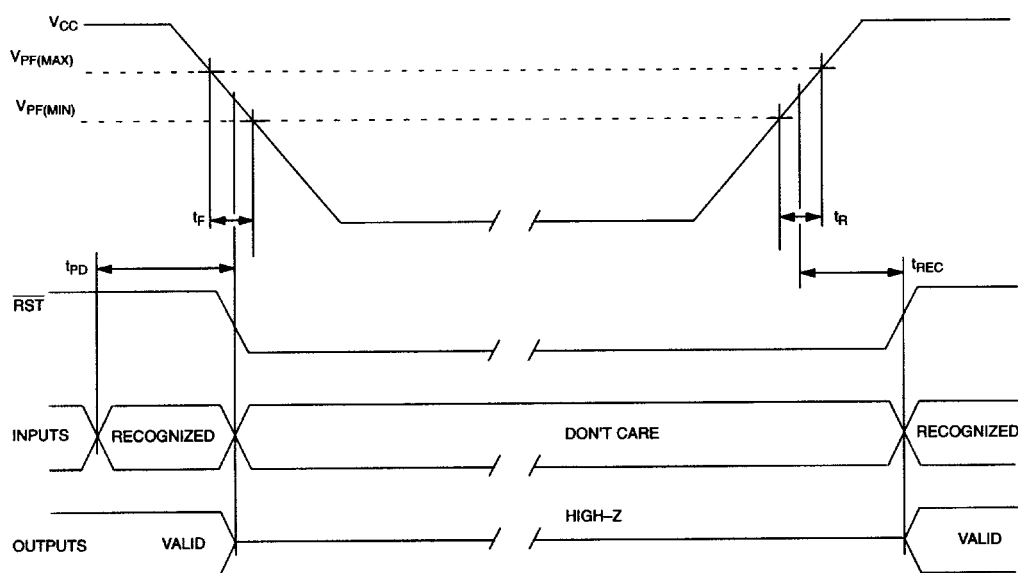
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at $V_{IH}$ , Before Power-Down	$t_{PD}$	0			$\mu\text{s}$	
$V_{CC}$ Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	$t_F$	300			$\mu\text{s}$	
$V_{CC}$ Fall Time: $V_{PF(MIN)}$ to $V_{SO}$	$t_{FB}$	10			$\mu\text{s}$	
$V_{CC}$ Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	$t_R$	0			$\mu\text{s}$	
$V_{PF}$ to $\overline{RST}$ High	$t_{REC}$	40		200	ms	

**Figure 8. +5V POWER-UP/DOWN WAVEFORM TIMING**




**POWER-UP/DOWN CHARACTERISTICS** ( $V_{CC} = +3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
$\overline{CE}$ or $\overline{WE}$ at $V_{IH}$ , Before Power-Down	$t_{PD}$	0			$\mu s$	
$V_{CC}$ Fall Time: $V_{PF(MAX)}$ to $V_{PF(MIN)}$	$t_F$	300			$\mu s$	
$V_{CC}$ Rise Time: $V_{PF(MIN)}$ to $V_{PF(MAX)}$	$t_R$	0			$\mu s$	
$V_{PF}$ to $\overline{RST}$ High	$t_{REC}$	40		200	ms	

**Figure 9. +3.3V POWER-UP/DOWN WAVEFORM TIMING**

**CAPACITANCE**
 $(T_A = +25^{\circ}C)$ 

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Capacitance On All Input Pins	$C_{IN}$			7	pF	1
Capacitance On $\overline{IRQ}/\overline{FT}$ , $\overline{RST}$ , and DQ Pins	$C_{IO}$			10	pF	1

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**AC TEST CONDITIONS**

Output Load: 25pF

Input Pulse Levels: 0V to +3V

Timing Measurement Reference Levels:

Input: +1.5V

Output: +1.5V

Input Pulse Rise and Fall Times: 5ns

**NOTES:**

- 1) Voltage referenced to ground.
- 2) Typical values are at +25°C and nominal supplies.
- 3) Outputs are open.
- 4) Battery switchover occurs at the lower of either the battery voltage or  $V_{PF}$ .
- 5) The  $\overline{IRQ}/FT$  and  $\overline{RST}$  outputs are open drain.
- 6) Using the recommended crystal on X1 and X2.
- 7)  $V_{CCO}$ ,  $\overline{CER}$ , and  $\overline{OER}$  pins open.
- 8)  $t_{AH1}$ ,  $t_{DH1}$  are measured from  $\overline{WE}$  going high.
- 9)  $t_{AH2}$ ,  $t_{DH2}$  are measured from  $\overline{CE}$  going high.
- 10) Typical measured with  $V_{BAT}$  at 3.0V. Typical with  $I_{CCO} = 100\mu A$  and  $V_{BAT} = 3.0V$  is  $V_{BAT} - 0.322$ .