FAIRCHILD SEMICONDUCTOR™

February 1984
Revised February 2002

MM74HCT05
Hex Inverter (Open Drain)

General Description

The MM74HCT05 is a logic function fabricated by using advanced silicon-gate CMOS technology, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. The device is also input and output characteristic and pinout compatible with standard DM74LS logic families. The MM74HCT05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

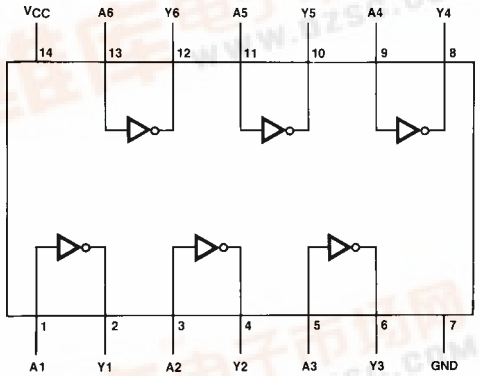
- Open drain for wire-NOR function
- LS-TTL pinout and threshold compatible
- Fanout of 10 LS-TTL loads
- Typical propagation delays:
  t_{PZL} (with 1 kΩ resistor) 10 ns
  t_{PLZ} (with 1 kΩ resistor) 8 ns

Ordering Code:

Order Number	Package Number	Package Description
MM74HCT05M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HCT05SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT05MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT05N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

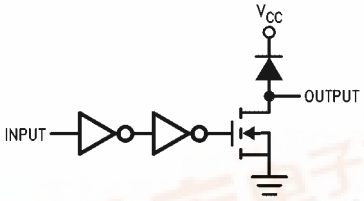
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

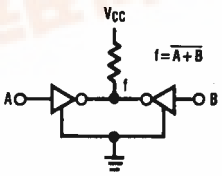


Top View

Logic Diagram



Typical Application



Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to +7.0V
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	+ 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input Voltage (V_{IN})	0	V_{CC}	V
Output Voltage (V_{OUT})	0	5.5	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics

(V_{CC} = 5V ± 10%,unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	T_A = −40 to 85°C		Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	V
V_{OL}	Maximum LOW Level Voltage	V_{IN} = V_{IH}				V
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		± 0.1	± 1.0	μA
I_{LKG}	Maximum HIGH Level Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC}		0.5	5.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		2.0	20	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.3	0.4	mA
I_{OHZ}	Off State Current	V_{CC} = 4.5 - 5.5, V_O = 5.5			10	μA

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PZL}	Maximum Propagation Delay	R_L = 1 kΩ	8	15	ns
t_{PLZ}	Maximum Propagation Delay	R_L = 1 kΩ	9	16	ns

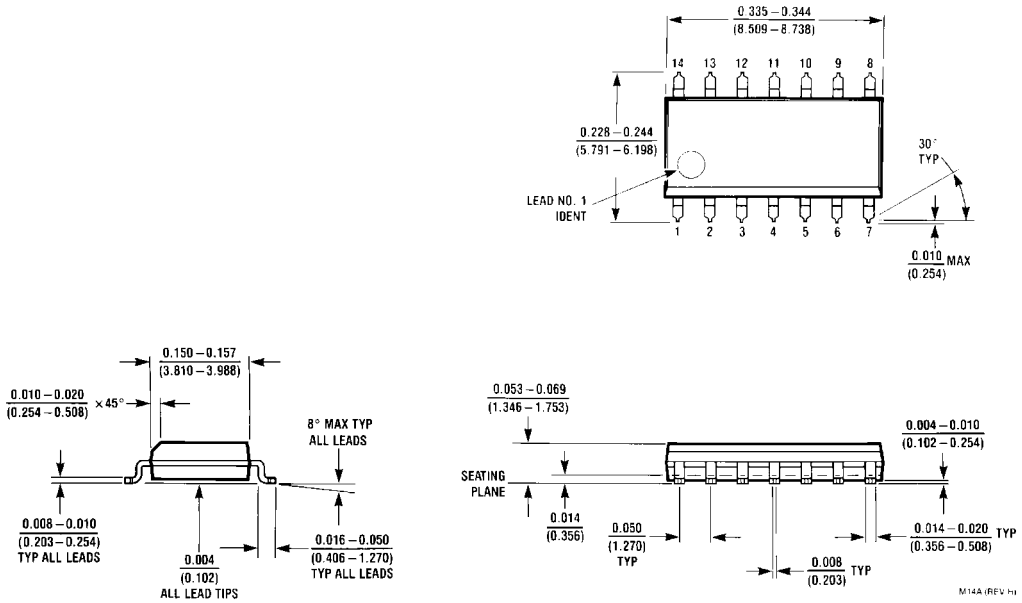
AC Electrical Characteristics

V_{CC} = 5V, ± 10%, C_L = 50pF, $t_r = t_f$ = 6 ns unless otherwise specified.

Symbol	Parameter	Conditions	T_A=25°C	T_A = −40 to 85°C		Units
			Typ	Guaranteed Limits		
t_{PZL}	Maximum Propagation Delay	R_L = 1kΩ	10	22	28	ns
t_{PLZ}	Maximum Propagation Delay	R_L = 1 kΩ	12	20	25	ns
t_{THL}	Maximum Output Fall Time		10	15	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) R_L = ∞		20		pF
C_{IN}	Maximum Input Capacitance			5	10	pF

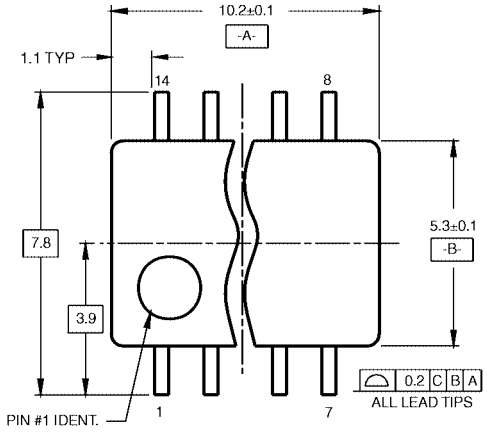
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

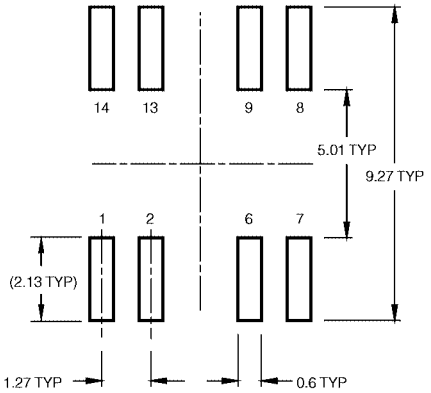
Physical Dimensions inches (millimeters) unless otherwise noted



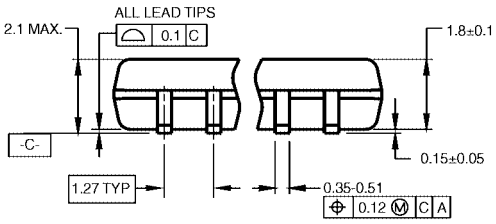
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

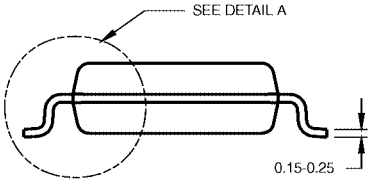


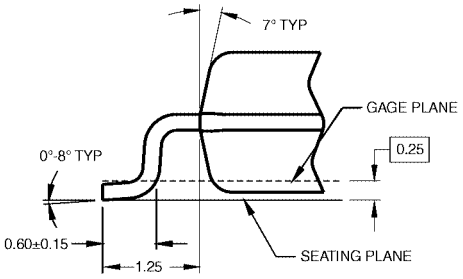


LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS





DETAIL A

NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

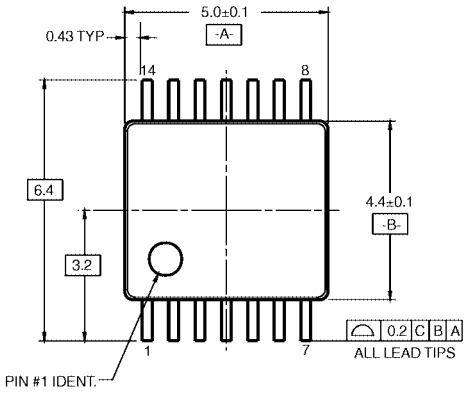
B. DIMENSIONS ARE IN MILLIMETERS.

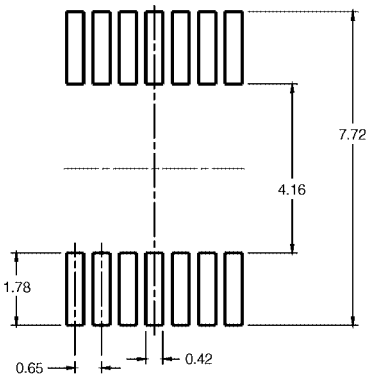
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

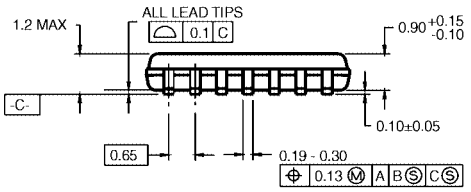
14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

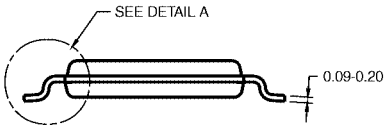
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

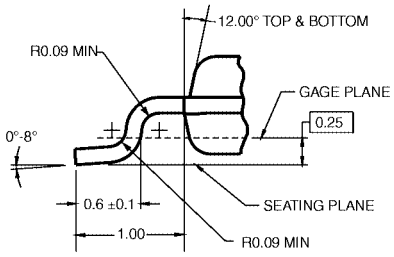




LAND PATTERN RECOMMENDATION







DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

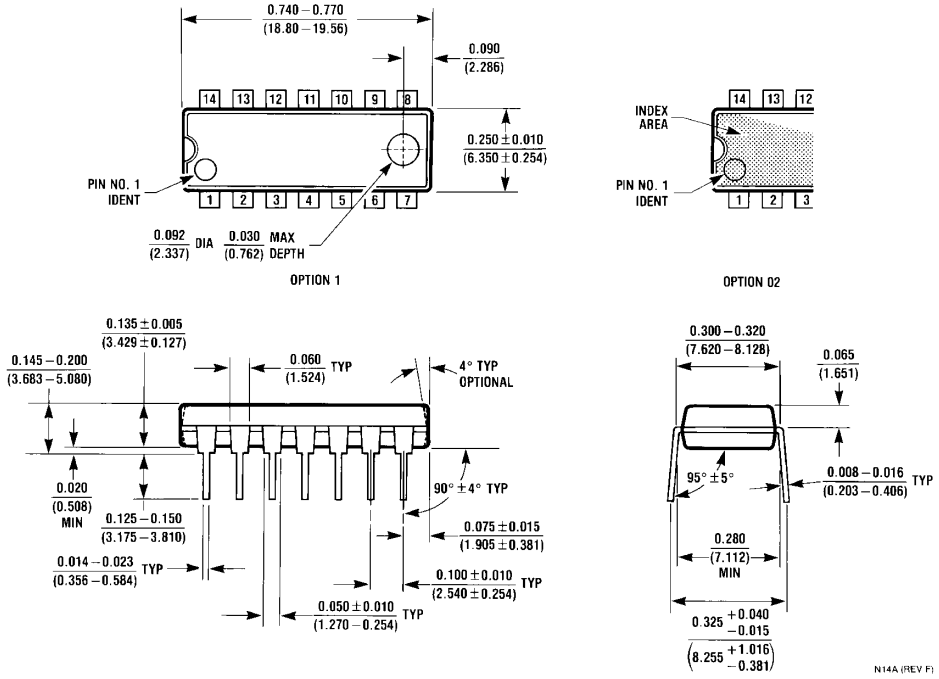
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A