CMOS 8-Bit Microcontroller

TMP86P202P/M, TMP86P203P/M

The TMP86P202/203 are high-speed and high-performance 8-bit single chip microcomputers with small package. The MCU contain CPU core, ROM, RAM, multirole timer counter, and 8-bit AD converter, on a chip.

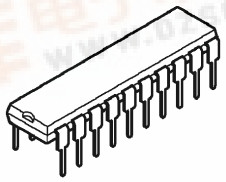
Product No.	ROM	RAM	Package	Resonator
TMP86P202P	2 K × 8 bits	128 × 8 bits	P-DIP20-300-2.54D	Ceramic, Crystal resonator
TMP86P202M*			P-SOP20-300-1.27	
TMP86P203P*			P-DIP20-300-2.54D	RC resonator
TMP86P203M*			P-SOP20-300-1.27	

*: Under development

Features

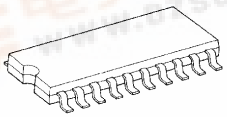
- 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: 0.50 μs (fc = 8 MHz)
- 132 types and 731 basic instructions
- Interrupt sources: 11 factors (External: 3, Internal: 8)
- Input/Output ports: 14 pins
  - High-Current Output 2 pins (Typ. 20mA)
- 8-bit timer/counter: 2 ch
  - Timer, PDO output, Event counter, PWM output, PPG modes
  - Possible to use as 16-bit timer by connecting each other
- Time Base Timer
- Divider output function
- Watchdog Timer
  - Interrupt source/Internal Reset (programmable)
- 8-bit successive approximate type AD converter
  - Analog input: 4 ch

P-DIP20-300-2.54D



TMP86P202P
TMP86P203P*

P-SOP20-300-1.27



TMP86P202M*
TMP86P203M*

*: Under development

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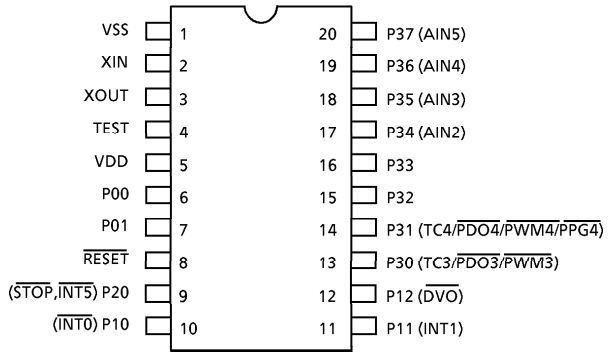
- Power saving operating modes (3 modes)
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.
  - IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer. Release by INTTBT interrupt.
  - IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock. Release by interrupts.
- Wide operating voltage: 3.3 to 5.5 V at 8 MHz (Ceramic resonator, Crystal resonator)
  4.5 to 5.5 V at 2.5 MHz (RC resonator) (Under development)

Note: AD conversion characteristics are guaranteed with limited supply voltage range (4.5 V to 5.5 V). If supply voltage is less than 4.5 V then AD conversion accuracy can not be guaranteed.

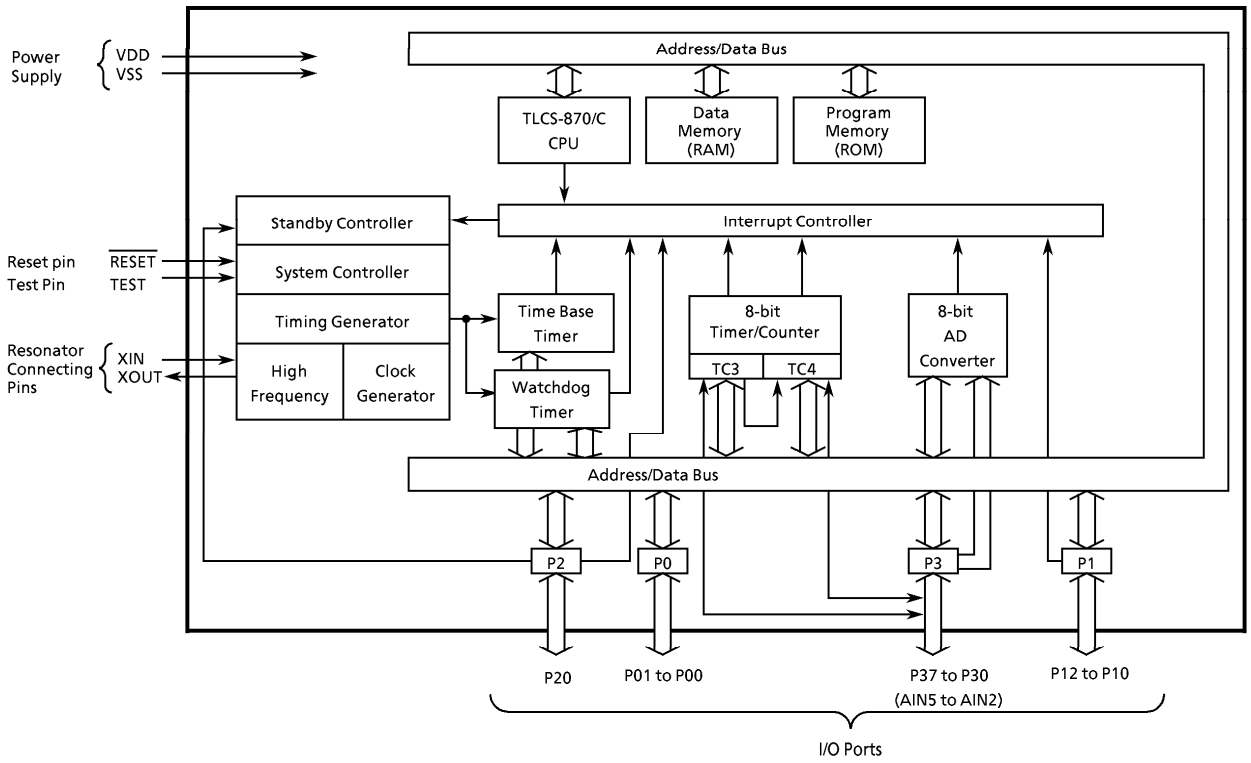
Pin Assignments (Top View)

P-DIP20-300-2.54D (for TMP86P202P and TMP86P203P*)
P-SOP20-300-1.27 (for TMP86P202M* and TMP86P203M*)

*: Under development



Block Diagram



Pin Function

The TMP86P202/203 has two modes: MCU and PROM.

(1) MCU mode

Pin Name	Input/Output	Function	
P01	I/O	2-bit programmable input/output ports. Each bit of these ports can be individually configured as an input or output under software control. Nch open-drain output function.	
P00	I/O		
P12 ($\overline{DVO}$)	I/O (Output)	3-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or output under software control. When used as function, the latch must be set to 1.	Divider output
P11 (INT1)	I/O (Input)		External interrupt input 1
P10 ($\overline{INT0}$)	I/O (Input)		External interrupt input 0
P20 ($\overline{INT5}$, $\overline{STOP}$)	I/O (Input)	1-bit programmable input/output ports. When used as input port and function, the latch must be set to 1.	External interrupt input 5 or STOP mode release signal input
P37 (AIN5)	I/O (Input)	8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or output under software control. When used as function and analog inputted latch must be set to 1.	AD converter analog input
P36 (AIN4)	I/O (Input)		
P35 (AIN3)	I/O (Input)		
P34 (AIN2)	I/O (Input)		
P33	I/O		
P32	I/O		
P31 (TC4, $\overline{PDO4}$, $\overline{PWM4}$, $\overline{PPG4}$)	I/O (I/O)		Timer/Counter 4 input, $\overline{PDO}$, $\overline{PWM}$, $\overline{PPG}$ output
P30 (TC3, $\overline{PDO3}$, $\overline{PWM3}$)	I/O (I/O)		Timer/Counter 3 input, $\overline{PDO}$, $\overline{PWM}$ output
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	Input	RESET signal input	
TEST	Input	TEST pin for out-going test. Be fixed to low.	
VDD, VSS	Power Supply	+ 5 V, 0 (GND)	

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin name (MCU mode)
A16	Input	Program memory address inputs	XOUT
A15 to A8			P37 to P30
A7 to A0			P37 to P30
D7 to D0	I/O	Program memory data input/outputs	P37 to P30
$\overline{CE}$	Input	Chip enable signal input	P00
$\overline{OE}$		Output enable signal input	P20
$\overline{PGM}$		Program mode signal input	P01
DIDS		PROM mode control signal	P12
VPP	Power supply	+ 12.75 V/5 V (Program supply voltage)	TEST
VCC		+ 6.25 V/5 V	VDD
GND		0 V	VSS
P11	Input	PROM mode setting pins. Be fixed at high level.	
$\overline{RESET}$		PROM mode setting pins. Be fixed at low level.	
CLK		Input a clock from the outside.	XIN

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and watchdog timer.

This section provides a description of the CPU core, the program memory, the data memory, and the reset circuit.

1.1 Memory Address Map

The TMP86P202/203 memory consist of 3 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86P202/203 memory address map. The general-purpose register banks are not assigned to the RAM address space.

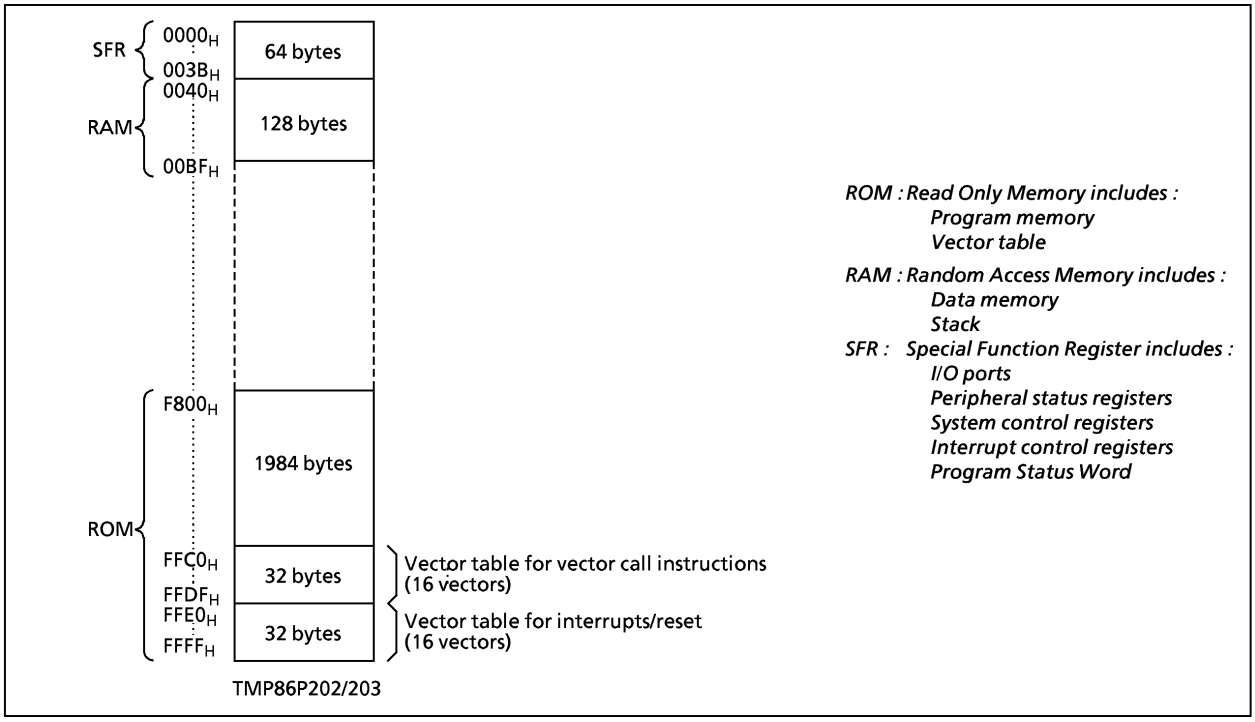


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86P202/203 has a 2 K×8 bits (address $F800_H$ to $FFFF_H$), of program memory. However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address Trap).

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Program voltage	V_{PP}	TEST/V_{PP}	– 0.3 to 13.0	
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	
Output Voltage	V_{OUT1}	$\overline{RESET}$, Tri-state Port	– 0.3 to V_{DD} + 0.3	
	V_{OUT2}	P20, Sink Open Drain Port	– 0.3 to 5.5	
Output Current (Per 1 pin)	I_{OUT1} I_{OH}	P0, P1, P3 Port	– 1.8	mA
	I_{OUT2} I_{OL}	P1, P2, P3 Port	12	
	I_{OUT3} I_{OL}	P0 Port	30	
Output Current (Total)	Σ I_{OUT1}	P0, P1, P3 Port	– 12	
	Σ I_{OUT2}	P1, P2, P3 Port	40	
	Σ I_{OUT3}	P0 Port	60	
Power Dissipation [T_{opr} = 85°C]	PD	DIP	250	mW
		SOP	180	
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 150	
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Max	Unit
Supply Voltage	V_{DD}		NORMAL1 mode	3.3 (TMP86P202) 4.5 (TMP86P203)	5.5	V
			IDLE0, 1 mode			
			STOP mode	2.0		
Input high Level	V_{IH1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.70$	V_{DD}	
	V_{IH2}	Hysteresis input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.90$		
Input low Level	V_{IL1}	Except Hysteresis input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.30$	
	V_{IL2}	Hysteresis input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 3.3 to 5.5 V (TMP86P202)	1.0	8.0	MHz
			V_{DD} = 4.5 to 5.5 V (TMP86P203)*	0.4	2.5	

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: AD conversion characteristics are guaranteed with limited supply voltage range (4.5 V to 5.5 V). If supply voltage is less than 4.5 V then AD conversion accuracy can not be guaranteed.

*: Under development

DC Standard

DC Characteristics (V_{SS} = 0 V, Topr = – 40 to 85°C)

Parameter	Symbol	Pins	Condition	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V/0 V	–	–	± 2	μA
	I_{IN2}	Sink Open Drain, Tri-state Port					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Resistance	R_{IN2}	$\overline{RESET}$ Pull-Up		100	220	450	kΩ
Output Leakage Current	I_{LO}	Sink Open Drain, Tri-state Port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V/0 V	–	–	± 2	μA
Output High Voltage	V_{OH}	P0, P1, P3 Port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA	4.1	–	–	V
Output Low Voltage	V_{OL}	P1, P2, P3 Port	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	–	–	0.4	
Output Low Current	I_{OL}	Middle Current Port (except XOUT, P0)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	8	–	mA
Output Low Current	I_{OL}	High Current Port (P0 Port)	V_{DD} = 4.5 V, V_{OL} = 1.0 V	–	20	–	
Supply Current in NORMAL 1 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3/0.2 V fc = 8.0 MHz	–	3.0	5.5	
Supply Current in IDLE 0, 1 mode				–	1.9	4.0	
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V/0.2 V	–	0.5	10.0	μA

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V
Note 2: Input current (I_{IN1}, I_{IN3}); The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} does not include I_{REF} current.

AD Conversion Characteristics

(V_{SS} = 0.0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Input Voltage	V_{AIN}		V_{SS}	–	V_{DD}	V
Power Supply Current of Analog Reference Voltage	I_{REF}	V_{DD} = 5.5 V V_{SS} = 0.0 V	–	0.6	1.0	mA
Non linearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V	–	–	± 2	LSB
Zero Point Error			–	–	± 2	
Full Scale Error			–	–	± 2	
Total Error			–	–	± 4	

Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
Note 2: Conversion time is different in recommended value by power supply voltage. About conversion time, please refer to "2.7.2 Register Configuration".
Note 3: Please use input voltage to AIN input Pin in limit of V_{DD} - V_{SS}. When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
Note 4: The relevant pin for I_{REF} is V_{DD}, so that the current flowing into V_{DD} is the power supply current I_{DD} + I_{REF}.
Note 5: AD conversion characteristics are guaranteed with limited supply voltage range (4.5 V to 5.5 V). If supply voltage is less than 4.5 V then AD conversion accuracy can not be guaranteed.

AC Characteristics

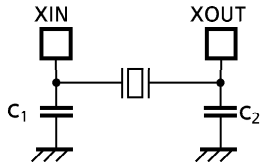
(V_{SS} = 0 V, V_{DD} = 3.3 to 5.5 V, Topr = – 40 to 85°C)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	NORMAL 1 mode	0.5	–	8	μs
		IDLE 0, 1 mode				
High Level Clock Pulse Width	twcH	For external clock operation (XIN input) fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	twcL					

Recommended Oscillation Conditions

TMP86P202 (V_{SS} = 0 V, V_{DD} = 3.3 to 5.5 V, T_{opr} = − 40 to 85°C)

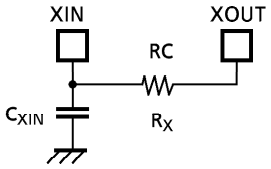
Parameter	Resonator	Oscillating Frequency	Recommended Resonator		Recommended Constant	
					C_1	C_2
High-frequency oscillation	Ceramic resonator	8 MHz	MURATA	CSA8.00MTZ	30 pF	30 pF
				CST8.00MTW	30 pF (built-in)	30 pF (built-in)
		4.19 MHz	MURATA	CSA4.19MG	30 pF	30 pF
				CST4.19MGW	30 pF (built-in)	30 pF (built-in)



(1) Ceramic, Crystal Oscillation

TMP86P203 (V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, T_{opr} = − 40 to 85°C) (Under development)

Parameter	Resonator	Oscillating Frequency	Recommended Constant	
			C_{XIN}	R_X
High-frequency oscillation	RC resonator	2 MHz	33 pF	10 kΩ
		400 kHz	100 pF	30 kΩ



(2) RC Oscillation

Note 1: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.

Note 2: To ensure stable oscillation, the resonator position, load capacitance, etc. must be appropriate. Because there factors are greatly affected by board patterns, please be sure to evaluate operation on the board on which the device will actually be mounted.

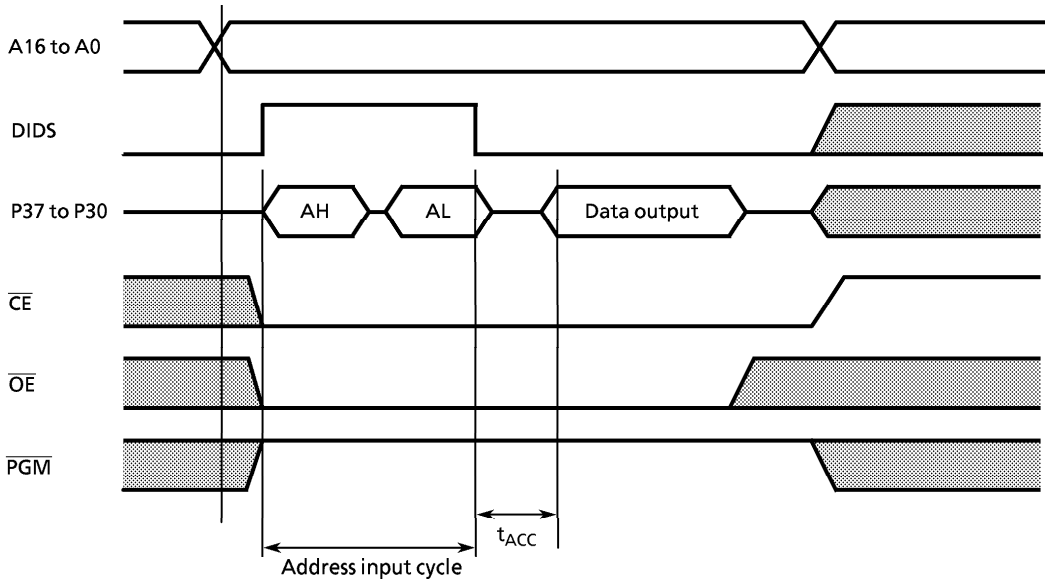
Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
http://www.murata.co.jp/search/index.html

DC Characteristics, AC Characteristics (PROM mode) (V_{SS} = 0 V, Topr = – 40 to 85°C)

(1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage	V_{IH4}		$V_{CC} \times 0.75$	–	V_{CC}	V
Low leve input voltage	V_{IL4}		0	–	$V_{CC} \times 0.25$	
Power supply	V_{CC}		4.75	5.0	5.25	
Power supply of program	V_{PP}					
Address access time	t_{ACC}	V_{CC} = 5.0 ± 0.25 V	–	–	1.5tcyc + 300	ns
Address input cycle	–		–	tcyc	–	

Note: tcyc = 250 ns at f_{CLK} = 16 MHz



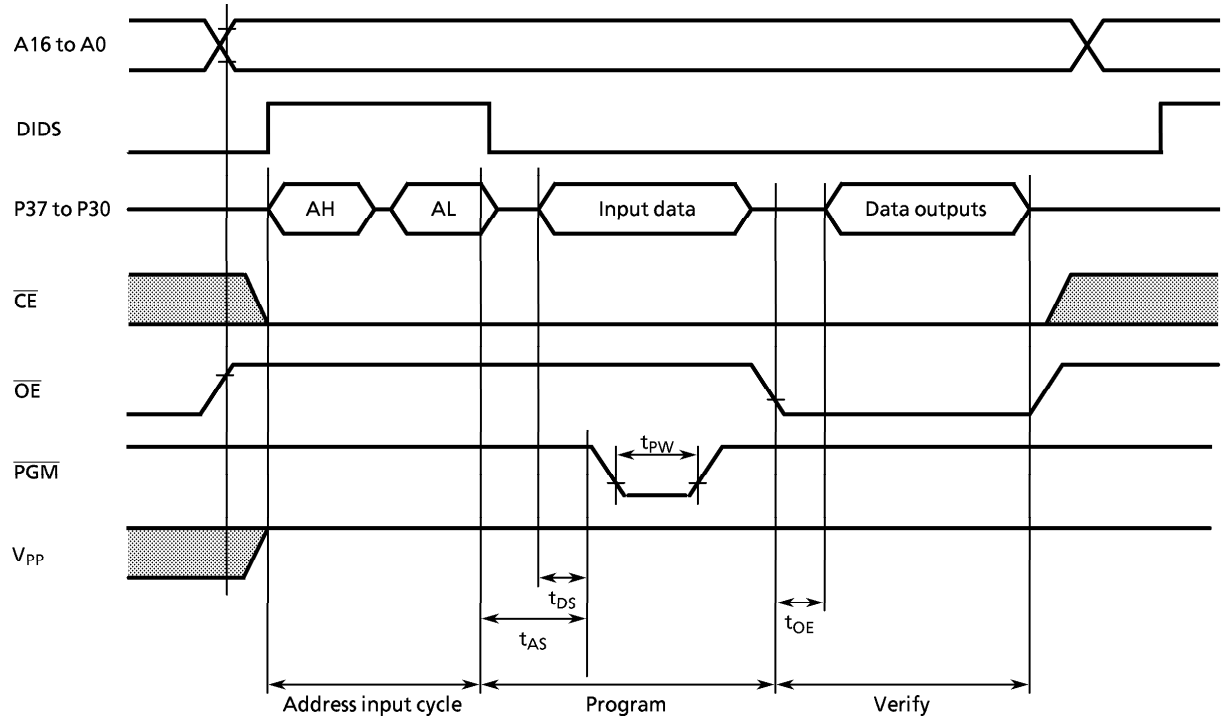
Note: DIDS and P37 to P30 are the signals for the TMP86P202/203.
All other signals are EPROM programmable.
AL: Address input (A0 to A7)
AH: Address input (A8 to A15)

(2) Program operation (High-speed) (Topr = 25 ± 5°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
High level input voltage	V_{IH4}		$V_{CC} \times 0.75$	–	V_{CC}	V
Low leve input voltage	V_{IL4}		0	–	$V_{CC} \times 0.25$	
Power supply	V_{CC}		6.0	6.25	6.5	
Power supply of program	V_{PP}		12.5	12.75	13.0	
Pulse width of initializing program	t_{PW}	V_{CC} = 6.0 V	0.095	0.1	0.105	ms
Address set up time	t_{AS}		0.5tcyc	–	–	ns
Address input cycle	–		–	tcyc	–	
Data set up time	t_{DS}		1.5tcyc	–	–	
$\overline{OE}$ to valid output data	t_{OE}		–	–	1.5tcyc + 300	

Note: tcyc = 250 ns at f_{CLK} = 16 MHz

High-speed program writing



Note: DIDS and P37 to P30 are the signals for the TMP86P202/203.
All other signals are EPROM programmable.
AL: Address input (A0 to A7)
AH: Address input (A8 to A15)

Note 1: The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.
Note 2: The pulling up/down device on the condition of V_{PP} = 12.75 V ± 0.25 V causes a damage for the device. Do not pull up/down at programming.
Note 3: Use the recommended adapter (see 1.2.2 (1)) and mode (see 1.2.2 (3) i).
Using other than the above condition may cause the trouble of the writting.