CMOS 8-Bit Microcontroller

TMP86P202P/M, TMP86P203P/M

The TMP86P202/203 are high-speed and high-performance 8-bit single chip microcomputers with small package. The MCU contain CPU core, ROM, RAM, multirole timer counter, and 8-bit AD converter, on a chip.

Product No.	ROM	RAM	Package Package	Resonator	
TMP86P202P		7.100	P-DIP20-300-2.54D	Conomic Chustol reconstan	
TMP86P202M*	2 K 0 h i .	120 0 h i .	P-SOP20-300-1.27	Ceramic, Crystal resonator	
TMP86P203P*	2 K × 8 bits	128 × 8 bits	P-DIP20-300-2.54D	RC resonator	
TMP86P203M*	LINEW DE		P-SOP20-300-1.27	NC resoliator	

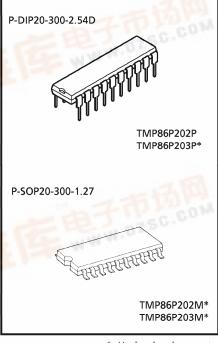
*: Under development

Features

- ◆ 8-bit single chip microcomputer TLCS-870/C series
- Instruction execution time: $0.50 \mu s (fc = 8 MHz)$
- 132 types and 731 basic instructions
- ◆ Interrupt sources: 11 factors (External: 3, Internal: 8)
- ♦ Input/Output ports: 14 pins
 - High-Current Output 2 pins (Typ. 20mA)
- ♦ 8-bit timer/counter: 2 ch
 - Timer, PDO output, Event counter, PWM output, PPG modes
 - Possible to use as 16-bit timer by connecting each other
- Time Base Timer
- Divider output function
- Watchdog Timer

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- Interrupt source/Internal Reset (programmable)
- 8-bit successive approximate type AD converter
 - Analog input: 4 ch



*: Under development

● For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter

For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance/Handling Precautions.

TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.

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The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer).

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86P202-1 2003-02-26

◆ Power saving operating modes (3 modes)

• STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/High-impedance.

• IDLE 0 mode: CPU stops, and peripherals operate using high-frequency clock of Time-Base-Timer.

Release by INTTBT interrupt.

• IDLE 1 mode: CPU stops, and peripherals operate using high-frequency clock.

Release by interrupts.

♦ Wide operating voltage: 3.3 to 5.5 V at 8 MHz (Ceramic resonator, Crystal resonator) 4.5 to 5.5 V at 2.5 MHz (RC resonator) (Under development)

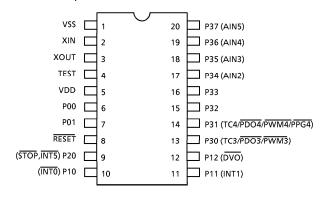
Note: AD conversion characteristics are guaranteed with limited supply voltage range (4.5 V to 5.5 V). If supply voltage is less than 4.5 V then AD conversion accuracy can not be guaranteed.

86P202-2 2003-02-26

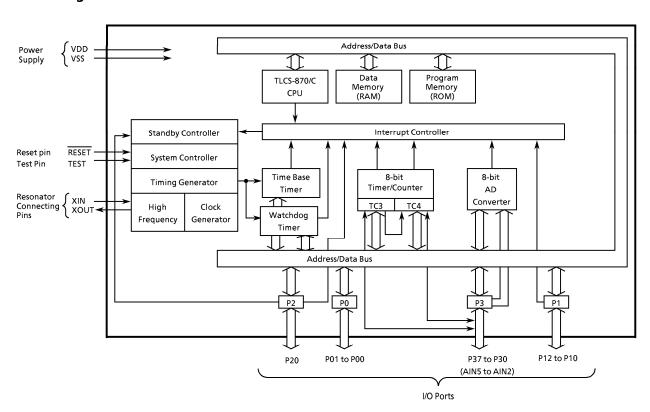
Pin Assignments (Top View)

P-DIP20-300-2.54D (for TMP86P202P and TMP86P203P*) P-SOP20-300-1.27 (for TMP86P202M* and TMP86P203M*)

*: Under development



Block Diagram



86P202-3 2003-02-26

Pin Function

The TMP86P202/203 has two modes: MCU and PROM.

(1) MCU mode

Pin Name	Input/Output	F	unction		
P01	I/O	2-bit programmable input/output ports. Each bit of these ports can be individually configured as an input or			
P00	I/O	output under software control. Nch open-drain output function.			
P12 (DVO)	I/O (Output)	3-bit programmable input/output ports (tri-state). Each bit of these ports	Divider output		
P11 (INT1)	I/O (Input)	can be individually configured as an input or output under software control.	External interrupt input 1		
P10 (INTO)	I/O (Input)	When used as function, the latch must be set to 1.	External interrupt input 0		
P20 (ĪNT5, STOP)	I/O (Input)	1-bit programmable input/output ports. When used as input port and function, the latch must be set to 1.	External interrupt input 5 or STOP mode release signal input		
P37 (AIN5)	I/O (Input)				
P36 (AIN4)	I/O (Input)		AD conventor cooler in such		
P35 (AIN3)	I/O (Input)	8-bit programmable input/output ports	AD converter analog input		
P34 (AIN2)	I/O (Input)	(tri-state). Each bit of these ports can be			
P33	1/0	individually configured as an input or output under software control.			
P32	I/O	When used as function and analog			
P31 (TC4, PDO4, PWM4, PPG4)	I/O (I/O)	inputted latch must be set to 1.	Timer/Counter 4 input, PDO, PWM, PPG output		
P30 (TC3, PDO3, PWM3)	I/O (I/O)		Timer/Counter 3 input, PDO, PWM output		
XIN, XOUT	Input, Output	Resonator connecting pins for high-freque used and XOUT is opened.	ncy clock. For inputting external clock, XIN is		
RESET	Input	RESET signal input			
TEST	Input	TEST pin for out-going test. Be fixed to lov	v.		
VDD, VSS	Power Supply	+ 5 V, 0 (GND)			

(2) PROM mode

Pin Name (PROM mode)	Input/Output	Functions	Pin name (MCU mode)
A16			XOUT
A15 to A8	Input	Program memory address inputs	P37 to P30
A7 to A0			P37 to P30
D7 to D0	I/O	Program memory data input/outputs	P37 to P30
CE		Chip enable signal input	P00
ŌĒ	1	Output enable signal input	P20
PGM	Input	Program mode signal input	P01
DIDS		PROM mode control signal	P12
VPP		+ 12.75 V/5 V (Program supply voltage)	TEST
vcc	Power supply	+ 6.25 V/5 V	VDD
GND		0 V	VSS
P11		PROM mode setting pins. Be fixed at high level.	
RESET	Input	PROM mode setting pins. Be fixed at low level.	
CLK		Input a clock from the outside.	XIN

Operational Description

1. CPU Core Functions

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and watchdog timer.

This section provides a description of the CPU core, the program memory, the data memory, and the reset circuit.

1.1 Memory Address Map

The TMP86P202/203 memory consist of 3 blocks: ROM, RAM and SFR (Special Function Register). They are all mapped in 64-Kbyte address space. Figure 1-1 shows the TMP86P202/203 memory address map. The general-purpose register banks are not assigned to the RAM address space.

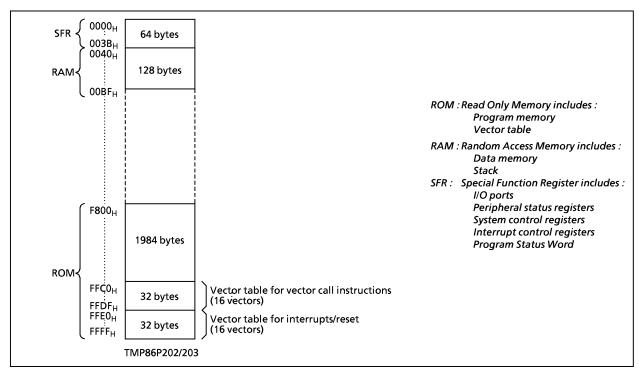


Figure 1-1. Memory Address Maps

1.2 Program Memory (ROM)

The TMP86P202/203 has a 2 K \times 8 bits (address F800_H to FFFF_H), of program memory. However, placing program memory on the internal RAM is deregulated if a certain procedure is executed (See 2.4.5 Address Trap).

86P202-6

2003-02-26

Electrical Characteristics

Absolute Maximum Ratings

 $(V_{SS} = 0 V)$

Parameter	Symbol	Pins	Rating	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	
Program voltage	V_{PP}	TEST/V _{PP}	– 0.3 to 13.0	
Input Voltage	V_{IN}		– 0.3 to V _{DD} + 0.3	٧
Outrout Valtana	V _{OUT1}	RESET, Tri-state Port	– 0.3 to V _{DD} + 0.3	
Output Voltage	V _{OUT2}	P20, Sink Open Drain Port	– 0.3 to 5.5	
	I _{OUT1} I _{OH}	P0, P1, P3 Port	- 1.8	
Output Current (Per 1 pin)	I _{OUT2} I _{OL}	P1, P2, P3 Port	12	
	I _{OUT3} I _{OL}	P0 Port	30	mΑ
	Σ l _{OUT1}	P0, P1, P3 Port	- 12	mA
Output Current (Total)	Σ I _{OUT2}	P1, P2, P3 Port	40	
	Σ I _{OUT3}	P0 Port	60	
		DIP	250	\A/
Power Dissipation [$T_{opr} = 85^{\circ}C$]	PD	SOP	180	mW
Soldering Temperature (time)	Tsld		260 (10 s)	
Storage Temperature	Tstg		– 55 to 150	°C
Operating Temperature	Topr		– 40 to 85	

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Condition

 $(V_{SS} = 0 \text{ V}, \text{ Topr} = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Pins	Condition	Min	Max	Unit
			NORMAL1 mode	3.3 (TMP86P202)		
Supply Voltage	V_{DD}		IDLE0, 1 mode	4.5 (TMP86P203)	5.5	
			STOP mode	2.0		
V _{IH}	V _{IH1}	Except Hysteresis input	V > 4.5.V	$V_{DD} \times 0.70$	V _{DD}	V
Input high Level	V _{IH2}	Hysteresis input	$V_{DD} \ge 4.5 V$	$V_{DD} \times 0.75$		
	V _{IH3}		V _{DD} < 4.5 V	$V_{DD} \times 0.90$		
	V_{IL1}	Except Hysteresis input	V _{DD} ≧ 4.5 V		$V_{DD} \times 0.30$	
Input low Level	V_{IL2}	Hysteresis input	V _{DD} ≦ 4.3 V	0	$V_{DD} \times 0.25$	
	V _{IL3}		V _{DD} < 4.5 V		$V_{DD} \times 0.10$	
Clask Fraguency	fc	VIN VOLIT	V _{DD} = 3.3 to 5.5 V (TMP86P202)	1.0	8.0	N/LI-
Clock Frequency	I TC	XIN, XOUT	V _{DD} = 4.5 to 5.5 V (TMP86P203)*	0.4	2.5	MHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: AD conversion characteristics are guaranteed with limited supply voltage range (4.5 V to 5.5 V). If supply voltage is less than 4.5 V then AD conversion accuracy can not be guaranteed.

^{*:} Under development

DC Standard

D	C Charact	eris	tics		$(V_{SS} = 0 V, T)$	Ор	$r = -40 \text{ to } 85^{\circ}\text{C}$
		Т		т			1

Parameter	Symbol	Pins	Condition	Min	Тур.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input		-	0.9	-	V
	I _{IN1}	TEST					
Innest Comment		Sink Open Drain, Tri-state				± 2	١,
Input Current	I _{IN2}	Port	$V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V}/0 \text{ V}$	_	_	12	μA
	I _{IN3}	RESET, STOP					
Input Resistance	R _{IN2}	RESET Pull-Up		100	220	450	kΩ
Output Leakage Current	I _{LO}	Sink Open Drain, Tri-state Port	V _{DD} = 5.5 V, V _{OUT} = 5.5 V/0 V	-	-	± 2	μΑ
Output High Voltage	V _{OH}	P0, P1, P3 Port	$V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$	4.1	_	_	l ,,
Output Low Voltage	V _{OL}	P1, P2, P3 Port	$V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$	_	_	0.4	V
Output Low Current	l _{OL}	Middle Current Port (except	V _{DD} = 4.5 V, V _{OL} = 1.0 V	_	8	_	
		XOUT, P0)					-
Output Low Current	l _{OL}	High Current Port (P0 Port)	$V_{DD} = 4.5 \text{ V}, V_{OL} = 1.0 \text{ V}$		20	-	
Supply Current in			V _{DD} = 5.5 V	_	3.0	5.5	mA
NORMAL 1 mode			V _{IN} = 5.3/0.2 V		0.0	0.0	
Supply Current in	1 .		fc = 8.0 MHz		1.9	4.0	
IDLE 0, 1 mode	lDD		10 - 0.0 191112	_	۳.۱	4.0	
Supply Current in			V _{DD} = 5.5 V		0.5	10.0	
STOP mode			V _{IN} = 5.3 V/0.2 V	-	0.5	10.0	μA

Note 1: Typical values show those at Topr = 25° C, $V_{DD} = 5 \text{ V}$

Note 2: Input current (I_{IN1} , I_{IN3}); The current through pull-up or pull-down resistor is not included.

Note 3: IDD does not include IREF current.

AD Conversion Characteristics

 $(V_{SS} = 0.0 \text{ V}, V_{DD} = 4.5 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Analog Input Voltage	V_{AIN}		V _{SS}	-	V_{DD}	٧
Power Supply Current of Analog Reference Voltage	I _{REF}	$V_{DD} = 5.5 V$ $V_{SS} = 0.0 V$	-	0.6	1.0	mA
Non linearity Error			-	_	± 2	
Zero Point Error		V _{DD} = 5.0 V, V _{SS} = 0.0 V	-	_	± 2	LSB
Full Scale Error		$V_{SS} = 0.0 V$	-	_	± 2	LOB
Total Error			-	_	± 4	

- Note 1: The total error includes all errors except a quantization error, and is defined as a maximum deviation from the ideal conversion line.
- Note 2: Conversion time is different in recommended value by power supply voltage.

 About conversion time, please refer to "2.7.2 Register Configuration".
- Note 3: Please use input voltage to AIN input Pin in limit of V_{DD} V_{SS}.

 When voltage of range outside is input, conversion value becomes unsettled and gives affect to other channel conversion value.
- Note 4: The relevant pin for I_{REF} is V_{DD} , so that the current flowing into V_{DD} is the power supply current $I_{DD} + I_{REF}$.
- Note 5: AD conversion characteristics are guaranteed with limited supply voltage range (4.5 V to 5.5 V). If supply voltage is less than 4.5 V then AD conversion accuracy can not be guaranteed.

AC Characteristics

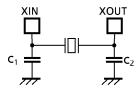
 $(V_{SS} = 0 \text{ V}, V_{DD} = 3.3 \text{ to } 5.5 \text{ V}, Topr = -40 \text{ to } 85^{\circ}\text{C})$

Parameter	Symbol	Condition	Min	Тур.	Max	Unit
Machine Cycle Time	tou	NORMAL 1 mode	0.5		•	
Machine Cycle Time	tcy	IDLE 0, 1 mode	0.5	_	8	μ S
High Level Clock Pulse Width	twcH	For external clock operation (XIN input)	F0			ns
Low Level Clock Pulse Width	twcL	fc = 8 MHz	50	_	I	113

Recommended Oscillation Conditions

TMP86P202 ($V_{SS} = 0 \text{ V}, V_{DD} = 3.3 \text{ to } 5.5 \text{ V}, T_{opr} = -40 \text{ to } 85^{\circ}\text{C}$)

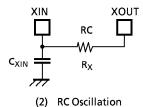
Parameter Resonator		Oscillating	Recomm	nended Resonator	Recommended Constant		
Parameter	Parameter Resonator		Recommended Resonator		C ₁	C ₂	
	O NALI-	MURATA	CSA8.00MTZ	30 pF	30 pF		
High-frequency	Coromic reconster	8 MHz		CST8.00MTW	30 pF (built-in)	30 pF (built-in)	
oscillation Ceramic resonato	Ceramic resonator	4.40.8411	MURATA	CSA4.19MG	30 pF	30 pF	
		4.19 MHz		CST4.19MGW	30 pF (built-in)	30 pF (built-in)	



(1) Ceramic, Crystal Oscillation

TMP86P203 ($V_{SS} = 0 \text{ V}$, $V_{DD} = 4.5 \text{ to } 5.5 \text{ V}$, $T_{opr} = -40 \text{ to } 85^{\circ}\text{C}$) (Under development)

Parameter	Resonator	Oscillating	Recommended Constant		
Parameter	Resolution	Frequency	C _{XIN}	RX	
High-frequency	RC resonator	2 MHz	33 pF	10 k Ω	
High-frequency oscillation	NC resonator	400 kHz	100 pF	30 kΩ	



- Note 1: When using the device (oscillator) in places exposed to high electric fields such as cathode-ray tubes, we recommend electrically shielding the package in order to maintain normal operating condition.
- Note 2: To ensure stable oscillation, the resonator position, load capacitance, etc. must be appropriate. Because there factors are greatly affected by board patterns, please be sure to evaluate operation on the board on which the device will actually be mounted.
- Note 3: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html

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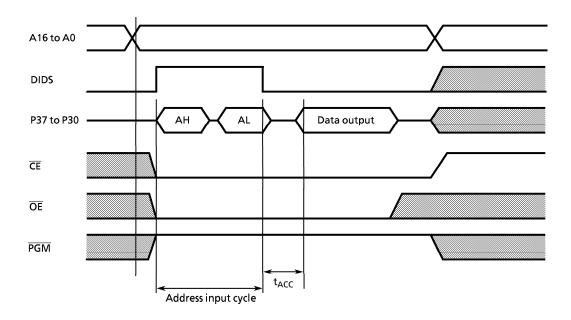
DC Characteristics, AC Characteristics (PROM mode)

 $(V_{SS} = 0 \text{ V, Topr} = -40 \text{ to } 85^{\circ}\text{C})$

(1) Read operation in PROM mode

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
High level input voltage	V _{IH4}		$V_{CC} \times 0.75$	-	V _{CC}	
Low leve input voltage	V _{IL4}		0	-	V _{CC} × 0.25	
Power supply	V _{CC}		4.75	5.0	5.25	\ \
Power supply of program	V_{PP}		4.73	5.0	3.23	
Address access time	t _{ACC}	$V_{CC} = 5.0 \pm 0.25 \text{ V}$	_	ı	1.5tcyc + 300	ns
Address input cycle	-		_	tcyc	_	113

Note: $tcyc = 250 \text{ ns at } f_{CLK} = 16 \text{ MHz}$



Note: DIDS and P37 to P30 are the signals for the TMP86P202/203.

All other signals are EPROM programmable.

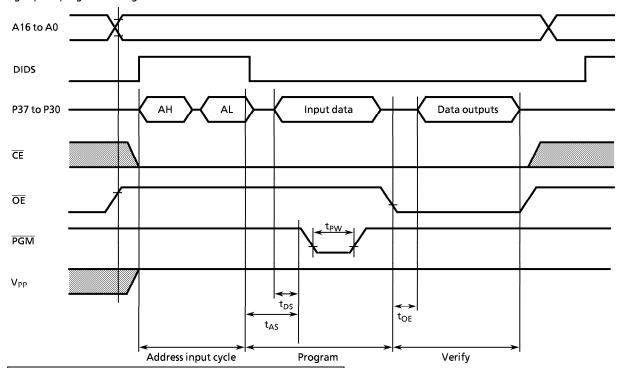
AL: Address input (A0 to A7)
AH: Address input (A8 to A15)

(2) Program operation (High-speed) (Topr = $25 \pm 5^{\circ}$ C)

Parameter	Symbol	Conditions	Min	Тур.	Max	Unit
High level input voltage	V _{IH4}		$V_{CC} \times 0.75$	-	V _{CC}	٧
Low leve input voltage	V _{IL4}		0	-	$V_{CC} \times 0.25$	
Power supply	V _{CC}		6.0	6.25	6.5	
Power supply of program	V_{PP}		12.5	12.75	13.0	
Pulse width of initializing program	t _{PW}	V _{CC} = 6.0 V	0.095	0.1	0.105	ms
Address set up time	t _{AS}		0.5tcyc	-	_	ns
Address input cycle	_		_	tcyc	_	
Data set up time	t _{DS}		1.5tcyc	-	_	
OE to valid output data	t _{OE}		-	-	1.5tcyc + 300	

Note: tcyc = 250 ns at $f_{CLK} = 16$ MHz

High-speed program writing



Note: DIDS and P37 to P30 are the signals for the TMP86P202/203.
All other signals are EPROM programmable.

AL: Address input (A0 to A7)
AH: Address input (A8 to A15)

Note 1: The power supply of V_{PP} (12.75 V) must be set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC} .

Note 2: The pulling up/down device on the condition of $V_{PP} = 12.75 \text{ V} \pm 0.25 \text{ V}$ causes a damage for the device. Do not pull up/down at programming.

Note 3: Use the recommended adapter (see 1.2.2 (1)) and mode (see 1.2.2 (3) i).

Using other than the above condition may cause the trouble of the writting.