CMOS 8-Bit Microcontroller

TMP87CM23AF, TMP87CP23F

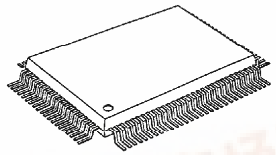
The TMP87CM23A/CP23 are the high speed and high performance 8-bit single chip microcomputers. These MCU contain, large ROM, RAM, input/output ports, LCD driver, a 8-bit AD converter, four multi-function timer/counters, two serial interfaces, and two clock generators on chip.

Product No.	ROM	RAM	Package	OTP MCU
TMP87CM23AF	32 K × 8-bit	1 K × 8-bit	P-QFP100-1420-0.65A	TMP87PP23F
TMP87CP23F	48 K × 8-bit	2 K × 8-bit		

Features

- ◆8-bit single chip microcomputer TLCS-870 Series
- ◆Instruction execution time: 0.5 μs (at 8 MHz), 122 μs (at 32.768 kHz)
- ◆129 types and 412 basic instructions
  - Multiplication and Division (8 bits × 8 bits , 16 bits ÷ 8 bits): Execution time 3.5 μs (at 8 MHz)
  - Bit manipulations (Set/Clear/Complement/Load/Store/Test/ Exclusive OR)
  - 16-bit data operations
  - 1-byte jump/call (Short relative jump/Vector call)
- ◆14 interrupt sources (External: 5, Internal: 9)
  - All sources have independent latches each, and nested interrupt control is available
  - 4 edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ◆10 Input/Output ports (Max. 70 pins)
- ◆Two 16-bit Timer/Counters
  - Timer, Event counter, External trigger timer, Window, PPG output Pulse width measurement modes
- ◆Two 8-bit Timer/Counters
  - Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, PDO modes
- ◆Time Base Timer (Interrupt frequency: 1 Hz to 16384 Hz)
- ◆Divider output function (frequency: 1 kHz to 8 kHz)
- ◆Watchdog Timer
- ◆Two 8-bit Serial Interfaces
  - Each 8 bytes transmit/receive data buffer
  - Internal/external serial clock, and 4/8-bit mode

P-QFP100-1420-0.65A



TMP87CM23AF
TMP87CP23F

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◆LCD driver
- With display memory (20 bytes)
- LCD direct drive capability (Max. 40 seg × 4 com)
- 1/4, 1/3, 1/2 duty or static drive are programmably selectable

◆8-bit successive approximate type AD converter with sample and hold
- 8 analog inputs
- Conversion time:23 μs / 92 μs (at 8 MHz)

◆Dual clock operation (optinal)

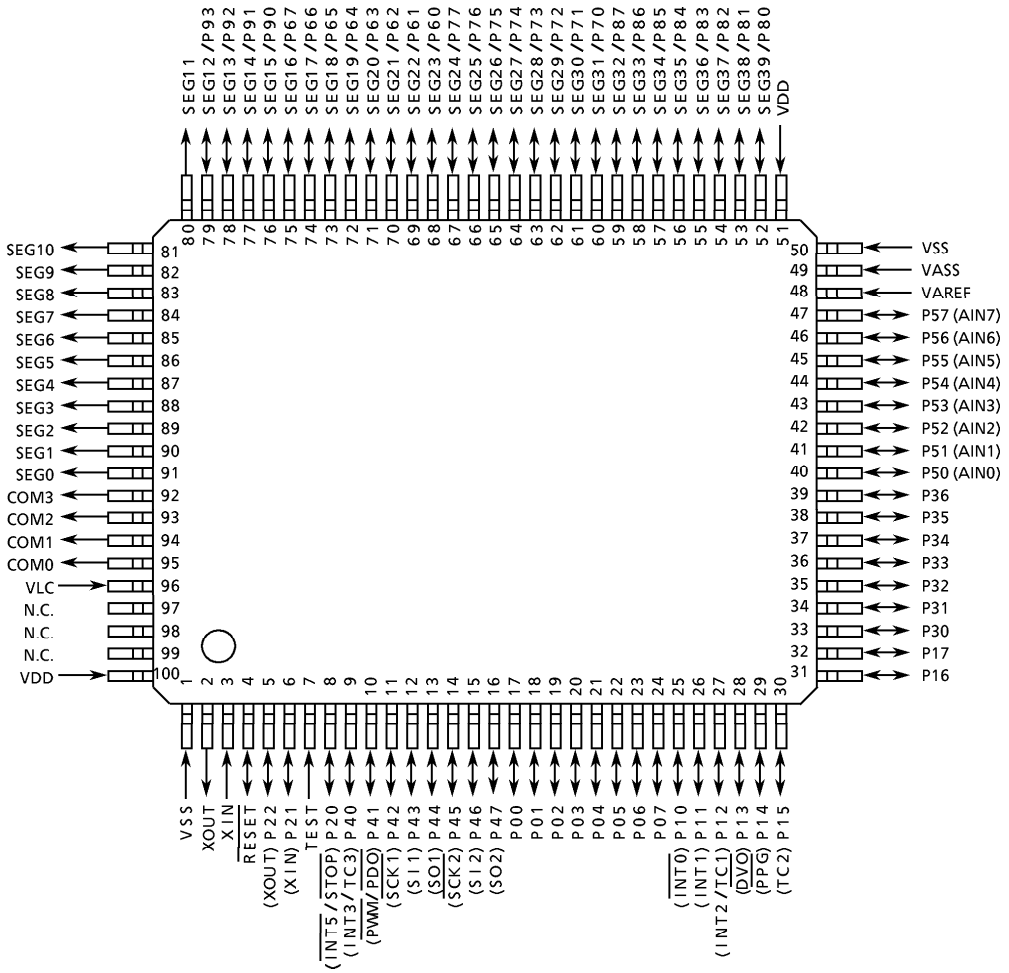
◆Five Power saving operating modes
- STOP mode: Oscillation stops. Battery/Capacitor back-up.
  Port output hold/high-impedance.
- SLOW mode: Low power consumption operation using
  low-frequency clock (32.768 kHz).
- IDLE1 mode: CPU stops, and Peripherals operate using
  high-frequency clock.
  Release by interrupts.
- IDLE2 mode: CPU stops, and Peripherals operate using high and low frequency clock.
  Release by interrupts.
- SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock.
  Release by interrupts.

◆Operating Voltage: 2.7 to 5.5 V at 4.2 MHz / 32.768 kHz, 4.5 to 5.5 V at 8 MHz / 32.768 kHz

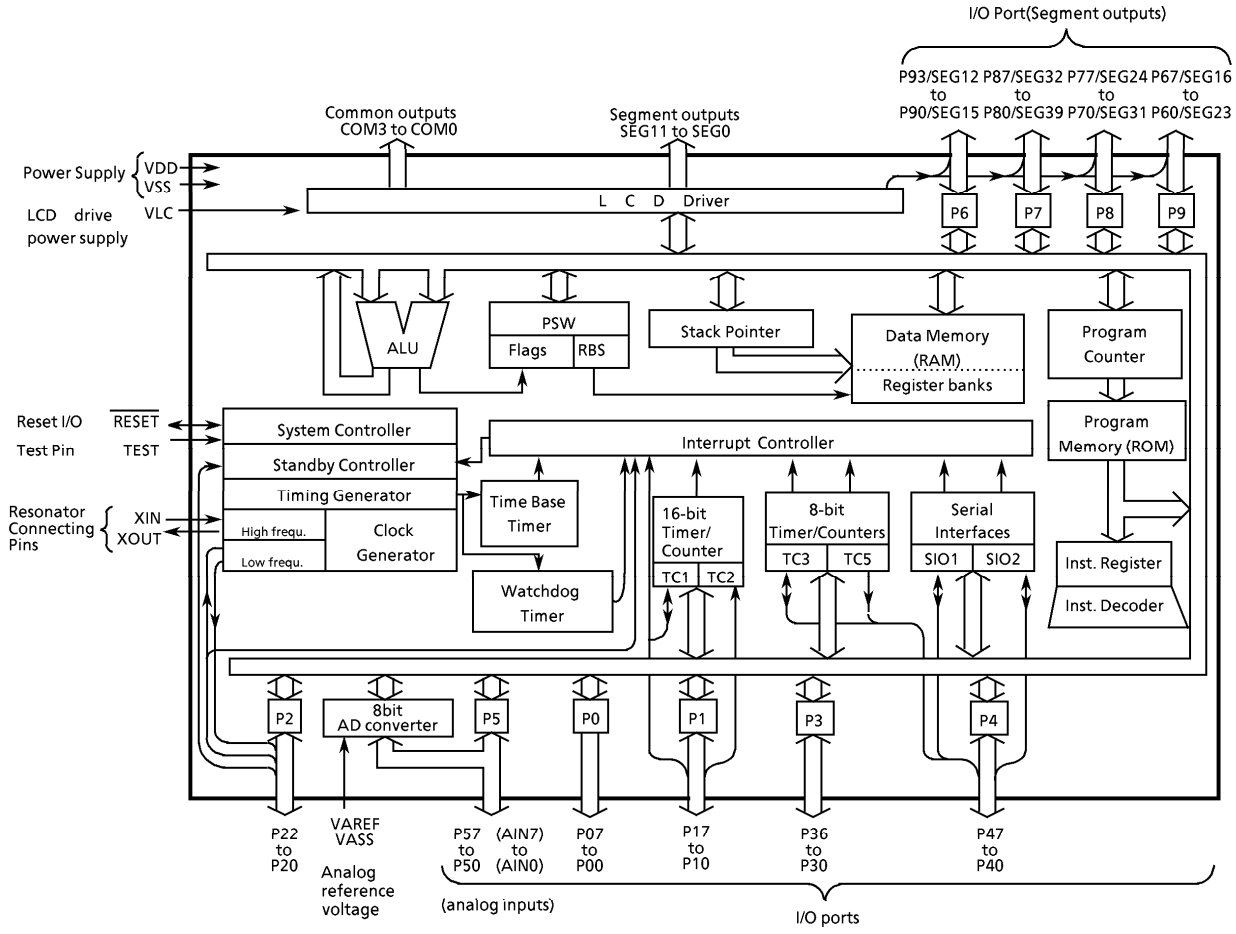
◆Emulation Pod: BM87CP23F0A

Pin Assignments (Top View)

P-QFP100-1420-0.65A



Block Diagram



Pin Function

Pin Name	Input / Output	Function	
P07 to P00	I/O	8-bit programmable input/output ports (tri-state).	
P17, P16			
P15 (TC2)	I/O (Input)	Each bit of these ports can be individually configured as an input or an output under software control. When used as an input port, timer/counter input or external interrupt input, the P0CR/P1CR must be set to "0". When used as timer/counter output or divider output, the P0CR/P1CR must be set to "1" after setting output latch to "1".	Timer/Counter 2 input
P14 ($\overline{PPG}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{DVO}$)			Divider output
P12 (INT2 / TC1)	I/O (Input)		External interrupt 2 input or Timer/Counter 1 input
P11 (INT1)			External interrupt 1 input
P10 ($\overline{INT0}$)			External interrupt 0 input
P22 (XTOUT)	I/O (Output)	3-bit input/output port with latch. When used as an input port, external interrupt input or STOP mode release input, the output latch must be set to "1".	Resonator connecting pins (32.768kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{INT5}$ / $\overline{STOP}$)			External interrupt 5 input or STOP mode release signal input
P36 to P30	I/O	7-bit input/output port with latch. When used as input port, the output latch must be set to "1".	
P47 (SO2)	I/O (Output)	8-bit input/output port with latch. When used as serial interface output or timer/counter output, the P4CR1 must be set to "1" after setting output latch to "1". When used as an input port, serial interface input or external interrupt input, the P4CR1 must be set to "0".	SIO2 serial data output
P46 (SI2)	I/O (Input)		SIO2 serial data input
P45 ($\overline{SCK2}$)	I/O (I/O)		SIO2 serial clock input/output
P44 (SO1)	I/O (Output)		SIO1 serial data output
P43 (SI1)	I/O (Input)		SIO1 serial data input
P42 ($\overline{SCK1}$)	I/O (I/O)		SIO1 serial clock input/output
P41 ($\overline{PWM}$/$\overline{PDO}$)	I/O (Output)		8-bit PWM output, 8-bit programmable divider output
P40 (INT3/TC3)	I/O (Input)		External interrupt 3 input, Timer/Counter 3 input
P57 (AIN07) to P50 (AIN00)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output under software control. When used as analog input, the P5CR must be set to "0".	AD converter analog inputs
SEG39 (P80) to SEG32 (P87)	Output (I/O)	8-bit input/output port with latch. When used as an input port, the segment output control register must be set to "0" after setting output latch to "1".	LCD segment outputs. When used as segment output, the segment output control register must be set to "1".
SEG31 (P70) to SEG24 (P77)	Output (I/O)		
SEG23 (P60) to SEG16 (P67)	Output (I/O)		
SEG15 (P90) to SEG12 (P93)	Output (I/O)	4-bit input/output port with latch. When used as an input port, the segment output control register must be set to "1" after setting output latch to "1".	
SEG11 to SEG0	Output	LCD segment outputs	
COM3 to COM0	Output	LCD common outputs	
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{RESET}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output	
TEST	Input	Test pin for out-going test. Be fixed to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	
VAREF, VASS		Analog reference voltage inputs (High, Low)	
VLC	LCD drive power supply.		

OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the TMP87CM23A/P23. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

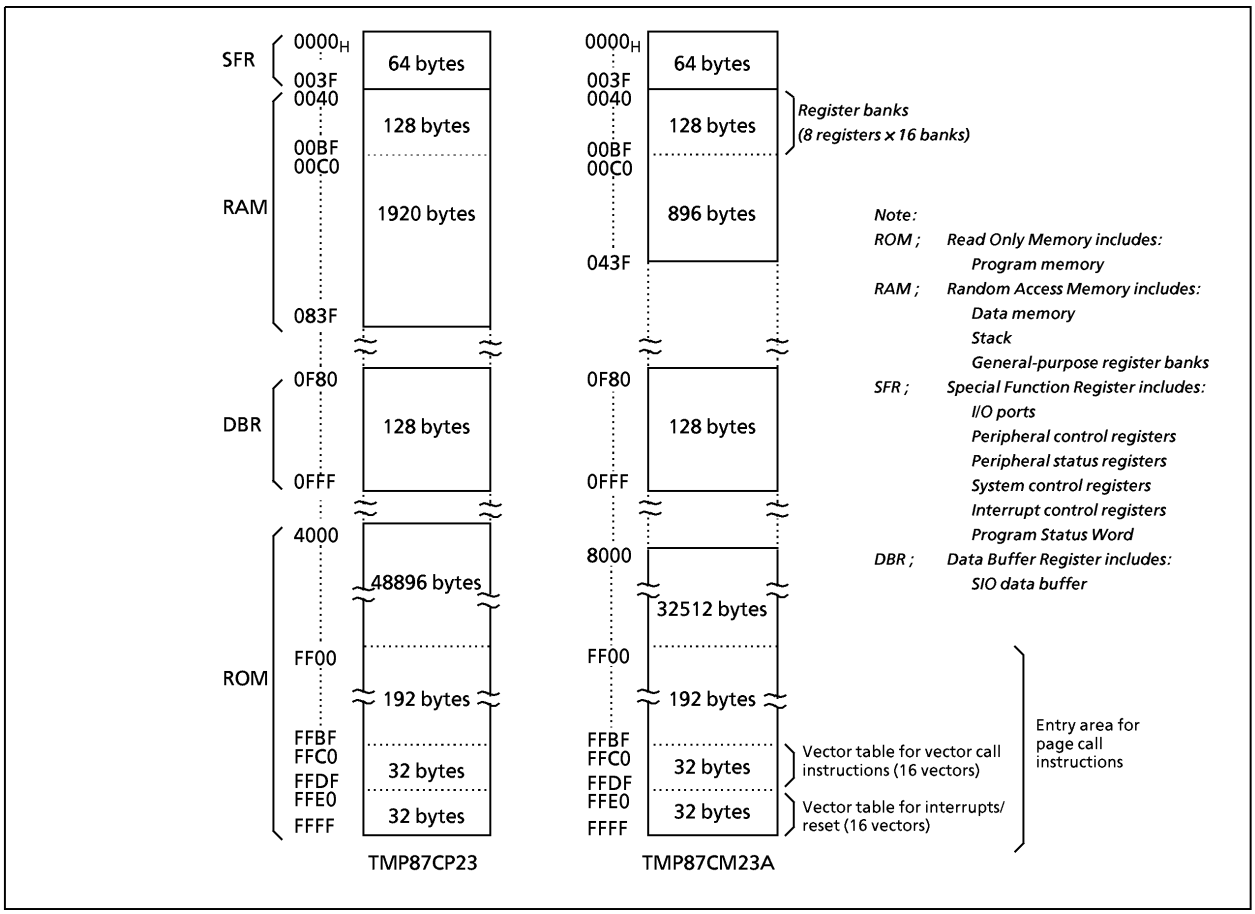


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings

(V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1 pin)	I_{OUT1}	Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41)	3.2	mA
	I_{OUT2}	P41	30	
Output Current (Total)	ΣI_{OUT1}	Ports P0, P1, P2, P3, P5, P6, P7, P8, P9, P4 (except P41)	120	mA
	ΣI_{OUT2}	P41	30	
Power Dissipation [Topr = 70°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10 s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 70	°C

Note 1: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Note 2: The absolute maximum input/output voltage ratings for the TMP87CM23A/CP23/PP23 are – 0.3 to VDD + 0.3 [V] at all I/O ports including sink open drain output ports. (However, the VPP pin of TMP87PP23 is not contained in these condition.)

Recommended Operating Conditions

(V_{SS} = 0 V, Topr = – 30 to 70°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc = 4.2 MHz	NORMAL1, 2 mode	2.7		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		$V_{DD} \times 0.70$	V_{DD}	V
	V_{IH2}	Hysteresis input			$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.90$		
Input Low Voltage	V_{IL1}	Except hysteresis input	$V_{DD} \geqq 4.5$ V		0	$V_{DD} \times 0.30$	V
	V_{IL2}	Hysteresis input				$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V			$V_{DD} \times 0.10$	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		0.4	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.2	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL1/2 mode and IDLE1/2 mode.

DC Characteristics

(V_{SS} = 0 V, Topr = − 30 to 70°C)

Parameter	Symbol	Pins	Conditions	Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis inputs		—	0.9	—	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V, V_{IN} = 5.5 V / 0 V	—	—	± 2	μA
	I_{IN2}	Open drain ports and tri-state ports					
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$					
Input Low Current	I_{IL}	Push-pull ports	V_{DD} = 5.5 V, V_{IN} = 0.4 V	—	—	− 2	mA
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO1}	Open drain ports	V_{DD} = 5.5 V, V_{OUT} = 5.5 V	—	—	2	μA
	I_{LO2}	Tri-state ports	V_{OUT} = 5.5 V / 0 V	—	—	± 2	
Segment Output Low Resistance	R_{OS1}	SEG39 to SEG0	V_{DD} = 5 V, $V_{DD} - V_{LC}$ = 3 V	—	20	—	kΩ
Common Output Low Resistance	R_{OC1}	COM3 to COM0					
Segment Output High Resistance	R_{OS2}	SEG39 to SEG0		—	200	—	kΩ
Common Output High Resistance	R_{OC2}	COM3 to COM0					
Segment/Common Output Voltage	$V_{O\ 2/3}$	SEG39 to SEG0 and COM3 to COM0		3.8	4.0	4.2	V
	$V_{O\ 1/2}$			3.3	3.5	3.7	
	$V_{O\ 1/3}$			2.8	3.0	3.2	
Output High Voltage	V_{OH1}	Push-pull ports (P4 port)	V_{DD} = 4.5 V, I_{OH} = − 200 μA	2.4	—	—	V
	V_{OH2}	Tri- state ports (P0, P1, P5 ports)	V_{DD} = 4.5 V, I_{OH} = − 0.7 mA	4.1	—	—	
Output Low Voltage	V_{OL}	Except XOUT and P41	V_{DD} = 4.5 V, I_{OL} = 1.6 mA	—	—	0.4	V
Output Low Current	I_{OL3}	P41	V_{DD} = 4.5 V, V_{OL} = 1.0 V	—	20	—	mA
Supply Current in NORMAL 1 , 2 mode	I_{DD}		V_{DD} = 5.5 V, fc = 8 MHz, fs = 32.768 kHz, V_{IN} = 5.3 V / 0.2 V	—	10	16	mA
Supply Current in IDLE 1, 2 mode				—	6	10	
Supply Current in SLOW mode			V_{DD} = 3.0 V, fs = 32.768 kHz, V_{IN} = 2.8 V / 0.2 V, LCD driver is not enable	—	30	60	μA
Supply Current in SLEEP mode				—	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5 V, V_{IN} = 5.3 V / 0.2 V	—	0.5	10	μA

Note 1: Typical values show those at Topr = 25°C , V_{DD} = 5 V.
Note 2: Input Current ; The current through pull-up or pull-down resistor is not included.
Note 3: I_{DD} ; Except for I_{REF}
Note 4: Output resistors Ros, Roc indicate "on" when switching levels.
Note 5: $V_{O2/3}$ indicates an output voltage at the 2/3 level when operating in the 1/4 or 1/3 duty mode.
Note 6: $V_{O1/2}$ indicates an output voltage at the 1/2 level when operating in the 1/2 duty or static mode.
Note 7: $V_{O1/3}$ indicates an output voltage at the 1/3 level when operating in the 1/4 or 1/3 duty mode.
Note 8: When using LCD, it is necessary to consider values of Ros1/2 and Rbc1/2.
Note 9: Times for SEG/COM output switching on: Ros1, Roc1: 2^6/fc, 2/fc (s)
Ros2, Roc2: 1/(n, f_F)
(1/n: duty, f_F: frame frequency)

AD Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	2.7	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}	V_{AREF} = 5.5 V, V_{ASS} = 0.0 V	–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0 V, V_{SS} = 0.0 V V_{AREF} = 5.000 V V_{ASS} = 0.000 V or V_{DD} = 2.7 V, V_{SS} = 0.0 V V_{AREF} = 2.700 V V_{ASS} = 0.000 V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

Note: Quantizing error is not contained in those errors.

AC Characteristics

(V_{SS} = 0 V, V_{DD} = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL 1, 2 mode	0.95	–	10	μs
		In IDLE 1, 2 mode				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 70°C)

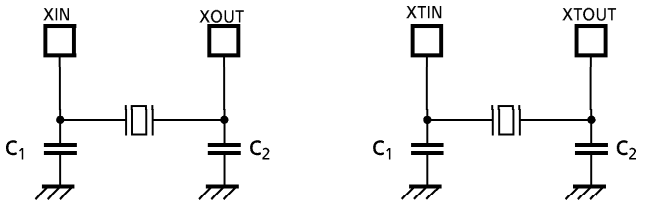
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	t_{cy}	In NORMAL 1, 2 mode	0.95	–	10	μs
		In IDLE 1, 2 mode				
		In SLOW mode	117.6	–	133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input), fc = 4.2 MHz	110	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input), fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

Recomended Oscillating Condition-1 (for TMP87CP23) (VSS = 0 V, VDD = 4.5 to 5.5 V, Topr = – 30 to 70°C)

Parameter	Osillator	Frequency	Recommender Oscillator		Recommended Condition	
					C_1	C_2
High-frequency	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30 pF	30 pF
			Standard/Lead Type (MURATA)	CSA8.00MTZ CST8.00MTW	Built-in 30 pF	Built-in 30 pF
			Standard/SMP Type (MURATA)	CSACS8.00MT	30 pF	30 pF
			Standard/Small ChipType (MURATA)	CSTCS8.00MT	Built-in 30 pF	Built-in 30 pF
		4 MHz	KYOCERA	KBR4.0MS	30 pF	30 pF
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF

Recomended Oscillating Condition-2 (for TMP87CP23) (VSS = 0V, VDD = 2.7 to 5.5V, Topr = – 30 to 70°C)

Parameter	Osillator	Frequency	Recommender Oscillator		Recommended Condition	
					C_1	C_2
High-frequency	Ceramic Resonator	4 MHz	Standard/Lead Type	CSA4.00MG	30 pF	30 pF
			(MURATA)	CST4.00MGW	Built-in 30 pF	Built-in 30 pF
			Standard/SMD Type (MURATA)	CSA4.00MGC CSAC4.00MGCM CSTC4.00MG	30 pF	30 pF
					Built-in 30 pF	Built-in 30 pF
			Standard/Small Chip Type	CSTCS4.00MG	Built-in 10 pF	Built-in 10 pF



(1) High-frequency (2) Low-frequency

Note 1: When used in high electric field such as a picture tube, the package is recommended to be electrically shielded to maintain a regular operation.

Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL; http://www.murata.co.jp/search/index.html