CMOS 8-Bit Microcontroller

TMP87CM53F

The 87CM53 is the high speed and high performance 8-bit single chip microcomputers. These MCU contain CPU core, ROM, RAM, input/output ports, an A/D converter, DTMF generator, multi-function timer/counters, two serial interfaces, and two clock generators on a chip. The 87CM53 provides high current output capability for LED direct drive.

Part No.	ROM	RAM	Package	OTP MCU
TMP87CM53F	32 K × 8-bit	1024 × 8-bit	P-QFP80-1420-0.80B	TMP87PM53F

Features

◆8-bit single chip microcomputer TLCS-870 Series
◆Instruction execution time: 0.5 μs (at 8 MHz, gear ratio1/1),
122 μs(at 32.768 kHz)
◆412 basic instructions
- Multiplication and Division (8 bits × 8 bits , 16 bits ÷ 8 bits)
- Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
- 16-bit data operations
- 1-byte jump/subroutine-call (Short relative jump / Vector call)

◆15 interrupt sources (External: 5, Internal: 10)
- All sources have independent latches each, and nested interrupt control is available.
- edge-selectable external interrupts with noise reject
- High-speed task switching by register bank changeover

◆10 Input/Output ports (72 pins)
- High current output: 7 pins (typ. 20 mA)

◆Two 16-bit Timer/Counters
- Timer, Event counter, Programmable pulse generator output, Pulse width measurement, External trigger timer, Window modes

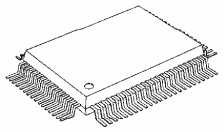
◆Two 8-bit Timer/Counters
- Timer, Event counter, Capture (Pulse width/duty measurement), PWM output, Programmable divider output modes

◆Time Base Timer (Interrupt frequenc: 0.95 Hz to 16384 Hz)
◆Divider output function (frequency: 0.976 kHz to 8.192 kHz)
◆Tone generator
- Single tone / Dual tone (DTMF) output function
- Melody (sine wave / square wave) output function

◆Watchdog Timer
◆8-bit Serial Interface
- 8 bytes transmit/receive data buffer
- Internal/external serial clock, and 4/8-bit mode

◆UART
◆8-bit successive approximate type A/D converter with sample and hold
- 8 analog inputs
- Conversion time:23 μs or 92 μs (at 8 MHz, gear ratio1/1)

P-QFP80-1420-0.80B



TMP87CM53F
TMP87PM53F

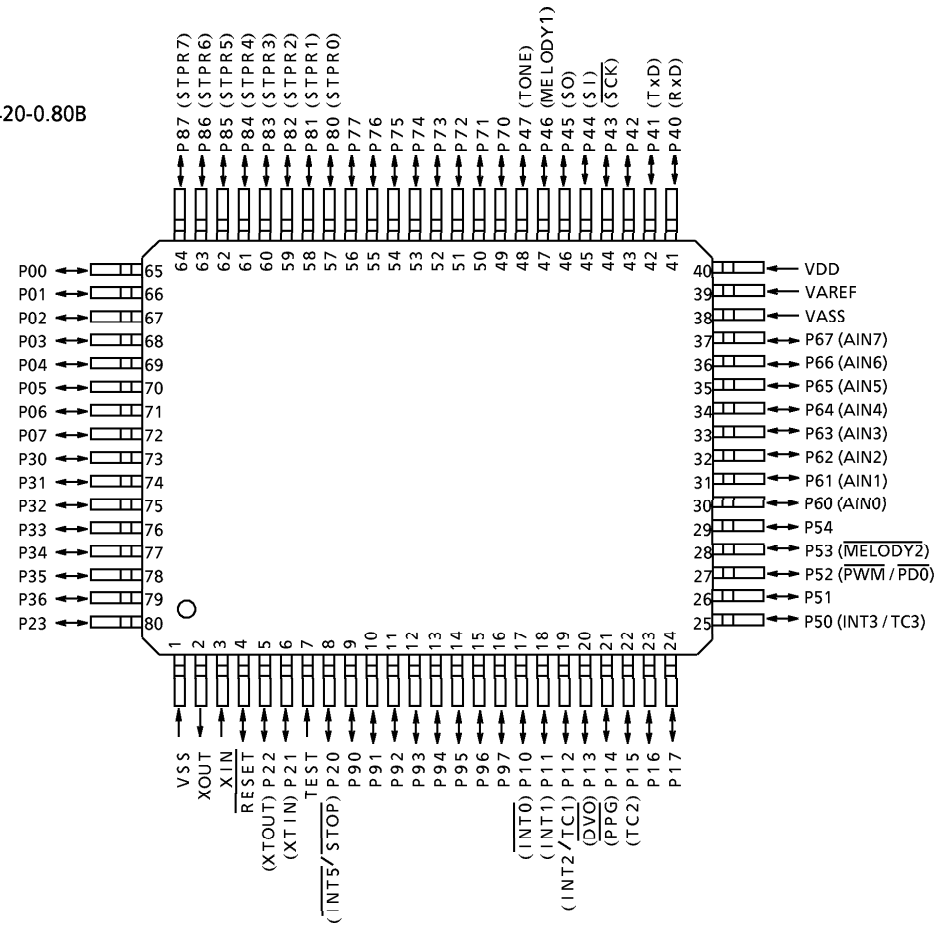
980910EBP1

◆Key on Wake-Up
◆Dual clock operation
◆Internal clock select mode (fc, fc/2, fc/4, fc/8) Initial fc/8 operation
◆Five Power saving operating modes
- STOP mode: Oscillation stops. Battery/Capacitor back-up.
  Port output hold/high-impedance.
- SLOW mode: Low power consumption operation using low-frequency clock (32.768kHz).
- IDLE1 mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- IDLE2 mode: CPU stops, and Peripherals operate using high and low frequency clock. Release by interrupts.
- SLEEP mode: CPU stops, and Peripherals operate using low-frequency clock. Release by interrupts.

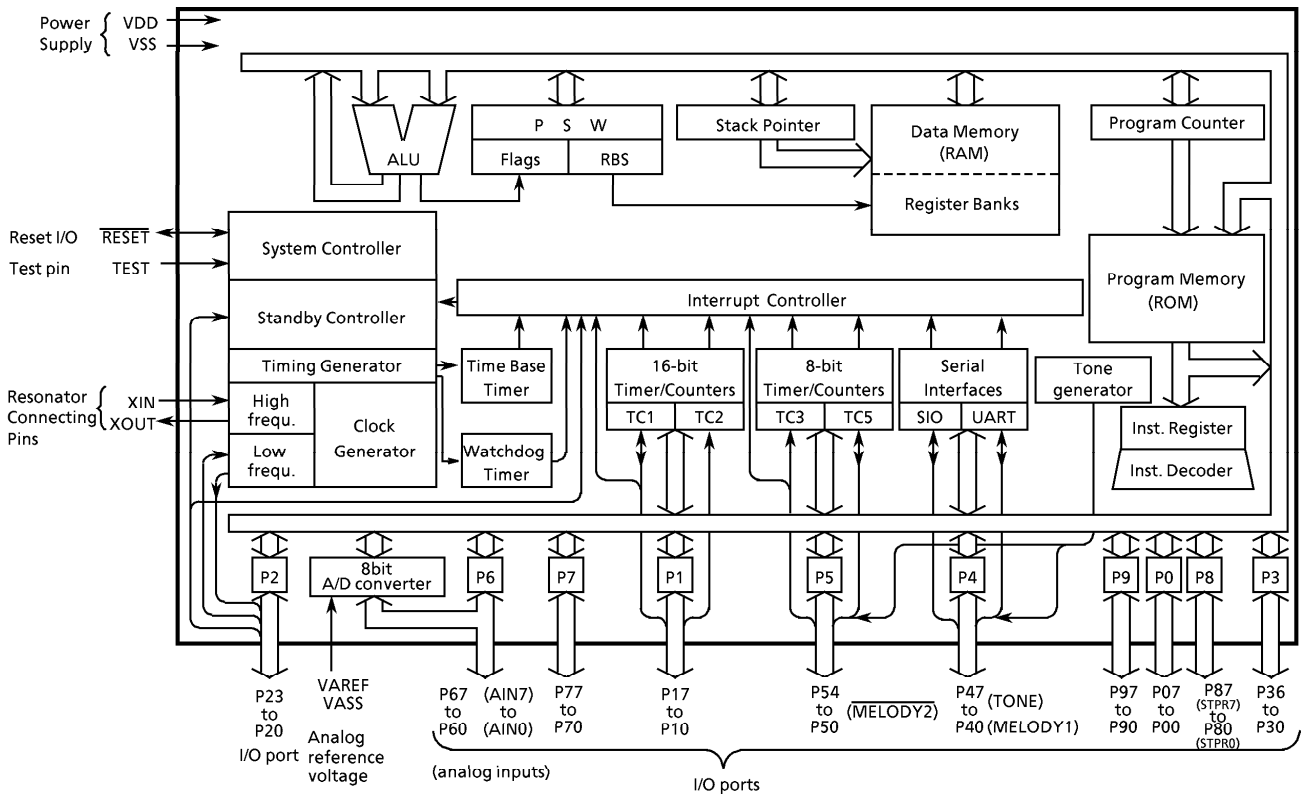
◆Wide operating voltage: 2.2 to 5.5 V at [3.58 MHz] [3.84 MHz] [4.0 MHz] [4.19 MHz] / 32.768 kHz,
4.5 to 5.5 V at 8 MHz / 32.768 kHz
◆Emulation Pod: BM87CM53F0A

Pin Assignments (Top View)

P-QFP80-1420-0.80B



Block Diagram



Pin Function

Pin Name	Input / Output	Function	
P07 to P00	I/O	Two 8-bit programmable input/output ports (tri-state). Each bit of these ports can be individually configured as an input or an output under software control. During reset, all bits are configured as input. When used as a divider output or a PPG output, the latch must be set to "1".	
P17, P16	I/O		
P15 (TC2)	I/O (Input)		Timer/Counter 2 input
P14 ($\overline{\text{PPG}}$)	I/O (Output)		Programmable pulse generator output
P13 ($\overline{\text{DVO}}$)			Divider output
P12 (INT2 / TC1)	I/O (Input)		External interrupt input 2 or Timer/Counter 1 input
P11 (INT1)			External interrupt input 1
P10 ($\overline{\text{INT0}}$)			External interrupt input 0
P23	I/O	4-bit input/output port with latch. When used as an input port, the latch must be set to "1".	
P22 (XTOUT)	I/O (Output)		Resonator connecting pins (32.768kHz). For inputting external clock, XTIN is used and XTOUT is opened.
P21 (XTIN)	I/O (Input)		
P20 ($\overline{\text{INT5}}$/$\overline{\text{STOP}}$)			External interrupt input 5 or STOP mode release signal input
P36 to P30	I/O	7-bit input/output port (high current output) with latch. When used as an input port, the latch must be set to "1".	
P47 (Tone)	I/O (Output)	8-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output or a port option under software control. During reset, all bits are configured as input. When used as an input port or a SIO input/output, the latch must be set to "1".	Tone output
P46 (Melody1)	I/O (Output)		Melody1 output (sine wave)
P45 (SO)	I/O (Output)		SIO serial data output
P44 (SI)	I/O (Input)		SIO serial data input
P43 ($\overline{\text{SCK}}$)	I/O (I/O)		SIO serial clock input/output
P42	I/O		
P41 (TxD)	I/O (Output)		SIO serial data output (asynchronous only)
P40 (RxD)	I/O (Input)		SIO serial data input (asynchronous only)
P54	I/O	5-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output or a port option under software control. During reset, all bits are configured as input. When used as an input port, an external interrupt input, or a $\overline{\text{PWM/PDO}}$ output, the latch must be set to "1".	
P53 ($\overline{\text{Melody2}}$)	I/O (Output)		$\overline{\text{Melody2}}$ output (square wave)
P52 ($\overline{\text{PWM/PDO}}$)	I/O (Output)		8-bit PWM output or 8-bit programmable divider output
P51	I/O		
P50 (INT3/TC3)	I/O (Input)		External interrupt input 3 or Timer/Counter 3 input
P67 (AIN7) to P60 (AIN0)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output under software control.	A/D converter analog inputs
P77 to P70	I/O	8-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output or a port option under software control. During reset, all bits are configured as input.	
P97 to P90	I/O		
P87 (STPR7) to P80 (STPR0)	I/O (Input)	8-bit programmable input/output port (tri-state). Each bit of the port can be individually configured as an input or an output or a pull-up resister under software control. During reset, all bits are configared as an input.	
XIN, XOUT	Input, Output	Resonator connecting pins for high-frequency clock. For inputting external clock, XIN is used and XOUT is opened.	
$\overline{\text{RESET}}$	I/O	Reset signal input or watchdog timer output/address-trap-reset output/system-clock-reset output.	
TEST	Input	Test pin for out-going test. Be tied to low.	
VDD, VSS	Power Supply	+ 5 V, 0 V (GND)	
VAREF, VASS		Analog reference voltage inputs (High, Low)	

OPERATIONAL DESCRIPTION

1. CPU CORE FUNCTIONS

The CPU core consists of a CPU, a system clock controller, an interrupt controller, and a watchdog timer. This section provides a description of the CPU core, the program memory (ROM), the data memory (RAM), and the reset circuit.

1.1 Memory Address Map

The TLCS-870 Series is capable of addressing 64K bytes of memory. Figure 1-1 shows the memory address maps of the 87CM53. In the TLCS-870 Series, the memory is organized 4 address spaces (ROM, RAM, SFR, and DBR). It uses a memory mapped I/O system, and all I/O registers are mapped in the SFR/DBR address spaces. There are 16 banks of general-purpose registers. The register banks are also assigned to the first 128 bytes of the RAM address space.

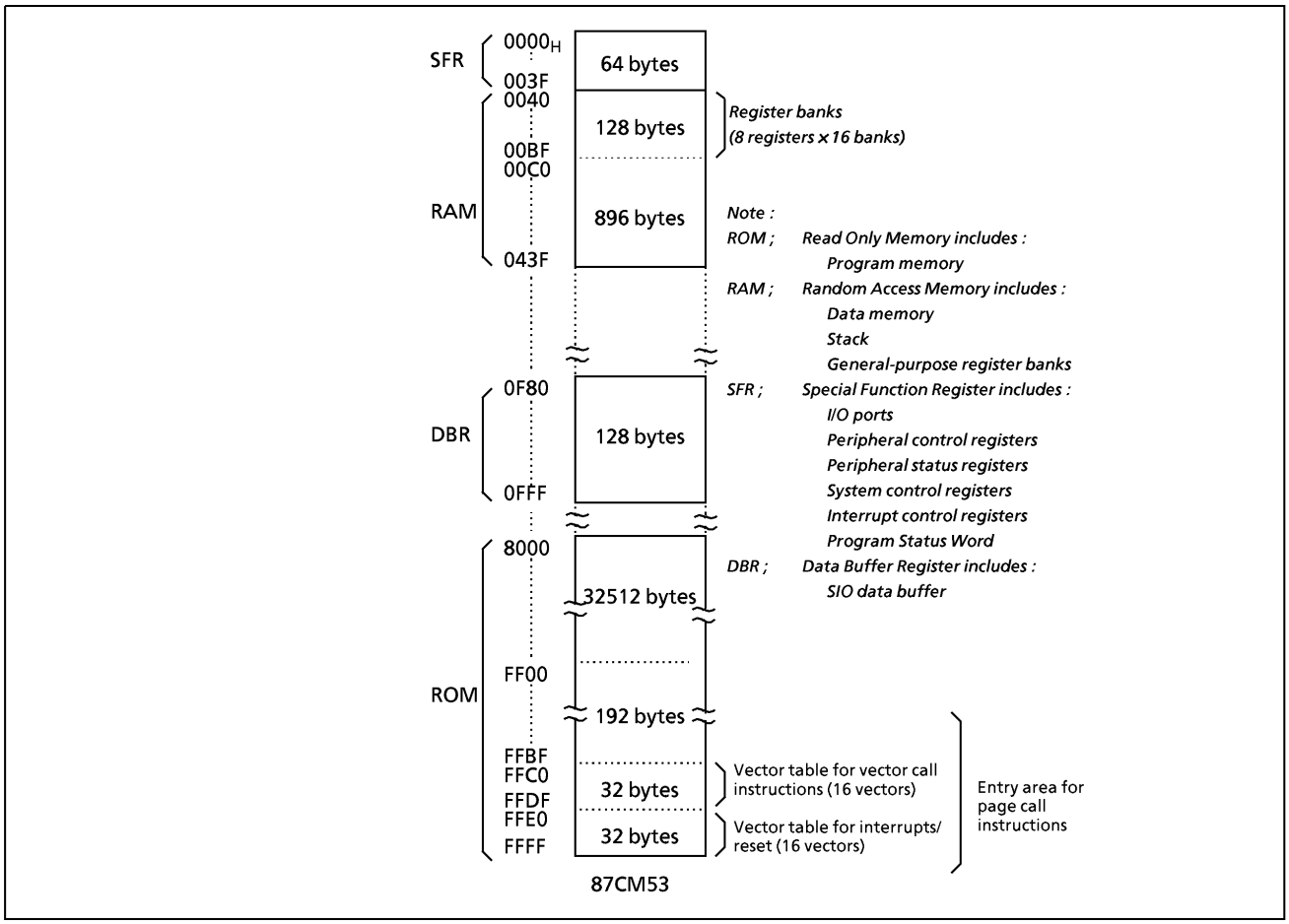


Figure 1-1. Memory Address Maps

Electrical Characteristics

Absolute Maximum Ratings (V_{SS} = 0 V)

Parameter	Symbol	Pins	Ratings	Unit
Supply Voltage	VDD		– 0.3 to 6.5	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}		– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1pin)	I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8, P9	3.2	mA
	I_{OUT2}	Port P3	30	
Output Current (Total)	Σ I_{OUT1}	Ports P0, P1, P2, P4, P5, P6, P7, P8, P9	160	mA
	Σ I_{OUT2}	Port P3	120	
Power Dissipation [Topr = 70°C]	PD		350	mW
Soldering Temperature (time)	Tsld		260 (10s)	°C
Storage Temperature	Tstg		– 55 to 125	°C
Operating Temperature	Topr		– 30 to 60	°C

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended Operating Conditions (V_{SS} = 0 V, Topr = – 30 to 60°C)

Parameter	Symbol	Pins	Conditions		Min	Max	Unit
Supply Voltage	V_{DD}		fc = 8 MHz	NORMAL1, 2 mode	4.5	5.5	V
				IDLE1, 2 mode			
			fc ≦ 4.2 MHz	NORMAL1, 2 mode	2.2 Note 2		
				IDLE1, 2 mode			
			fs = 32.768 kHz	SLOW mode			
				SLEEP mode			
				STOP mode	2.0		
Input High Voltage	V_{IH1}	Except hysteresis input	V_{DD} ≧ 4.5 V		V_{DD} × 0.70	V_{DD}	V
	V_{IH2}	Hysteresis input			V_{DD} × 0.75		
	V_{IH3}		V_{DD} < 4.5 V		V_{DD} × 0.90		
Input Low Voltage	V_{IL1}	Except hysteresis input	V_{DD} ≧ 4.5 V		0	V_{DD} × 0.30	V
	V_{IL2}	Hysteresis input				V_{DD} × 0.25	
	V_{IL3}		V_{DD} < 4.5 V			V_{DD} × 0.10	
Clock Frequency	fc	XIN, XOUT	V_{DD} = 4.5 to 5.5 V		3.58	8.0	MHz
			V_{DD} = 2.7 to 5.5 V			4.19	
	fs	XTIN, XTOUT			30.0	34.0	kHz

Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

Note 2: Clock frequency fc: The supply voltage range of the conditions shows the value in NORMAL1, 2 modes and·IDLE 1,2 modes.

Note 3: When the A/D converter is used, VDD must be set to ≧ 2.7 V.

D.C. Characteristics

(V_{SS} = 0 V, Topr = – 30 to 60°C)

Parameter	Symbol	Pins	Conditions		Min	Typ.	Max	Unit
Hysteresis Voltage	V_{HS}	Hysteresis input			–	0.9	–	V
Input Current	I_{IN1}	TEST	V_{DD} = 5.5 V V_{IN} = 5.5 V / 0 V		–	–	± 2	μA
	I_{IN2}	Sink open drain port and tri-state port						
	I_{IN3}	$\overline{RESET}$, $\overline{STOP}$						
Input Resistance	R_{IN2}	$\overline{RESET}$			100	220	450	kΩ
	R_{IN}	P8 pull-up resistor			30	70	150	
Output Leakage Current	I_{LO}	Sink open drain port and tri-state port	V_{DD} = 5.5 V, V_{OUT} = 5.5 V		–	–	2	μA
Output High Voltage	V_{OH2}	Tri-state port	V_{DD} = 4.5 V, I_{OH} = – 0.7 mA		4.1	–	–	V
Output Low Voltage	V_{OL}	Except XOUT and P3	V_{DD} = 4.5 V, I_{OL} = 1.6 mA		–	–	0.4	V
Output Low Current	I_{OL3}	Port P3	V_{DD} = 4.5 V, V_{OL} = 1.0 V		–	20	–	mA
Supply Current in NORMAL 1, 2 mode	I_{DD}		V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V fc = 8 MHz fs = 32.768 kHz	TONE no output	–	9	12	mA
				TONE output	–	10.5	13.5	
Supply Currnt in IDLE 1, 2 mode				TONE no output	–	4.5	6.5	
				TONE output	–	6.0	8.0	
Supply Currnt in NORMAL 1, 2 mode			V_{DD} = 2.2 V V_{IN} = 2.2 V / 0.2 V fc = 4.2 MHz fs = 32.768 kHz	TONE no output	–	1.5	2.5	
				TONE output	–	2.0	3.0	
Supply Currnt in IDLE 1, 2 mode				TONE no output	–	0.8	1.8	
				TONE output	–	1.3	2.3	
Supply Current in SLOW mode	I_{DD}		V_{DD} = 3.0 V V_{IN} = 2.8 V / 0.2 V fs = 32.768 kHz		–	30	60	μA
Supply Current in SLEEP mode					–	15	30	μA
Supply Current in STOP mode			V_{DD} = 5.5 V V_{IN} = 5.3 V / 0.2 V			0.5	10	μA

Note 1: Typical values show those at Topr = 25°C, V_{DD} = 5 V.
Note 2: Input current: The current through pull-up or pull-down resistor is not included.

A/D Conversion Characteristics

(V_{SS} = 0 V, V_{DD} = 2.7 to 5.5 V, Topr = – 30 to 60°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Analog Reference Voltage	V_{AREF}	$V_{AREF} - V_{ASS} \geqq 2.5$ V	2.7	—	V_{DD}	V
	V_{ASS}		V_{SS}	—	1.5	
Analog Input Voltage	V_{AIN}	$V_{DD} = V_{AREF}$ = 5.0 V $V_{SS} = V_{ASS}$ = 0.0 V	V_{ASS}	—	V_{AREF}	V
Analog Supply Current	I_{REF}		—	0.5	1.0	V
Nonlinearity Error		V_{DD} = 2.7 to 5.5 V	—	—	± 1	mA
Zero Point Error		V_{SS} = 0.0 V	—	—	± 1	
Full Scale Error		V_{AREF} = 2.700 V, 5.000 V	—	—	± 1	LSB
Total Error		V_{ASS} = 0.000 V	—	—	± 2	

Note: Total Error = total number of each type error excluding guantization error.

Tone Output Characteristics

(V_{SS} = 0 V, V_{DD} = 2.2 to 5.5 V, Topr = – 30 to 60°C)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Tone Output Voltage (ROW)	V_{TONE}	RL ≧ 10 kΩ, V_{DD} = 2.2 V	126	150	178	mVrms
Pre-Emphasis High Band (COL / ROW)	PEHB	PEHB = 20 log (COL /ROW)	1	2	3	dB
Output Distortion	DIS		—	—	5	%
Frequency Stability	△f	fc = 3.84 MHz, 4.00 MHz, 8.00 MHz (Except error of osc. frequency)	—	—	0.7	%
		fc = 3.58 MHz (Except error of osc. frequency)	—	—	0.66	
		fc = 4.19 MHz (Except error of osc. frequency)	—	—	0.93	

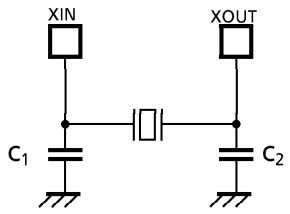
A.C. Characteristics

(V_{SS} = 0 V, Topr = – 40 to 85°C)

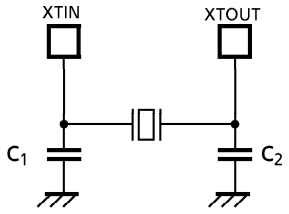
Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Machine Cycle Time	tcy	In NORMAL1, 2 mode (gear ratio)	0.5 (1/1)	–	8.9(1/8)	μs
		In IDLE1, 2 mode (gear ratio)				
		In SLOW mode	117.6		133.3	
		In SLEEP mode				
High Level Clock Pulse Width	t_{WCH}	For external clock operation (XIN input) fc = 8 MHz	50	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
High Level Clock Pulse Width	t_{WSH}	For external clock operation (XTIN input) fs = 32.768 kHz	14.7	–	–	μs
Low Level Clock Pulse Width	t_{WSL}					

Recommended Oscillating Condition

Parameter	Oscillator	Frequency	Recommended Oscillator		Recommended Condition C_1	Recommended Condition C_2
High-frequency	Ceramic Resonator	8 MHz	KYOCERA	KBR8.0M	30 pF	30 pF
		4 MHz	KYOCERA	KBR4.0MS		
			MURATA	CSA4.00MG		
	Crystal Oscillator	8 MHz	TOYOCOM	210B 8.0000	20 pF	20 pF
		4 MHz	TOYOCOM	204B 4.0000		
Low-frequency	Crystal Oscillator	32.768 kHz	NDK	MX-38T	15 pF	15 pF



(1) High-frequency



(2) Low-frequency

Note: When it is used in high electrical field, an electrical shield of the package is recommended to retain normal operations

Note: To obtain an accurate oscillating frequency the condenser capacity must be adjusted on the set.