

TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/H Series

TMP95PW64

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, "Points of Note and Restrictions".
Especially, take care below cautions.

****CAUTION****

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of X1) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficulty. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontrollers

TMP95PW64F

1. Outline and Features

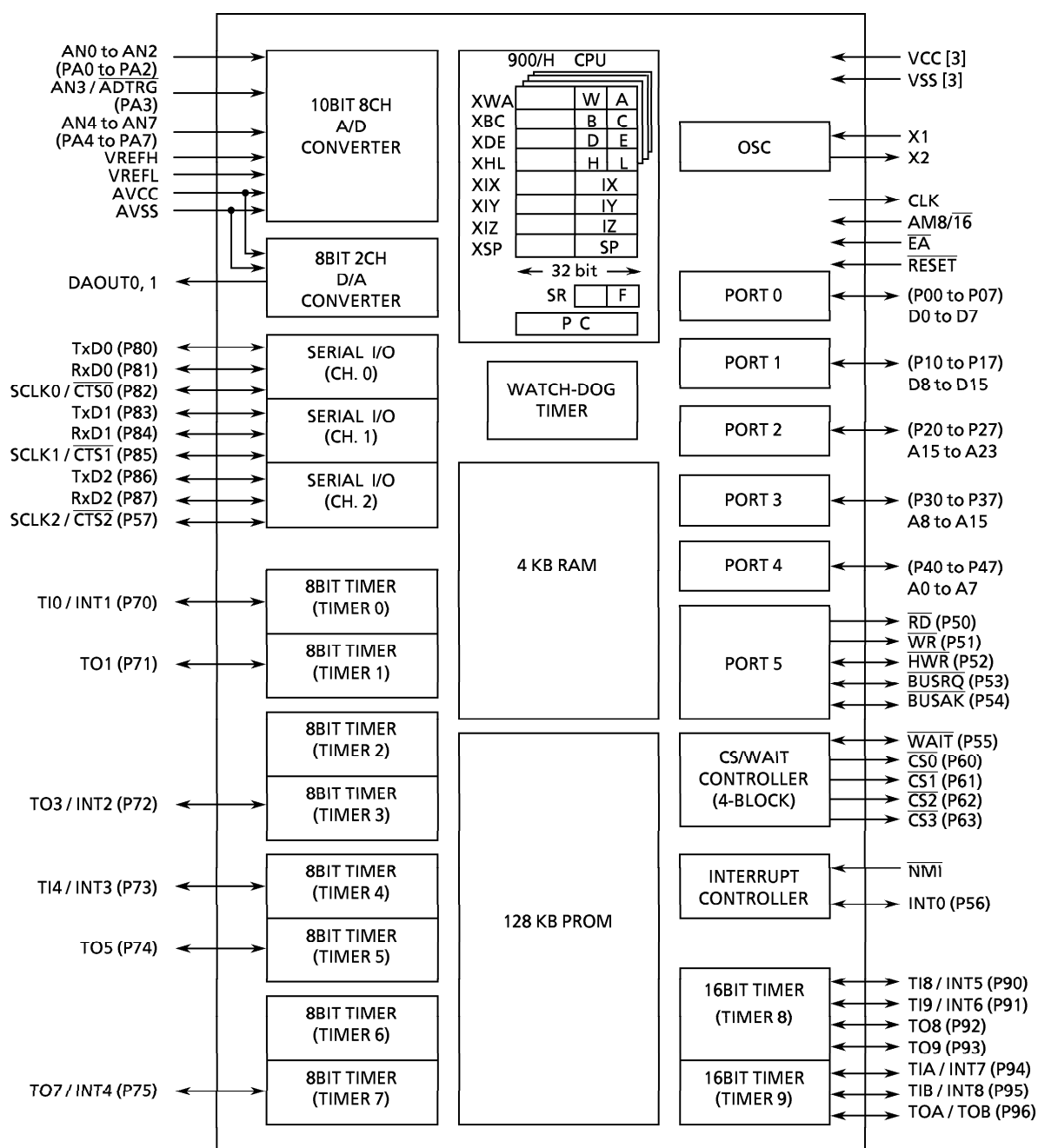
TMP95PW64 is an LSI for TMP95CW64 system evaluation. TMP95PW64 incorporates a 128K-byte one-time PROM. With an adapter socket, the user can write/verify data in the TMP95PW64's PROM using a general-purpose EPROM writer.

TMP95PW64 is pin-compatible with TMP95CW64, which incorporates a mask ROM. To achieve the same operations as TMP95CW64, write program data to the internal PROM.

Product Name	ROM	RAM	Package	Adapter Socket
TMP95PW64F	OTP 128 Kbyte	4 Kbyte	P-LQFP100-1414-0.50F	BM11129

000707EBP1

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Note: After a reset, functions in parentheses () are selected for the shared pins.

Figure 1 TMP95PW64 Block Diagram

2. Pin Assignment and Pin Functions

This section shows the TMP95PW64F pin assignment, and the names and an outline of the functions of the input/output pins.

2.1 Pin Assignment Diagram

Figure 2.1 is a pin assignment diagram for TMP95PW64F.

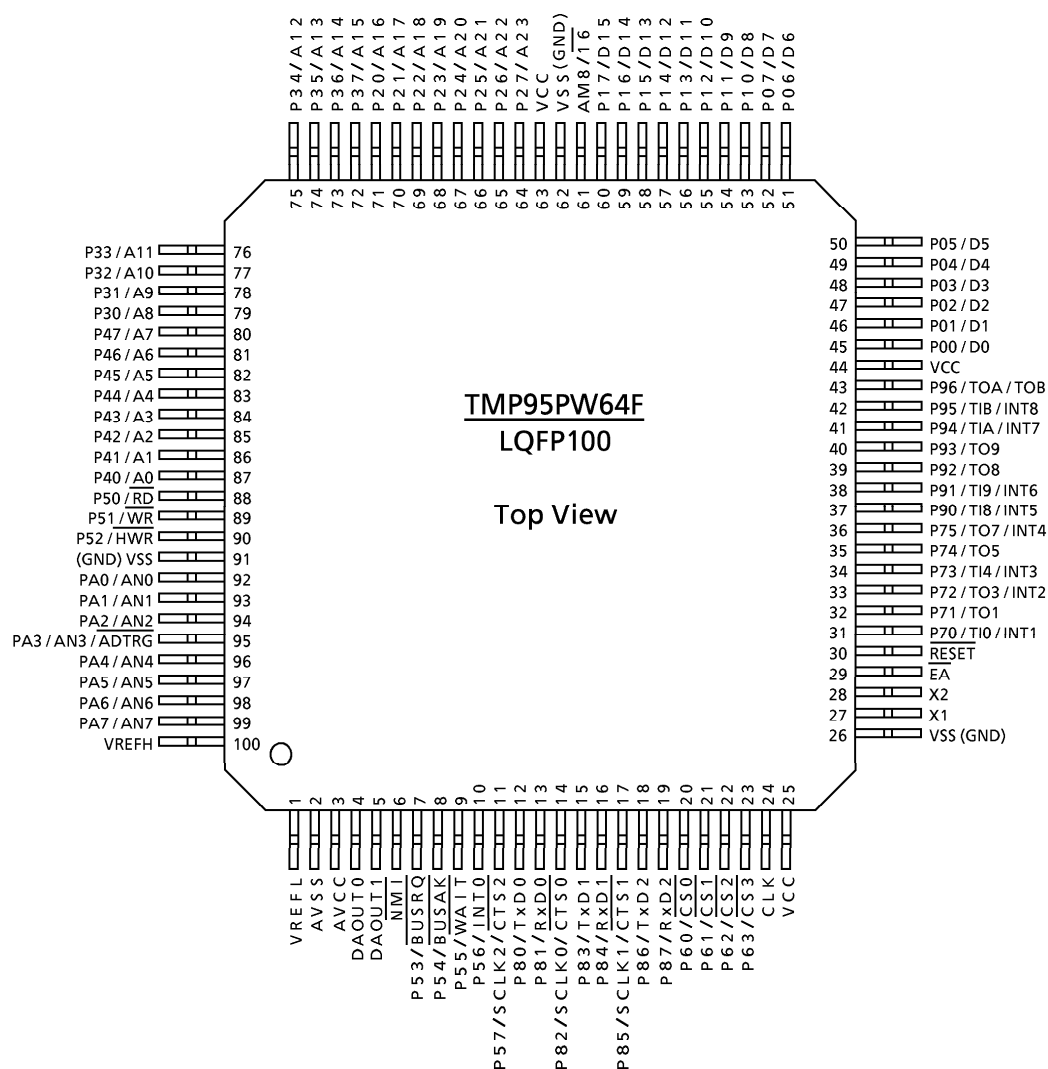


Figure 2.1 Pin Allocation Diagram (100-Pin LQFP)

2.2 Pin Names and Functions

TMP95PW64 has an MCU mode and a PROM mode.

(1) Pin Names and Functions in MCU Mode

Table 2.2 (1) lists the names and functions of the input/output pins.

Table 2.2 Pin Names and Functions (1/4)

Pin Name	Number of Pins	Input/Output	Function
P00 to P07 / D0 to D7	8	Input/output	Port 0: I/O port. Input or output specifiable in units of bits
		Input/output	Data: Data bus 0 to 7
P10 to P17 / D8 to D15	8	Input/output	Port 1: I/O port. Input or output specifiable in units of bits
		Input/output	Data: Data bus 8 to 15
P20 to P27 / A16 to A23	8	Input/output	Port 2: I/O port. Input or output specifiable in units of bits
		Output	Address: Address bus 16 to 23
P30 to P37 / A8 to A15	8	Input/output	Port 3: I/O port. Input or output specifiable in units of bits
		Output	Address: Address bus 8 to 15
P40 to P47 / A0 to A7	8	Input/output	Port 4: I/O port. Input or output specifiable in units of bits
		Output	Address: Address bus 0 to 7
P50 / $\overline{RD}$	1	Output	Port 50: Output-only port
		Output	Read: Outputs strobe signal to read external memory (setting P5 <P50> = 0 and P5FC <P50F> = 1 outputs strobe signal at all read timings)
P51 / $\overline{WR}$	1	Output	Port 51: Output-only port.
		Output	Write: Outputs strobe signal to write data on pins D0 to D7
P52 / $\overline{HWR}$	1	Input/output	Port 52: I/O port (with built-in pull-up resistor)
		Output	Upper write: Outputs strobe signal to write data on pins D8 to D15
P53 / $\overline{BUSRQ}$	1	Input/output	Port 53: I/O port (with built-in pull-up resistor)
		Input	Bus request: Input pin to request external bus release
P54 / $\overline{BUSAK}$	1	Input/output	Port 54: I/O port (with built-in pull-up resistor)
		Output	Bus acknowledge: Output pin to acknowledge that CPU received $\overline{BUSRQ}$ and released external bus.
P55 / $\overline{WAIT}$	1	Input/output	Port 55: I/O port (with built-in pull up resistor)
		Input	Wait: Buswait request pin for CPU (Effective when 1 + N WAIT mode, or 0 + N WAIT mode. Set using chipselect/wait control register.)
P56 / INT0	1	Input/output	Port 56: I/O port (with built-in pull-up resistor)
		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge. 

Table 2.2 Pin Names and Functions (2/4)

Pin Name	Number of Pins	Input/Output	Function
P57 / SCLK2 / $\overline{\text{CTS2}}$	1	Input/output	Port 57: I/O port (with built-in pull-up resistor)
		Input/output	Serial clock input/output 2
		Input	Serial data ready to send 2 (Clear-to-send)
P60 / $\overline{\text{CS0}}$	1	Output	Port 60: Output-only port
		Output	Chip select 0: Outputs 0 if address is within specified address range
P61 / $\overline{\text{CS1}}$	1	Output	Port 61: Output-only port
		Output	Chip select 1: Outputs 0 if address is within specified address range
P62 / $\overline{\text{CS2}}$	1	Output	Port 62: Output-only port
		Output	Chip select 2: Outputs 0 if address is within specified address range
P63 / $\overline{\text{CS3}}$	1	Output	Port 63: Output-only port
		Output	Chip select 3: Outputs 0 if address is within specified address range
P70 / TI0 / INT1	1	Input/output	Port 70: I/O port
		Input	Timer input 0: Input pin for timer 0
		Input	Interrupt request pin 1: Rising-edge interrupt request pin 
P71 / TO1	1	Input/output	Port 71: I/O port.
		Output	Timer output 1: Output pin for timer 0 or 1
P72 / TO3 / INT2	1	Input/output	Port 72: I/O port
		Output	Timer output 3: Output pin for timer 2 or 3
		Input	Interrupt request pin 2: Rising-edge interrupt request pin 
P73 / TI4 / INT3	1	Input/output	Port 73: I/O port
		Input	Timer input 4: Input pin for timer 4
		Input	Interrupt request pin 3: Rising-edge interrupt request pin 
P74 / TO5	1	Input/output	Port 74: I/O port
		Output	Timer output 5: Output pin for timer 4 or 5
P75 / TO7 / INT4	1	Input/output	Port 75: I/O port
		Output	Timer output 7: Output pin for timer 6 or 7
		Input	Interrupt request pin 4: Rising-edge interrupt request pin 
P80 / TxD0	1	Input/output	Port 80: I/O port (with built-in pull-up resistor)
		Output	Serial transmission data 0
P81 / RxD0	1	Input/output	Port 81: I/O port (with built-in pull-up resistor)
		Input	Serial receive data 0
P82 / SCLK0 / $\overline{\text{CTS0}}$	1	Input/output	Port 82: I/O port (with built-in pull-up resistor)
		Input/output	Serial clock input/output 0
		Input	Serial data ready to send 0 (Clear-to-send)

Table 2.2 Pin Names and Functions (3/4)

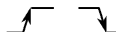
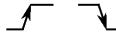
Pin Name	Number of Pins	Input/Output	Function
P83 / TxD1	1	Input/output	Port 83: I/O port (with built-in pull-up resistor)
		Output	Serial transmission data 1
P84 / RxD1	1	Input/output	Port 84: I/O port (with built-in pull-up resistor)
		Input	Serial receive data 1
P85 / SCLK1 / $\overline{\text{CTS1}}$	1	Input/output	Port 85: I/O port (with built-in pull-up resistor)
		Input/output	Serial clock input/output 1
		Input	Serial data ready to send 1 (Clear-to-send)
P86 / TxD2	1	Input/output	Port 86: I/O port (with built-in pull-up resistor)
		Output	Serial transmission data 2
P87 / RxD2	1	Input/output	Port 87: I/O port (with built-in pull-up resistor)
		Input	Serial receive data 2
P90 / TI8 / INT5	1	Input/output	Port 90: I/O port
		Input	Timer input 8: Input pin for timer 8
		Input	Interrupt request pin 5: Interrupt request pin with programmable rising/falling edge 
P91 / TI9 / INT6	1	Input/output	Port 91: I/O port
		Input	Timer input 9: Input pin for timer 8
		Input	Interrupt request pin 6: Rising edge interrupt request pin 
P92 / TO8	1	Input/output	Port 92: I/O port
		Output	Timer output 8: Output pin for timer 8
P93 / TO9	1	Input/output	Port 93: I/O port
		Output	Timer output 9: Output pin for timer 8
P94 / TIA / INT7	1	Input/output	Port 94: I/O port
		Input	Timer input A: Input pin for timer 9
		Input	Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge 
P95 / TIB / INT8	1	Input/output	Port 95: I/O port
		Input	Timer input B: Input pin for timer 9
		Input	Interrupt request pin 8: Rising edge interrupt request pin 
P96 / TOA / TOB	1	Input/output	Port 96: I/O port
		Output	Timer input A: Output pin for timer 9
		Output	Timer input B: Output pin for timer 9
PA0 to PA2 / AN0 to AN2	3	Input	Port A0 to A2: Input-only port
		Input	Analog input 0 to 2: A/D converter input pins
PA3 / AN3 / $\overline{\text{ADTRG}}$	1	Input	Port A3: Input-only port
		Input	Analog input 3: A/D converter input pin
		Input	External start trigger

Table 2.2 Pin Names and Functions (4/4)

Pin Name	Number of Pins	Input/Output	Function
PA4 to PA7 / AN4 to AN7	4	Input	Port A4 to A7: Input-only port
		Input	Analog input 4 to 7: A/D converter input pins
DAOUT0	1	Output	D/A output 0: D/A converter 0 output pin
DAOUT1	1	Output	D/A output 1: D/A converter 1 output pin
NMI	1	Input	Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both falling and rising edge 
CLK	1	Output	Clock output: Outputs external clock divided by 4. Pulled up during reset.
EA	1	Input	External access: Connect to VCC.
AM8 / $\overline{16}$	1	Input	Address mode: External data bus width select pin Connect this pin to VCC. Data bus width at external access can be set by chip select/wait control register.
RESET	1	Input	Reset: Initializes TMP95PW64 (with built-in pull-up resistor)
VREFH	1	Input	Reference voltage input pin for A/D converter (high)
VREFL	1	Input	Reference voltage input pin for A/D converter (low)
AVCC	1		Power supply pin for A/D converter and reference voltage input pin for D/A converter: Connect to power supply
AVSS	1		GND pin for A/D converter and reference voltage input pin for D/A converter: Connect to GND
X1 / X2	2	Input/output	Oscillator connecting pin
VCC	3		Collector supply pin: Connect all VCC pins to power supply
VSS	3		GND pin: Connect all VSS pins to GND (0 V)

Note: Software can be used to turn off the resistance of pull-up pins with resistors (except for the RESET pin).

(2) PROM Mode Pin Functions and Pin Processing

Tables 2.2 (2) and (3) show the names and functions of the input/output pins, and the pin processing.

Table 2.2 (2) Pin Names and Functions

Pin Function Name	Number of Pins	Input/Output	Function	Pin Name (In MCU Mode)
A7 to A0	8	Input	Program memory address input	P20 to P27
A15 to A8	8			P17 to P10
A16	1			P34
D7 to D0	8	Input/output	Program memory data input/output	P07 to P00
$\overline{CE}$	1	Input	Chip enable input	P35
$\overline{OE}$	1	Input	Output control input	P37
PGM	1	Input	Program control input	P36
VPP	1	Power supply	12.75 V / 5 V (program power supply)	$\overline{EA}$
VCC	4	Power supply	6.25 V / 5 V	VCC, AVCC
VSS	4	Power supply	0 V	VSS, AVSS

Table 2.2 (3) Pin Names and Pin Processing

Pin Name	Number of Pins	Input/Output	Pin Processing
P33	1	Input	Fixed to low level (SECURITY pin)
RESET	1	Input	Fixed to low level (set to PROM mode)
CLK	1	Input	
X1	1	Input	Connect oscillator and set to self-oscillation
X2	1	Output	
P32 to P30 P47 to P40 P57 to P52 P75 to P70 P87 to P80 P96 to P90 PA7 to PA0 AM8/16 NMI	48	Input	Fixed to high level
P51 to P50 P63 to P60	6	Output	Open
VREFH	1	Input	
VREFL	1		

3. Operation

The following describes the structure and operation of the TMP95PW64 hardware.

In TMP95PW64, the internal ROM of TMP95CW64 is replaced by an internal PROM. Otherwise, TMP95PW64 is structurally and operationally identical to TMP95CW64. Accordingly, for functions not described here, see the TMP95CW64 section of the manual. TMP95PW64 supports MCU operating mode and PROM operating mode.

3.1 MCU Mode

(1) Setting and Function

Opening the CLK pin (setting to output) sets MCU mode.

In MCU mode, TMP95PW64 operates the same as TMP95CW64.

(2) Memory Map

Figure 3.1 shows the memory map in MCU mode and the CPU access area in each addressing mode.

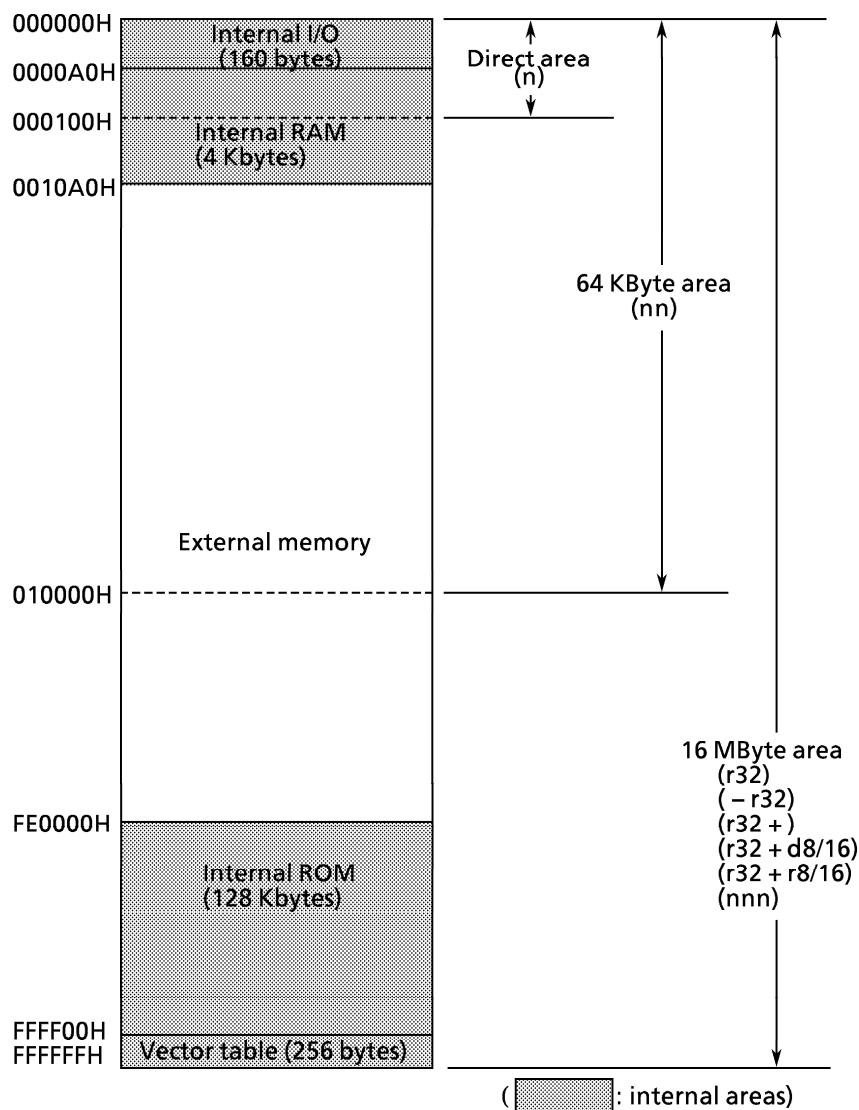


Figure 3.1 TMP95PW64 Memory Map

(2) Memory Map

The internal PROM addresses in PROM mode are 0000H to 1FFFFH. These correspond to MCU mode addresses FE0000H to FFFFFFFH.

Figure 3.2 (2) shows a comparison of the MCU and PROM mode memory maps.

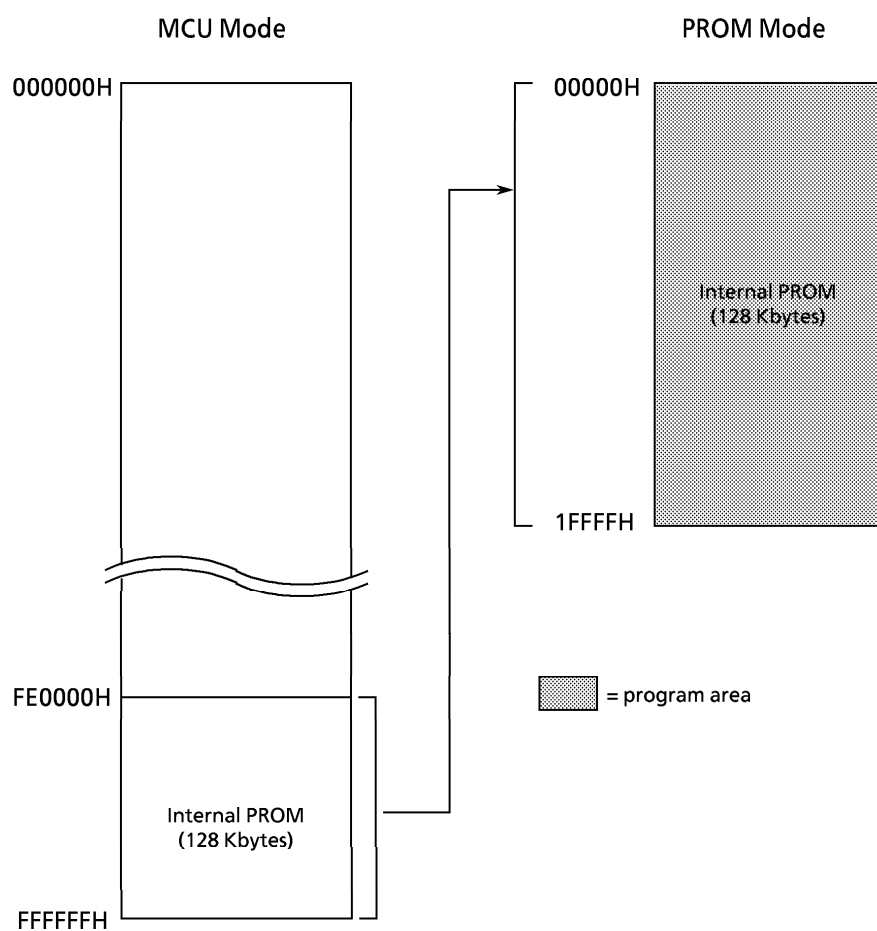


Figure 3.2 (2) Memory Map Comparison

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 6.5	V
Input Voltage	V_{IN}	except for $\overline{EA}$ pin	– 0.5 to $V_{CC} + 0.5$
		$\overline{EA}$ pin	– 0.5 to 14.0
Output current (total)	ΣI_{OL}	+ 120	mA
Output current (total)	ΣI_{OH}	– 120	mA
Power Dissipation ($T_a = + 70^\circ\text{C}$)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	+ 260	$^\circ\text{C}$
Storage Temperature	T_{STG}	– 65 to + 150	$^\circ\text{C}$
Operating Temperature	T_{OPR}	– 20 to + 70	$^\circ\text{C}$

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Electrical Characteristics

- (1) $V_{CC} = + 5\text{ V} \pm 10\%$, $T_a = - 20$ to $+ 70^\circ\text{C}$ ($f_c = 8$ to 25 MHz)

(Typical values are for $T_a = + 25^\circ\text{C}$, $V_{CC} = + 5\text{ V}$.)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8/16 X1	V_{IL}		– 0.3	0.8	V
	V_{IL1}		– 0.3	0.3 V_{CC}	V
	V_{IL2}		– 0.3	0.25 V_{CC}	V
	V_{IL3}		– 0.3	0.3	V
	V_{IL4}		– 0.3	0.2 V_{CC}	V
Input High Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75) RESET, NMI, INT0 to 4 EA, AM8/16 X1	V_{IH}		2.2	$V_{CC} + 0.3$	V
	V_{IH1}		0.7 V_{CC}	$V_{CC} + 0.3$	V
	V_{IH2}		0.75 V_{CC}	$V_{CC} + 0.3$	V
	V_{IH3}		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
	V_{IH4}		0.8 V_{CC}	$V_{CC} + 0.3$	V
Output Low Voltage	V_{OL}	$I_{OL} = 1.6\text{ mA}$		0.45	V
Output High Voltage	V_{OH}	$I_{OH} = - 400\text{ }\mu\text{A}$	2.4		V
	V_{OH1}	$I_{OH} = - 100\text{ }\mu\text{A}$	0.75 V_{CC}		V
	V_{OH2}	$I_{OH} = - 20\text{ }\mu\text{A}$	0.9 V_{CC}		V
Darlington Drive Current (8 Output Pins max.)	I_{DAR}	$V_{EXT} = 1.5\text{ V}$ $R_{EXT} = 1.1\text{ k}\Omega$	– 1.0	– 3.5	mA
Input Leakage Current	I_{LI}	$0.0 \leq V_{in} \leq V_{CC}$	0.02 (Typ)	± 5	μA
Output Leakage Current	I_{LO}	$0.2 \leq V_{in} \leq V_{CC} - 0.2$	0.05 (Typ)	± 10	μA
Operating Current (RUN) IDLE2 IDLE1 STOP ($T_a = - 20$ to $+ 70^\circ\text{C}$) STOP ($T_a = 0$ to $+ 50^\circ\text{C}$)	I_{CC}	$f_c = 25\text{ MHz}$	40 (Typ)	50	mA
			30 (Typ)	40	mA
			3.5 (Typ)	10	mA
			0.5 (Typ)	50	μA
	I_{CC}	$0.2 \leq V_{in} \leq V_{CC} - 0.2$ $0.2 \leq V_{in} \leq V_{CC} - 0.2$		10	μA
Power Down Voltage (@STOP, RAM Back up)	V_{STOP}	$V_{IL2} = 0.2\text{ V}_{CC}$, $V_{IH2} = 0.8\text{ V}_{CC}$	2.0	6.0	V
Pull Up Resistance	R_{RP}		45	160	$\text{k}\Omega$
Pin Capacitance	C_{IO}	$f_c = 1\text{ MHz}$		10	pF
Schmitt Width RESET, NMI, INT0 to 4	V_{TH}		0.4	1.0 (Typ)	V

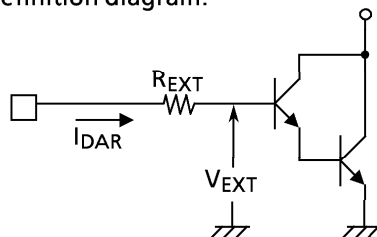
Note: I_{DAR} guarantees up to eight pins from any output port.

(2) $V_{CC} = +3\text{ V} \pm 10\%$, $T_a = -20$ to $+70^\circ\text{C}$ ($f_c = 4$ to 10 MHz)

(Typical values are for $T_a = +25^\circ\text{C}$, $V_{CC} = +3\text{ V}$.)

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Low Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75)	V_{IL} V_{IL1}		-0.3 -0.3	0.6 $0.3 V_{CC}$	V V
RESET, NMI, INT0 to 4	V_{IL2}		-0.3	$0.25 V_{CC}$	V
EA, AM8/16	V_{IL3}		-0.3	0.3	V
X1	V_{IL4}		-0.3	$0.2 V_{CC}$	V
Input High Voltage (D0 to 15) Port 2 to A (except P56, P70, P72, P73, P75)	V_{IH} V_{IH1}		2.0 $0.7 V_{CC}$	$V_{CC} + 0.3$ $V_{CC} + 0.3$	V V
RESET, NMI, INT0 to 4	V_{IH2}		$0.75 V_{CC}$	$V_{CC} + 0.3$	V
EA, AM8/16	V_{IH3}		$V_{CC} - 0.3$	$V_{CC} + 0.3$	V
X1	V_{IH4}		$0.8 V_{CC}$	$V_{CC} + 0.3$	V
Output Low Voltage	V_{OL}	$I_{OL} = 1.6\text{ mA}$		0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	2.4		V
Input Leakage Current	I_{LI}	$0.0 \leq V_{in} \leq V_{CC}$	0.02 (Typ)	± 5	μA
Output Leakage Current	I_{LO}	$0.2 \leq V_{in} \leq V_{CC} - 0.2$	0.05 (Typ)	± 10	μA
Operating Current (RUN)	I_{CC}	$f_c = 10\text{ MHz}$	12 (Typ)	25	mA
IDLE2			4.5 (Typ)	17	mA
IDLE1			0.8 (Typ)	5	mA
STOP ($T_a = -20$ to $+70^\circ\text{C}$)		$0.2 \leq V_{in} \leq V_{CC} - 0.2$	0.5 (Typ)	50	μA
STOP ($T_a = 0$ to $+50^\circ\text{C}$)		$0.2 \leq V_{in} \leq V_{CC} - 0.2$		10	μA
Power Down Voltage (@ STOP, RAM Back up)	V_{STOP}	$V_{IL2} = 0.2 V_{CC}$, $V_{IH2} = 0.8 V_{CC}$	2.0	6.0	V
Pull Up Registance	R_{RP}		70	400	$\text{k}\Omega$
Pin Capacitance	C_{IO}	$f_c = 1\text{ MHz}$		10	pF
Schmitt Width RESET, NMI, INT0 to 4	V_{TH}		0.4	1.0 (Typ)	V

Refer: I_{DAR} definition diagram.



4.3 AC Electrical Characteristics

(1) $V_{CC} = +5\text{ V} \pm 10\%$, $T_a = -20$ to $+70^\circ\text{C}$

(fc = 8 MHz to 25 MHz)

No.	Parameter	Symbol	Formula		20 MHz		25 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Oscillation cycle (= x)	t_{OSC}	40	125	50		40		ns
2	Clock pulse width	t_{CLK}	$2.0x - 40$		60		40		ns
3	A0 to 23 valid $\rightarrow$ Clock hold	t_{AK}	$0.5x - 20$		5		0		ns
4	Clock valid $\rightarrow$ A0 to 23 hold	t_{KA}	$1.5x - 60$		15		0		ns
5	A0 to 23 valid $\rightarrow$ $\overline{RD}/\overline{WR}$ fall	t_{AC}	$1.0x - 20$		30		20		ns
6	$\overline{RD}/\overline{WR}$ rise $\rightarrow$ A0 to 23 hold	t_{CA}	$0.5x - 20$		5		0		ns
7	A0 to 23 valid $\rightarrow$ D0 to 15 input	t_{AD}		$3.5x - 40$		135		100	ns
8	$\overline{RD}$ fall $\rightarrow$ D0 to 15 input	t_{RD}		$2.5x - 45$		80		55	ns
9	$\overline{RD}$ low pulse width	t_{RR}	$2.5x - 40$		85		60		ns
10	$\overline{RD}$ rise $\rightarrow$ D0 to 15 hold	t_{HR}	0		0		0		ns
11	$\overline{WR}$ low pulse width	t_{WW}	$2.5x - 40$		85		60		ns
12	D0 to 15 valid $\rightarrow$ $\overline{WR}$ rise	t_{DW}	$2.0x - 40$		60		40		ns
13	$\overline{WR}$ rise $\rightarrow$ D0 to 15 hold	t_{WD}	$0.5x - 10$		15		10		ns
14	A0 to 23 valid $\rightarrow$ $\overline{WAIT}$ input $\left(\begin{smallmatrix} 1 \\ +n \end{smallmatrix} \text{ WAIT mode}\right)$	t_{AW}		$3.5x - 90$		85		50	ns
	A0 to 23 valid $\rightarrow$ $\overline{WAIT}$ input $\left(\begin{smallmatrix} 0 \\ +n \end{smallmatrix} \text{ WAIT mode}\right)$	t_{AW}		$1.5x - 40$		35		20	ns
15	$\overline{RD}/\overline{WR}$ fall $\rightarrow$ $\overline{WAIT}$ hold $\left(\begin{smallmatrix} 1 \\ +n \end{smallmatrix} \text{ WAIT mode}\right)$	t_{CW}	$2.5x + 0$		125		100		ns
	$\overline{RD}/\overline{WR}$ fall $\rightarrow$ $\overline{WAIT}$ hold $\left(\begin{smallmatrix} 0 \\ +n \end{smallmatrix} \text{ WAIT mode}\right)$	t_{CW}	$0.5x + 0$		25		20		ns
16	$\overline{WR}$ rise $\rightarrow$ PORT valid	t_{CP}		200		200		200	ns
17	$\overline{CS}$ Low pulse width (PSRAM mode)	t_{CE}	$3.0x - 40$		110		80		ns
18	$\overline{CS}$ fall $\rightarrow$ D0 to 15 input (PSRAM mode)	t_{CEA}		$3.0x - 60$		90		60	ns
19	Address setup time (PSRAM mode)	t_{PASC}	$0.5x - 15$		10		5		ns
20	$\overline{CS}$ precharge time (PSRAM mode)	t_{PP}	$1.0x - 10$		40		30		ns

AC measuring conditions

- Output level: High 2.2 V / Low 0.8 V, $C_L = 50\text{ pF}$
- Input level: High 2.4 V / Low 0.45 V (D0 to D15)
High 0.8 V_{CC} / Low 0.2 V_{CC} (except for D0 to D15)

(2) $V_{CC} = +3\text{ V} \pm 10\%$, $T_a = -20$ to $+70^\circ\text{C}$

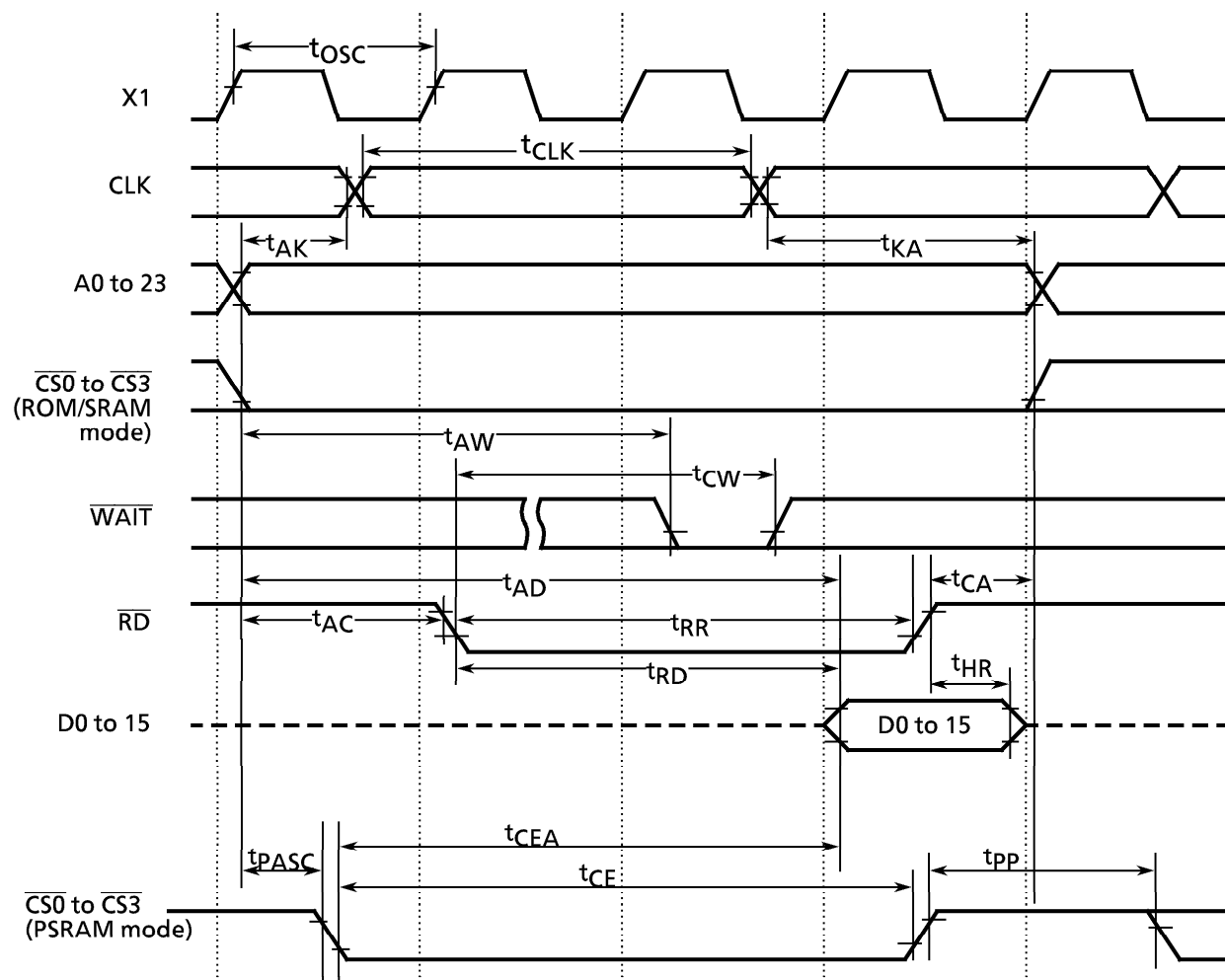
(fc = 4 MHz to 10 MHz)

No.	Parameter	Symbol	Formula		10 MHz		Unit
			Min	Max	Min	Max	
1	Oscillation cycle (= x)	t _{OSC}	100	250	100		ns
2	Clock pulse width	t _{CLK}	2.0x – 70		130		ns
3	A0 to 23 valid → $\overline{\text{RD}}/\overline{\text{WR}}$ fall	t _{AC}	1.0x – 60		40		ns
4	$\overline{\text{RD}}/\overline{\text{WR}}$ rise → A0 to 23 hold	t _{CA}	0.5x – 40		10		ns
5	A0 to 23 valid → D0 to 15 input	t _{AD}		3.5x – 125		225	ns
6	$\overline{\text{RD}}$ fall → D0 to 15 input	t _{RD}		2.5x – 115		135	ns
7	$\overline{\text{RD}}$ Low pulse width	t _{RR}	2.5x – 40		210		ns
8	$\overline{\text{RD}}$ rise → D0 to 15 hold	t _{HR}	0		0		ns
9	$\overline{\text{WR}}$ Low pulse width	t _{WW}	2.5x – 40		210		ns
10	D0 to 15 valid → $\overline{\text{WR}}$ rise	t _{DW}	2.0x – 120		80		ns
11	$\overline{\text{WR}}$ rise → D0 to 15 hold	t _{WD}	0.5x – 40		10		ns
12	A0 to 23 valid → $\overline{\text{WAIT}}$ input ^(1 WAIT + n mode)	t _{AW}		3.5x – 130		220	ns
	A0 to 23 valid → $\overline{\text{WAIT}}$ input ^(0 + n WAIT mode)	t _{AW}		1.5x – 80		70	ns
13	$\overline{\text{RD}}/\overline{\text{WR}}$ fall → $\overline{\text{WAIT}}$ hold ^(1 WAIT + n mode)	t _{CW}	2.5x + 0		250		ns
	$\overline{\text{RD}}/\overline{\text{WR}}$ fall → $\overline{\text{WAIT}}$ hold ^(0 + n WAIT mode)	t _{CW}	0.5x + 0		50		ns
14	$\overline{\text{WR}}$ rise → PORT valid	t _{CP}		200		200	ns
15	$\overline{\text{CS}}$ Low pulse width (PSRAM mode)	t _{CE}	3.0x – 70		230		ns
16	$\overline{\text{CS}}$ fall → D0 to 15 input (PSRAM mode)	t _{CEA}		3.0x – 160		140	ns
17	Address setup time (PSRAM mode)	t _{PASC}	0.5x – 30		20		ns
18	$\overline{\text{CS}}$ precharge time (PSRAM mode)	t _{PP}	1.0x – 40		60		ns

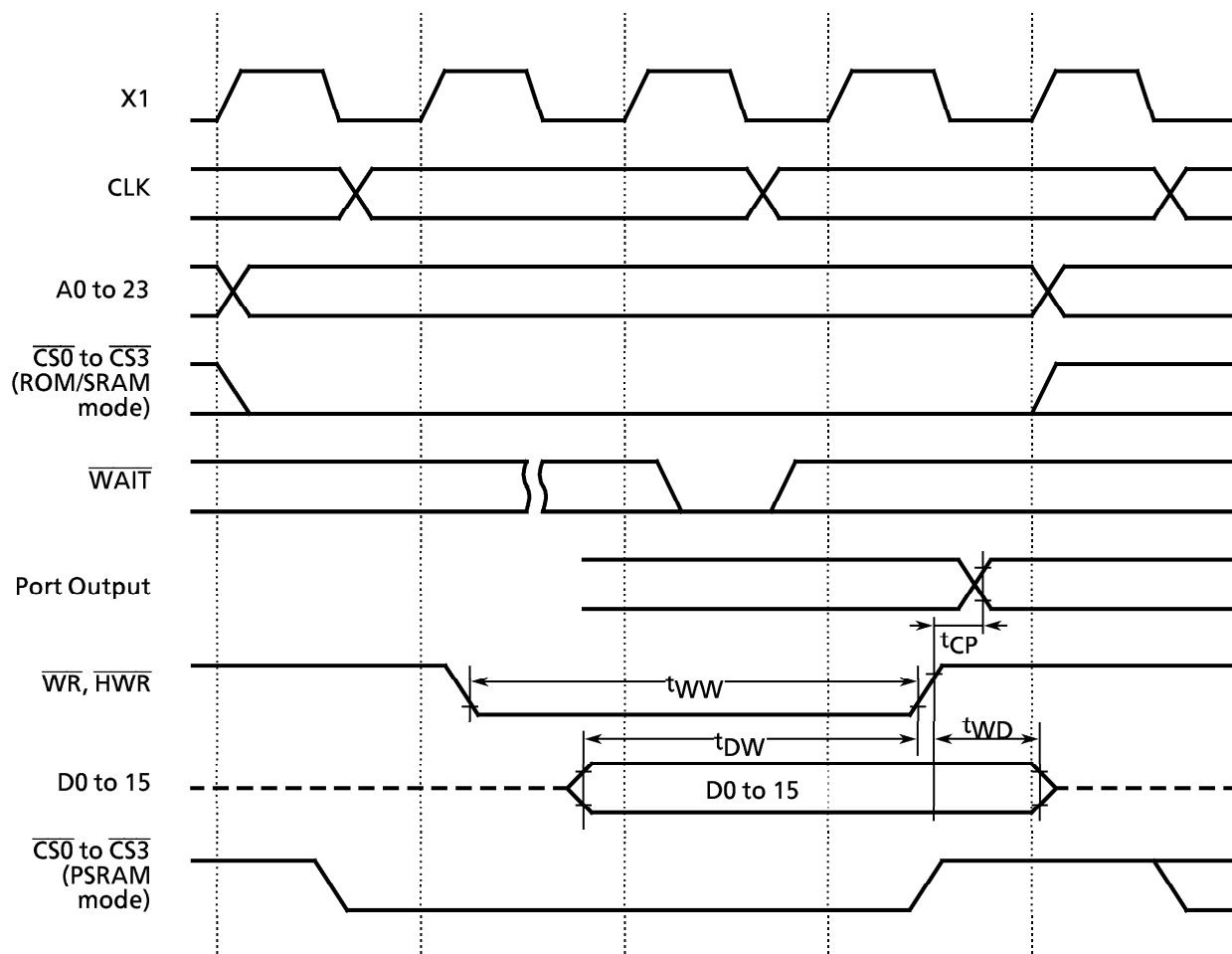
AC measuring conditions

- Output level: High 0.7x V_{CC} / Low 0.3x V_{CC}, CL = 50 pF
- Input level: High 0.9x V_{CC} / Low 0.1x V_{CC}

(3) Read Cycle



(4) Write Cycle



4.4 Serial Channel Timing

(1) I/O interface mode

① SCLK input mode

$V_{CC} = +5\text{ V} \pm 10\%$, $T_a = -20\text{ to } +70^\circ\text{C}$ ($f_c = 8\text{ to } 25\text{ MHz}$)
 $V_{CC} = +3\text{ V} \pm 10\%$, $T_a = -20\text{ to } +70^\circ\text{C}$ ($f_c = 4\text{ to } 10\text{ MHz}$)

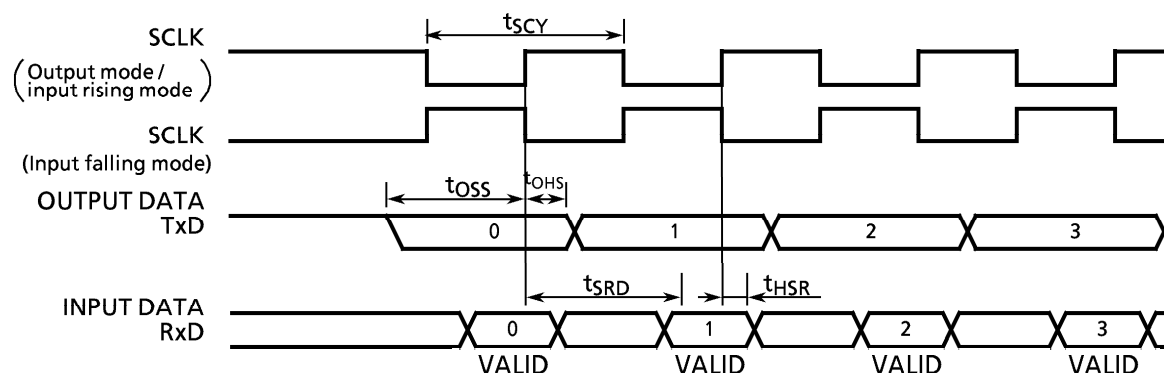
Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	16x		1.6		0.64		μs
Output Data → SCLK rise/fall*	t_{OSS}	$t_{SCY}/2 - 5x - 50$		250		70		ns
SCLK rise/fall* → Output Data hold	t_{OHS}	$5x - 100$		400		100		ns
SCLK rise/fall* → input data hold	t_{HSR}	0		0		0		ns
SCLK rise/fall* → valid data input	t_{SRD}		$t_{SCY} - 5x - 100$		1000		340	ns

*) SCLK rise/fall: In SCLK rising edge mode, SCLK rising edge timing; in SCLK falling edge mode, SCLK falling edge timing

② SCLK output mode

$V_{CC} = +5\text{ V} \pm 10\%$, $T_a = -20\text{ to } +70^\circ\text{C}$ ($f_c = 8\text{ to } 25\text{ MHz}$)
 $V_{CC} = +3\text{ V} \pm 10\%$, $T_a = -20\text{ to } +70^\circ\text{C}$ ($f_c = 4\text{ to } 10\text{ MHz}$)

Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle (programmable)	t_{SCY}	16x	8192x	1.6	819.2	0.64	327.6	μs
Output Data → SCLK rising edge	t_{OSS}	$t_{SCY} - 2x - 150$		1250		410		ns
SCLK rising edge → Output Data hold	t_{OHS}	$2x - 80$		120		0		ns
SCLK rising edge → Input Data hold	t_{HSR}	0		0		0		ns
SCLK rising edge → valid data input	t_{SRD}		$t_{SCY} - 2x - 150$		1250		410	ns



(2) UART Mode (SCLK0 to 2 External Input)

$V_{CC} = +5\text{ V} \pm 10\%$, $T_a = -20\text{ to } +70^\circ\text{C}$ ($f_c = 8\text{ to } 25\text{ MHz}$)
 $V_{CC} = +3\text{ V} \pm 10\%$, $T_a = -20\text{ to } +70^\circ\text{C}$ ($f_c = 4\text{ to } 10\text{ MHz}$)

Parameter	Symbol	Formula		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK cycle	t_{SCY}	$4x + 20$		420		180		ns
Low-level SCLK pulse width	t_{SCYL}	$2x + 5$		205		85		ns
High-level SCLK pulse width	t_{SCYH}	$2x + 5$		205		85		ns

4.5 A/D Conversion Characteristics

V_{CC} = +5 V ± 10%, T_a = -20 to +70°C (f_c = 8 to 25 MHz)V_{CC} = +3 V ± 10%, T_a = -20 to +70°C (f_c = 4 to 10 MHz)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
A/D analog reference supply voltage (+)		V _{REFH}		V _{CC} - 0.2		V _{CC}	V
A/D analog reference supply voltage (-)		V _{REFL}		V _{SS}		V _{SS} + 0.2	
Analog reference voltage		AV _{CC}		V _{CC} - 0.2		V _{CC}	
Analog reference voltage		AV _{SS}		V _{SS}		V _{SS} + 0.2	
Analog input voltage		V _{AIN}		V _{REFL}		V _{REFH}	
Analog reference voltage supply current	<VREFON> = 1	I _{REF}	V _{CC} = 5 V ± 10%			3.7	mA
			V _{CC} = 3 V ± 10%			2.2	
	<VREFON> = 0		V _{CC} = 2.7 to 5.5 V		0.02	5.0	
Total tolerance (excludes quantization error)		E _T	V _{CC} = 5 V ± 10%		± 1	± 3	LSB
			V _{CC} = 3 V ± 10%		± 1	± 3	

Note 1: 1LSB = (V_{REFH} - V_{REFL}) / 2¹⁰ [V]

Note 2: Power supply current ICC from the VCC pin includes the power supply current from the AVCC pin.

4.6 D/A Conversion Characteristics

V_{CC} = +5 V ± 10%, T_a = -20 to +70°C (f_c = 8 to 25 MHz)V_{CC} = +3 V ± 10%, T_a = -20 to +70°C (f_c = 4 to 10 MHz)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Analog reference voltage	AV _{CC}		V _{CC} - 0.2		V _{CC}	V
Analog reference voltage	AV _{SS}		V _{SS}		V _{SS} + 0.2	
Total tolerance		R = 1 MΩ (Note)			7.0	LSB
		R = 5 MΩ (Note)			4.0	LSB
		R = 10 MΩ (Note)			3.5	LSB
Differential linear error				2.0		LSB

Note: R is the external load resistance on the D/A converter output pin (DAOUT0, DAOUT1).

4.7 Event Counter (External Input Clocks: TI0, TI4, TI8, TI9, TIA, TIB)

V_{CC} = +5 V ± 10%, T_a = -20 to +70°C (f_c = 8 to 25 MHz)V_{CC} = +3 V ± 10%, T_a = -20 to +70°C (f_c = 4 to 10 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
External input clock cycle	t _{VCK}	8x + 100		900		420		ns
External low-level input clock pulse width	t _{VCKL}	4x + 40		440		200		ns
External high-level input clock pulse width	t _{VCKH}	4x + 40		440		200		ns

4.8 Interrupt Operation

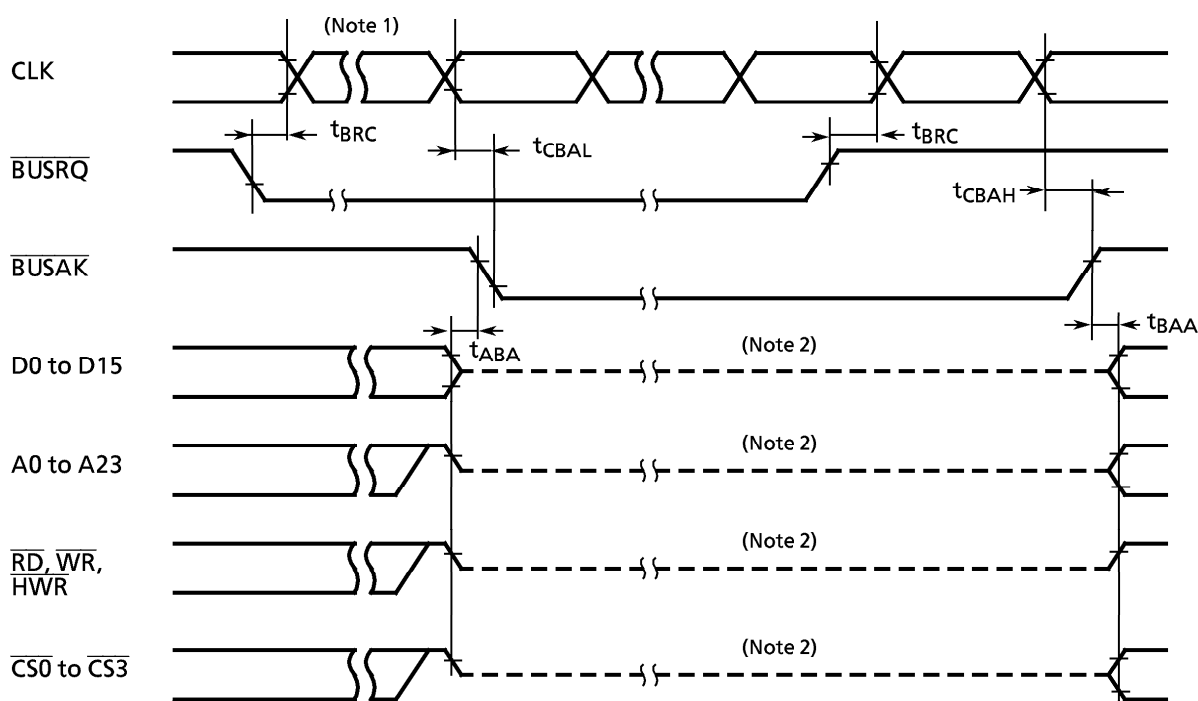
V_{CC} = +5 V ± 10%, T_a = -20 to +70°C (f_c = 8 to 25 MHz)V_{CC} = +3 V ± 10%, T_a = -20 to +70°C (f_c = 4 to 10 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{\text{NMI}}$, INT0 to 4 low-level pulse width	t _{INTAL}	4x		400		160		ns
$\overline{\text{NMI}}$, INT0 to 4 high-level pulse width	t _{INTAH}	4x		400		160		ns
INT5 to INT8 low-level pulse width	t _{INTBL}	8x + 100		900		420		ns
INT5 to INT8 high-level pulse width	t _{INTBH}	8x + 100		900		420		ns

4.9 Bus Request/Bus Acknowledge Timing

$V_{CC} = +5\text{ V} \pm 10\%$, $T_a = -20$ to $+70^\circ\text{C}$ ($f_c = 8$ to 25 MHz)
 $V_{CC} = +3\text{ V} \pm 10\%$, $T_a = -20$ to $+70^\circ\text{C}$ ($f_c = 4$ to 10 MHz)

Parameter	Symbol	Calculator		10 MHz		25 MHz		Unit
		Min	Max	Min	Max	Min	Max	
BUSRQ setup time for CLK	t_{BRC}	120		120		120		ns
CLK → BUSAK fall	t_{CBAL}		$2.0x + 120$		320		200	ns
CLK → BUSAK rise	t_{CBAH}		$0.5x + 40$		90		60	ns
Time from output buffer off until BUSAK falling edge	t_{ABA}	0	80	0	80	0	80	ns
Time from BUSAK rising edge until output buffer on	t_{BAA}	0	80	0	80	0	80	ns



Note 1: When $\overline{BUSRQ}$ goes to low level to request bus release, if the current bus cycle is yet complete due to a wait, the bus is not released until the wait completes.

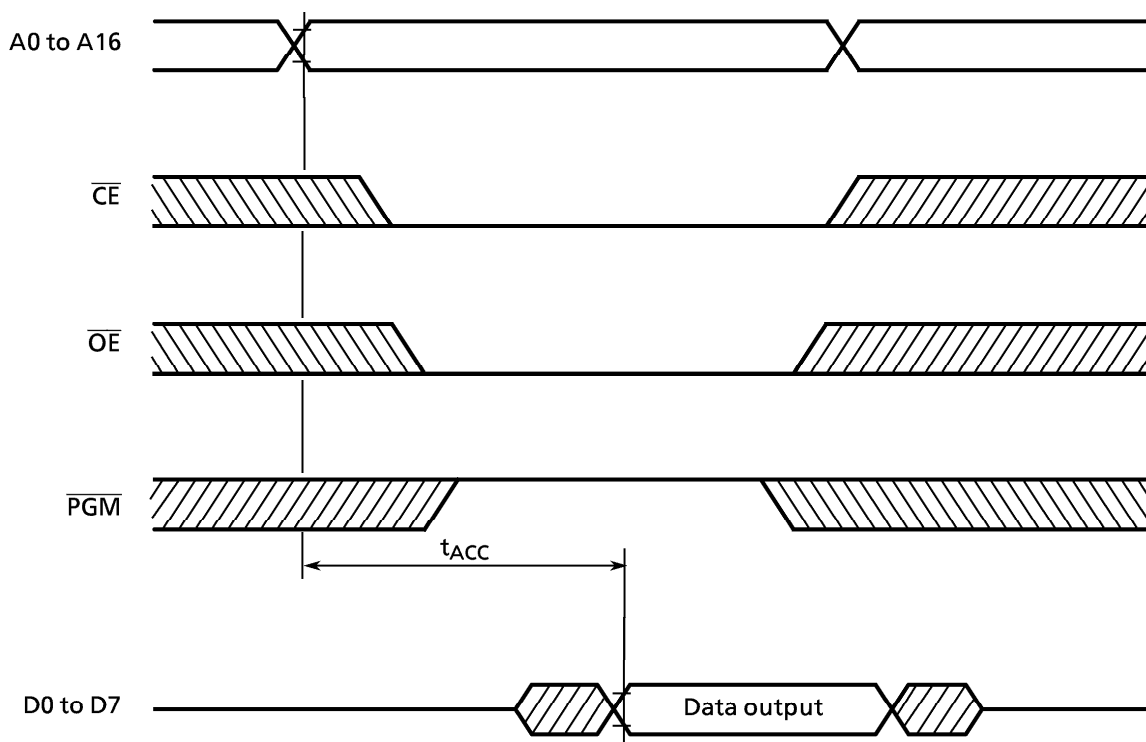
Note 2: The dotted line indicates only that the output buffer is off, not that the signal is at middle level. Immediately after bus release, the signal level prior to the bus release is held dynamically by the external load capacitance. Therefore, designs should allow for the fact that when using an external resistor or similar to fix the signal level while the bus is released, after bus release a delay occurs before the signal goes to its fixed level (due to the CR time constant). The internal programmable pull-up resistor continues to function in accordance with the internal signal level.

4.10 Read Operations in PROM Mode

DC / AC Electrical Specifications

 $T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$

Parameter	Symbol	Test Condition	Min	Max	Unit
V_{PP} Read Voltage	V_{PP}		4.5	5.5	V
Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, PGM)	V_{IH}		2.2	$V_{CC} + 0.3$	V
Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, PGM)	V_{IL}		-0.3	0.8	V
Address to Output Delay	t_{ACC}	$C_L = 50\text{ pF}$	-	$2.25TCYC + \alpha$	ns

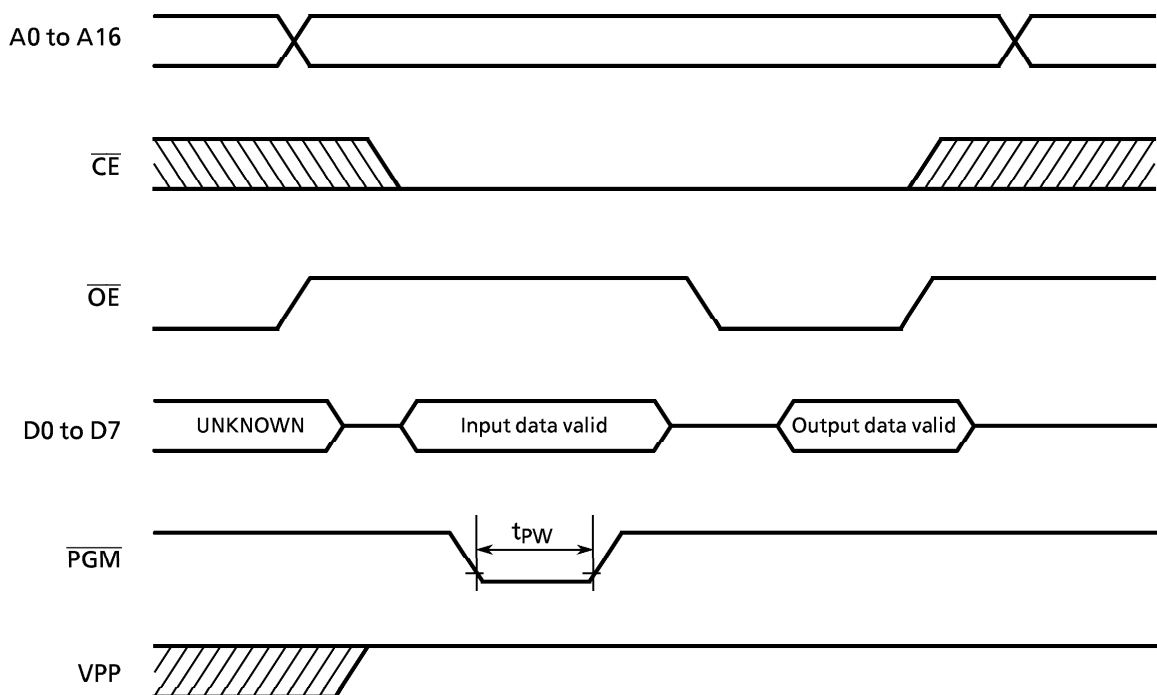
 $TCYC = 400\text{ ns}$ (10 MHz Clock) $\alpha = 200\text{ ns}$ 

4.11 Program Operations in PROM Mode

DC / AC Electrical Specifications

 $T_a = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Programing Supply Voltage	V_{PP}		12.50	12.75	13.00	V
Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH}		2.6		$V_{CC} + 0.3$	V
Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL}		-0.3		0.8	V
V_{CC} Supply Current	I_{CC}	$f_c = 10\text{ MHz}$	-		50	mA
V_{PP} Supply Current	I_{PP}	$V_{PP} = 13.00\text{ V}$	-		50	mA
$\overline{PGM}$ Program Pulse Width	t_{PW}	$C_L = 50\text{ pF}$	0.095	0.1	0.105	ms



Note 1: When turning the V_{PP} (12.75 V) power supply off and on, ensure that V_{CC} is on.

Note 2: Do not plug in or unplug the device when the V_{PP} power (12.75 V) is on.
(This can damage the device.)

Note 3: The V_{PP} pin maximum rating is 14 V. When the program is executed, the voltage applied, including overshoot, should not exceed 14 V.

