Low Voltage/Low Power CMOS 16-bit Microcontrollers

TMP93CS20F

1. Outline and Device Characteristics

The TMP93CS20 is high-speed, advanced 16-bit microcontrollers. It enables low-voltage and low-power-consumption operation.
The TMP93CS20 is housed in 144-pin flat packages.
The device characteristics are as follows:

(1) Original 16-bit CPU (900/L CPU)

- TLCS-90 instruction mnemonic upward compatible
- 16 Mbytes linear address space
- General-purpose registers, register bank system
- 16-bit multiplication, 16-bit division, bit transfer and bit manipulation instructions
- Micro DMA: 4 channels (1.6 μs per 2 bytes at 20 MHz)

(2) Minimum instruction execution time: 200 ns at 20 MHz

(3) Internal RAM: 2 Kbytes

Internal ROM: 64 Kbytes

(4) LCD driver

- Boosting circuit (Reference voltage external input)
- Maximum 40segment × 4common
- 1/4, 1/3, 1/2 duty, static driving selection

(5) Timer for realtime clock: 1 channel

(6) 8-bit timer: 4 channels

(7) 16-bit timer: 4 channels

(8) Serial interface:2 channels

- UART/Synchronous mode: 1 channel
- UART: 1 channel

(9) Serial bus interface: 1 channel

- I^2C bus mode/Clock synchronous 8-bit SIO mode

(10) 10-bit AD converter: 8 channels

(11) Large current drive port: 8 ports (Port A)

(12) Watchdog timer

(13) Key-on wake-up (Key input interrupt)

(14) Interrupt functions

- 9 CPU interrupts (SWI instruction, and Illegal instruction)
- 24 internal interrupts
- 12 external interrupts

7-level priority can be set.

(15) I/O ports: 88 pins (including XT1, XT2)

- Large current output: 8 pins, LED can be directly driven.

(16) Standby function: 4 halt modes (Run, Idle2, Idle1, Stop)

(17) Clock gear function

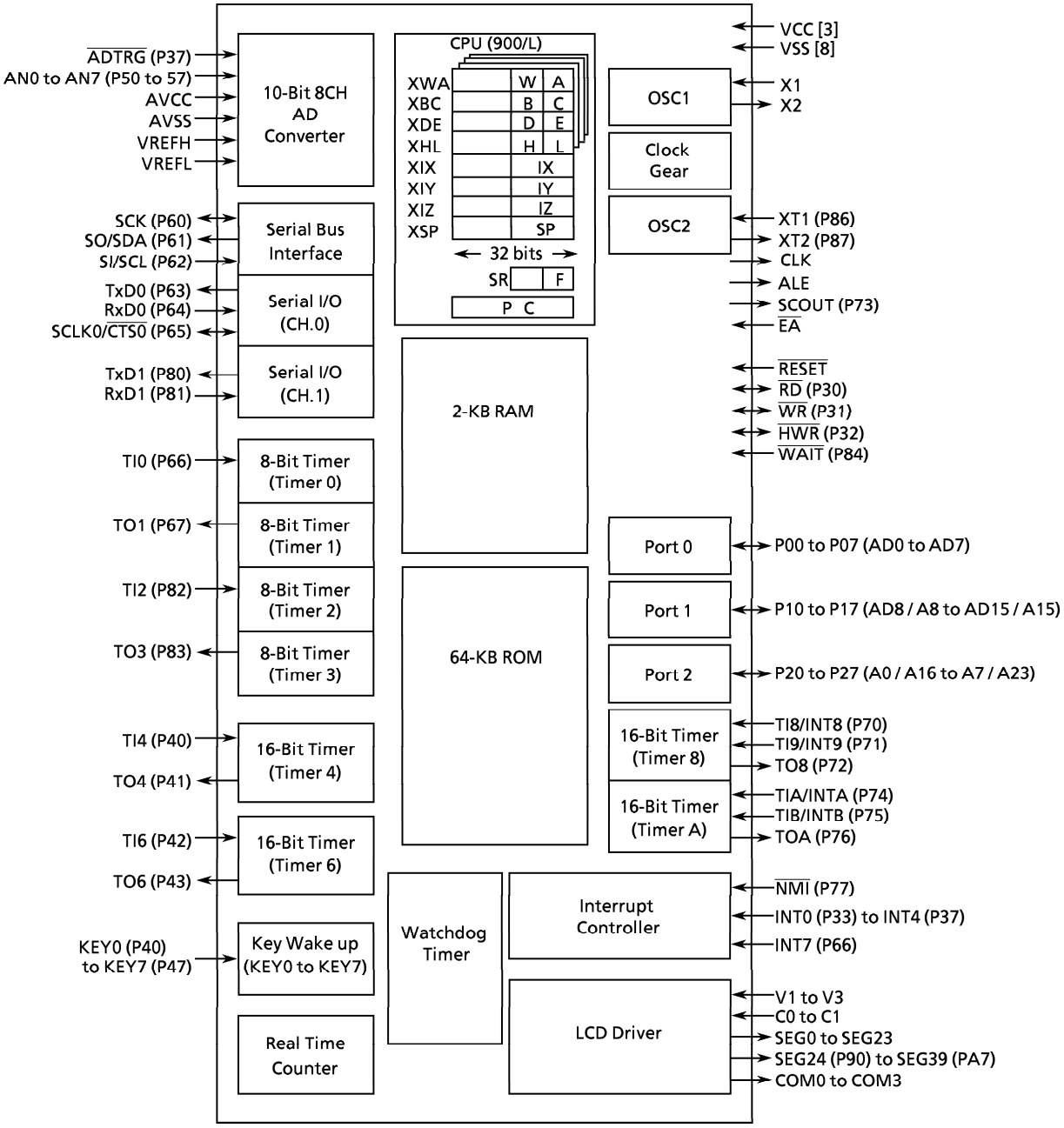
- Clock gear: High-frequency clock can be changed from fc to fc/16.
- Dual clock Operation

(18) Operating voltage

- Vcc = 2.7 to 5.5 V

(19) Package

- P-LQFP144-1616-0.40



Note: The item in parentheses ( ) are the initial setting after reset.

Figure 1 TMP93CS20 Block Diagram

2. Pin Assignment and Functions

The assignment of input and output pins for the TMP93CS20, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93CS20F.

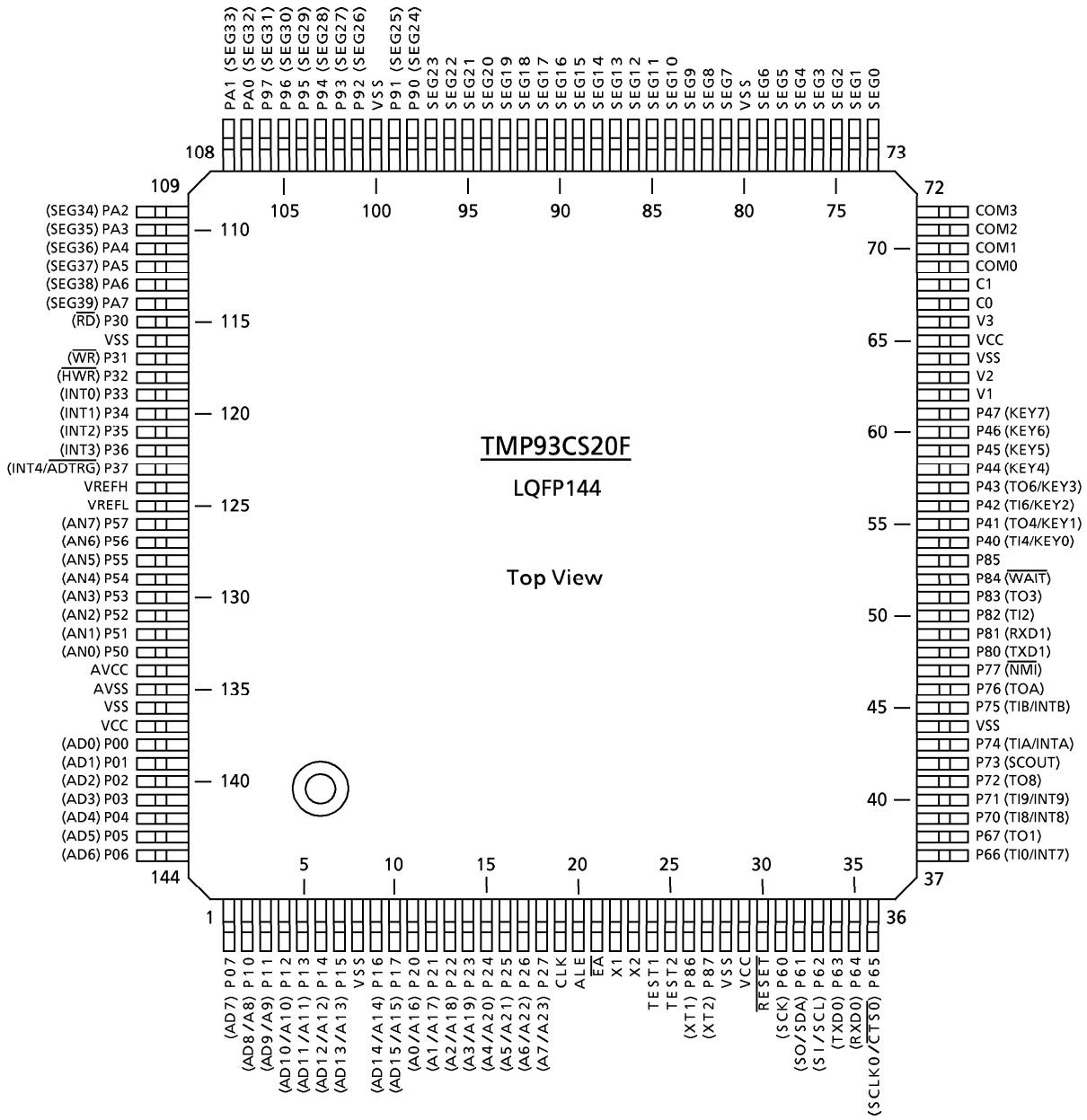


Figure 2.1.1 Pin Assignment (144-pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 Pin names and functions.

Table 2.2.1 Pin Names and Function (1/4)

Pin Name	Number of Pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O I/O	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 for address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O I/O Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 for address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level (with pull-up resistor) Address: Bits 0 to 7 for address bus Address: Bits 16 to 23 for address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory (Read when reading internal memory at P3<P30> = 0, P3FC<P30F> = 1)
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to 7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to 15
P33 INT0	1	I/O Input	Port 33: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising/falling edge
P34 INT1	1	I/O Input	Port 34: I/O port (with pull-up resistor) Interrupt request pin 1: Interrupt request pin with programmable rising/falling edge
P35 INT2	1	I/O Input	Port 35: I/O port (with pull-up resistor) Interrupt request pin 2: Interrupt request pin with programmable rising/falling edge
P36 INT3	1	I/O Input	Port 36: I/O port (with pull-up resistor) Interrupt request pin 3: Interrupt request pin with programmable rising/falling edge
P37 INT4 $\overline{ADTRG}$	1	I/O Input Input	Port 37: I/O port (with pull-up resistor) Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge AD converter external start trigger input
P40 TI4 KEY0	1	I/O Input Input	Port 40: I/O port (with pull-up resistor) Timer input 4: 16-bit timer 4 input Key input 0: Key-on wake-up pin 0

Table 2.2.1 Pin Names and Function (2/4)

Pin Name	Number of Pins	I/O	Functions
P41 TO4 KEY1	1	I/O Output Input	Port 41: I/O port (with pull-up resistor) Timer output 4: 16-bit timer 4 output Key input 1: Key-on wake-up pin 1
P42 TI6 KEY2	1	I/O Input Input	Port 42: I/O port (with pull-up resistor) Timer input 6: 16-bit timer 6 input Key input 2: Key-on wake-up pin 2
P43 TO6 KEY3	1	I/O Output Input	Port 43: I/O port (with pull-up resistor) Timer output 6: 16-bit timer 6 output Key input 3: Key-on wake-up pin 3
P44 to 47 KEY4 to KEY7	4	I/O Input	Port 44 to 47: I/O port (with pull-up resistor) Key input 4 to 7: Key-on wake-up pin 4 to 7
P50 to P57 AN0 to AN7	8	Input Input	Port 50 to 57: Pin used to input port Analog input 0 to 7
P60 SCK	1	I/O I/O	Port 60: I/O port Clock I/O pin in SIO mode of the serial bus interface
P61 SO SDA	1	I/O Output I/O	Port 61: I/O port (with programmable open drain) Data send channel in SIO mode of the serial bus interface Data I/O pin in I^2C bus mode of the serial bus interface
P62 SI SCL	1	I/O Input I/O	Port 62: I/O port (with programmable open drain) Data receive channel in SIO mode of the serial bus interface Clock I/O pin in I^2C bus mode of the serial bus interface
P63 TXD0	1	I/O Output	Port 63: I/O port (with programmable open drain) Serial send data 0
P64 RXD0	1	I/O Input	Port 64: I/O port Serial receive data 0
P65 SCLK0 $\overline{CTS0}$	1	I/O I/O Input	Port 65: I/O port Serial clock I/O 0 Serial data send enable 0 (Clear To Send)
P66 TI0 INT7	1	I/O Input Input	Port 66: I/O port Timer input 0: 8-bit timer 0 input Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge
P67 TO1	1	I/O Output	Port 67: I/O port Timer output1: 8-bit timer 0 or timer 1 output
P70 TI8 INT8	1	I/O Input Input	Port 70: I/O port (with pull-up resistor) Timer input 8: 16-bit timer 8 input Interrupt request pin 8: Interrupt request pin with programmable rising/falling edge
P71 TI9 INT9	1	I/O Input Input	Port 71: I/O port (with pull-up resistor) Timer input 9: 16-bit timer 8 input Interrupt request pin 9: Interrupt request pin with rising edge

Table 2.2.1 Pin Names and Function (3/4)

Pin Name	Number of Pins	I/O	Functions
P72 TO8	1	I/O Output	Port 72: I/O port (with pull-up resistor) Timer output 8: 16-bit timer 8 output
P73 SCOUT	1	I/O Output	Port 73: I/O port (with pull-up resistor) System clock output: System clock or double system clock output to be synchronized with the external circuit
P74 TIA INTA	1	I/O Input Input	Port 74: I/O port (with pull-up resistor) Timer input A: 16-bit timer A input Interrupt request pin A: Interrupt request pin with programmable rising/falling edge
P75 TIB INTB	1	I/O Input Input	Port 75: I/O port (with pull-up resistor) Timer input B: 16-bit timer B input Interrupt request pin B: Interrupt request pin with rising edge
P76 TOA	1	I/O Output	Port 76: I/O port (with pull-up resistor) Timer output A: 16-bit timer A output
P77 $\overline{\text{NMI}}$	1	I/O Input	Port 77: I/O port (with pull-up resistor) Non-maskable Interrupt request pin: Interrupt request pin with programmable falling edge or both edges.
P80 TXD1	1	I/O Output	Port 80: I/O port (with programmable open drain) Serial send data 1
P81 RXD1	1	I/O Input	Port 81: I/O port (with programmable open drain) Serial receive data 1
P82 TI2	1	I/O Input	Port 82: I/O port (with programmable open drain) Timer input 2: 8-bit timer 2 input pin
P83 TO3	1	I/O Output	Port 83: I/O port (with programmable open drain) Timer output 3: 8-bit timer 2, 3 output pin
P84 $\overline{\text{WAIT}}$	1	I/O Input	Port 84: I/O port (with programmable open drain) Wait: Pin used to request CPU bus wait
P85	1	I/O	Port 85: I/O port (with programmable open drain)
P86 XT1	1	I/O Input	Port 86: I/O port (open drain) Low Frequency Oscillator connecting pin
P87 XT2	1	I/O Output	Port 87: I/O port (open drain) Low Frequency Oscillator connecting pin
P90 to P97 SEG24 to 31	8	Output Output	Port 90 to 97: Output port (open drain) Segment data output pin
PA0 to PA7 SEG32 to 39	8	Output Output	Port A0 to A7: Output port, Large current port (open drain) LCD segment output pin
SEG0 to 23	24	Output	LCD segment output
COM0 to 3	4	Output	LCD common output

Table 2.2.1 Pin Names and Function (4/4)

Pin Name	Number of Pins	I/O	Functions
AVCC	1	Power supply	Power supply pin for AD converter
AVSS	1	Power supply	GND pin for AD converter (0 V)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
X1	1	Input	Oscillator connecting pin
X2	1	Output	Oscillator connecting pin
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI
ALE	1	Output	Address Latch Enable Can be disabled for reducing noise.
CLK	1	Output	Clock output: Outputs "External input clock X1 ÷ 4" Clock. Pulled-up during reset. Can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	The VCC pin should be connected.
VCC	3	Power supply	Power supply pin (All Vcc pins should be connected with the power supply pin.)
VSS	8	Power supply	GND pin (0 V) (All Vss pins should be connected with GND (0 V).)
TEST1 TEST2	2	Output Input	TEST1 should be connected with TEST2 pin.
C0, C1, V1 to V3	5	LCD pin	LCD drive boosting pin. A condenser should be connected between C0 and C1, V1, V2, V3 and GND.

Note: All pins that have built-in pull-up resistors can be disconnected from the built-in pull-up resistor by software.

3. Operation

This section describes in blocks the functions and basic operations of TMP93CS20 device. Please also refer to section 7., Precautions in use, which describes some points requiring careful attention.

3.1 CPU

TMP93CS20 devices have a built-in high-performance 16-bit CPU (900/L CPU). (For basics of the CPU operation, see the information on the TLCS-900/L CPU in the previous chapter).
This section describes some CPU functions unique to the TMP93CS20, that are not described in the previous chapter, entitled TLCS-900/L CPU.

3.1.1 Reset

To reset a TMP93CS20 device, the $\overline{\text{RESET}}$ pin must be kept at 0 for at least ten system clock cycles (16 μs at 20 MHz) while remaining within the specified operating voltage range and sustaining a stable clock oscillation.
When a reset signal is accepted, the CPU sets itself as follows:

- The Program Counter (PC) is set according to the Reset Vector that is stored from FFFF00H to FFFF02H.

  PC (7 to 0) ← Data in location FFFF00H
  PC (15 to 8) ← Data in location FFFF01H
  PC (23 to 16) ← Data in location FFFF02H

- The Stack pointer (XSP) for system mode is set to 100H.
- The <IFF2 to 0> bits of the status register SR are set to 111. (Sets mask register to interrupt level 7)
- The <MAX> bit of SR is set to 1. (Sets to maximum mode. See previous chapter).
- The <RFP2 to 0> bits of SR are set to 000. (Clears register banks to 0)

When the reset is released, instruction execution starts from PC (the reset vector). The reset makes no changes in any CPU internal registers other than those specifically mentioned above.
When a reset is received, signal and data processing for built-in I/Os, ports, and other pins is affected as follows:

- Initializes built-in I/O registers as per specifications.
- Sets port pins (including pins also used as built-in I/Os) to General-Purpose Input / Output Port mode.
- Pulls up the CLK pin to 1.
- Sets the ALE pin to High Impedance (High-Z).

Note 1: Resetting makes no change in any register in the CPU except the program counter (PC), status register (SR) and stack pointer (XSP), nor in the data in the internal RAM.
Note 2: The CLK pin is pulled up to "H" level during reset . When the voltage is put down externally, there is possible to cause malfunctions.

Figure 3.1.1 shows the reset timing chart of TMP93CS20.

3.2 Memory Map

Figure 3.2.1 is a memory map of the TMP93CS20.

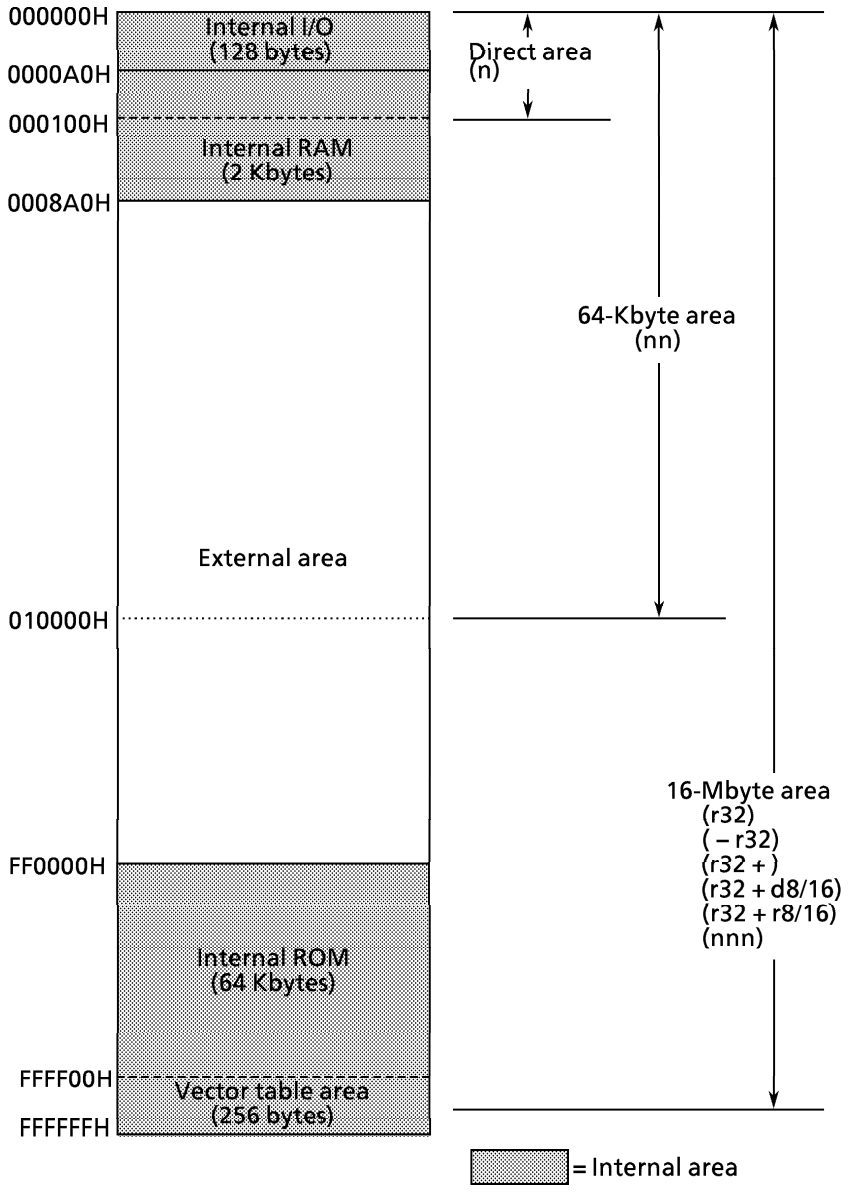


Figure 3.2.1 Memory Map

4. Electrical Characteristics

4.1 Absolute Maximum Ratings (TMP93CS20F)

"X" used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>. The value of X changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for fc, with gear = fc/1 (SYSCR1<SYSCK, GEAR 2 to 0> = 0000).

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	– 0.5 to 6.5	V
Input Voltage	V_{IN}	– 0.5 to Vcc + 0.5	V
Output Current (per one pin), Large current port	I_{OL1}	20	mA
Output Current (per one pin)	I_{OL2}	2	mA
Output Current (total of large current port)	ΣI_{OL1}	80	mA
Output Current (total)	ΣI_{OL}	120	mA
Output Current (total)	ΣI_{OH}	– 80	mA
Power Dissipation (Ta = 85)	P_D	600	mW
Soldering Temperature (10 s)	T_{SOLDER}	260	℃
Storage Temperature	T_{STG}	– 65 to 150	℃
Operating Temperature	T_{OPR}	– 40 to 85	℃

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Ta = – 40 to 85°C

Parameter		Symbol	Condition		Min	Typ. (Note)	Max	Unit
Power Supply Voltage (AVcc = Vcc, AVss = Vss = 0 V)		Vcc	fc = 4 to 20 MHz	fs = 30 to 34 kHz	4.5		5.5	V
			fc = 4 to 12.5 MHz		2.7			
Input Low Voltage	AD0 to 15	V_{IL}	Vcc ≧ 4.5 V		– 0.3		0.8	V
			Vcc < 4.5 V				0.6	
	Port	V_{IL1}	Vcc = 2.7 to 5.5 V				0.3 Vcc	
	KEY0 to 7, $\overline{NMI}$, INT0 to 4	V_{IL2}					0.25 Vcc	
	$\overline{EA}$	V_{IL3}					0.3	
	X1	V_{IL4}					0.2 Vcc	
	$\overline{RESET}$	V_{IL5}					0.1 Vcc	
Input High Voltage	AD0 to 15	V_{IH}	Vcc ≧ 4.5 V		2.2		Vcc + 0.3	V
			Vcc ≧ 4.5 V		2.0			
	Port	V_{IH1}	Vcc = 2.7 to 5.5 V		0.7 Vcc			
	KEY0 to 7, $\overline{NMI}$, INT0 to 4	V_{IH2}			0.75 Vcc			
	$\overline{EA}$	V_{IH3}			Vcc – 0.3			
	X1	V_{IH4}			0.8 Vcc			
	$\overline{RESET}$	V_{IH5}			0.6 Vcc			

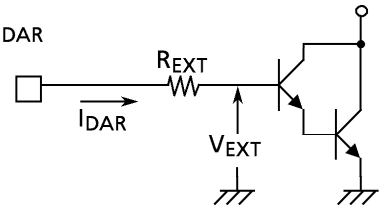
Note: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA (Vcc = 2.7 to 5.5 V)			0.45	V
Output Low Current (PA0 to 7)	I_{OLA}	V_{OL} = 1.0 V (Vcc = 5 V ± 10%)	16			mA
		V_{OL} = 1.0 V (Vcc = 3 V ± 10%)	7			
Output High Voltage	V_{OH1}	I_{OH} = −400 μA (Vcc = 3 V ± 10%)	2.4			V
	V_{OH2}	I_{OH} = −400 μA (Vcc = 5 V ± 10%)	4.2			
Darlington Drive Current (8 Output Pins max)	I_{DAR} (Note 2)	V_{EXT} = 1.5 V, R_{EXT} = 1.1 kΩ (Vcc = 5 V ± 10% only)	−1.0		−3.5	mA
Input Leakage Current	I_{LI}	0.0 ≦ V_{IN} ≦ V_{CC}		0.02	±5	μA
Output Leakage Current	I_{LO}	0.2 ≦ V_{IN} ≦ V_{CC} − 0.2		0.05	±10	
Power Down Voltage (at Stop, RAM Back-up)	V_{STOP}	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc	2.0		6.0	V
Pin Capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt Width KEYx, $\overline{NMI}$, INT0 to 4, $\overline{RESET}$	V_{TH}		0.4	1.0		V
Programmable Pull-Up Resistance	R_{KH}	Vcc = 5 V ± 10%	50		150	kΩ
		Vcc = 3 V ± 10%	100		300	
Normal	I_{CC}	Vcc = 5 V ± 10%, fc = 20 MHz		25	28	mA
Run				20	25	
Idle2				14	17	
Idle1				3.5	5	
Normal		Vcc = 3 V ± 10%, fc = 12.5 MHz (Typ. Vcc = 3.0 V)		11	14	mA
Run				9	12	
Idle2				6	7.5	
Idle1				1.5	2.0	
Slow		Vcc = 3 V ± 10%, fs = 32.768 kHz (Typ. Vcc = 3.0 V) at Boosting frequency = 1 kHz		28	37	μA
Run				21	27	
Idle2				14	19	
Idle1				7	9	
Stop		Ta ≦ 50°C		0.2	10	μA
		Ta ≦ 70°C			20	
		Ta ≦ 85°C			50	

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.
Note 2: I_{DAR} is guaranteed for up to eight ports.
Note 3: Segment or Common output is not loaded.
Note 4: I_{CC} measurement conditions (NORMAL, SLOW). Only CPU is operational; output pins are open and input pins are fixed.

e.g. Diagram of I_{DAR}



4.3 AC Electrical Characteristics

(1) Vcc = 5 V ± 10%

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	50	31250	62.5		50		ns
2	CLK width	t_{CLK}	2x – 40		85		60		ns
3	A0 to A23 Valid→ CLK Hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK Valid→ A0 to A23 Hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to A15 Valid→ ALE Fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall→ A0 to A15 Hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE High Width	t_{LL}	x – 40		23		10		ns
8	ALE Fall→ $\overline{RD}$/$\overline{WR}$ Fall	t_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$/$\overline{WR}$ Rise→ ALE Rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to A15 Valid→ $\overline{RD}$/$\overline{WR}$ Fall	t_{ACL}	x – 25		38		25		ns
11	A0 to A23 Valid→ $\overline{RD}$/$\overline{WR}$ Fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$/$\overline{WR}$ Rise→ A0 to A23 Hold	t_{CA}	0.5x – 25		6		0		ns
13	A0 to A15 Valid→ D0 to D15 Input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to A23 Valid→ D0 to D15 Input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$ Fall → D0 to D15 Input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ Low Pulse Width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$ Rise→ D0 to D15 Hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ Rise→ A0 to A15 Output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ Low Pulse Width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to D15 Valid→ $\overline{WR}$ Rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ Rise →D0 to D15 Hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to A23 Valid→ $\overline{WAIT}$ Input ($^{1\ WAIT}_{+\ n\ mode}$)	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to A15 Valid→ $\overline{WAIT}$ Input ($^{1\ WAIT}_{+\ n\ mode}$)	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}$/$\overline{WR}$ Fall→$\overline{WAIT}$ Hold ($^{1\ WAIT}_{+\ n\ mode}$)	t_{CW}	2.0x + 0		125		100		ns
25	A0 to A23 Valid→ Port Input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to A23 Valid→ Port Hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ Rise→Port Valid	t_{CP}		200		200		200	ns

AC Measuring Conditions

- Output Level: High 2.2 V/Low 0.8 V, CL = 50 pF
  (However, CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input Level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 × Vcc/Low 0.2 × Vcc (except for AD0 to AD15)

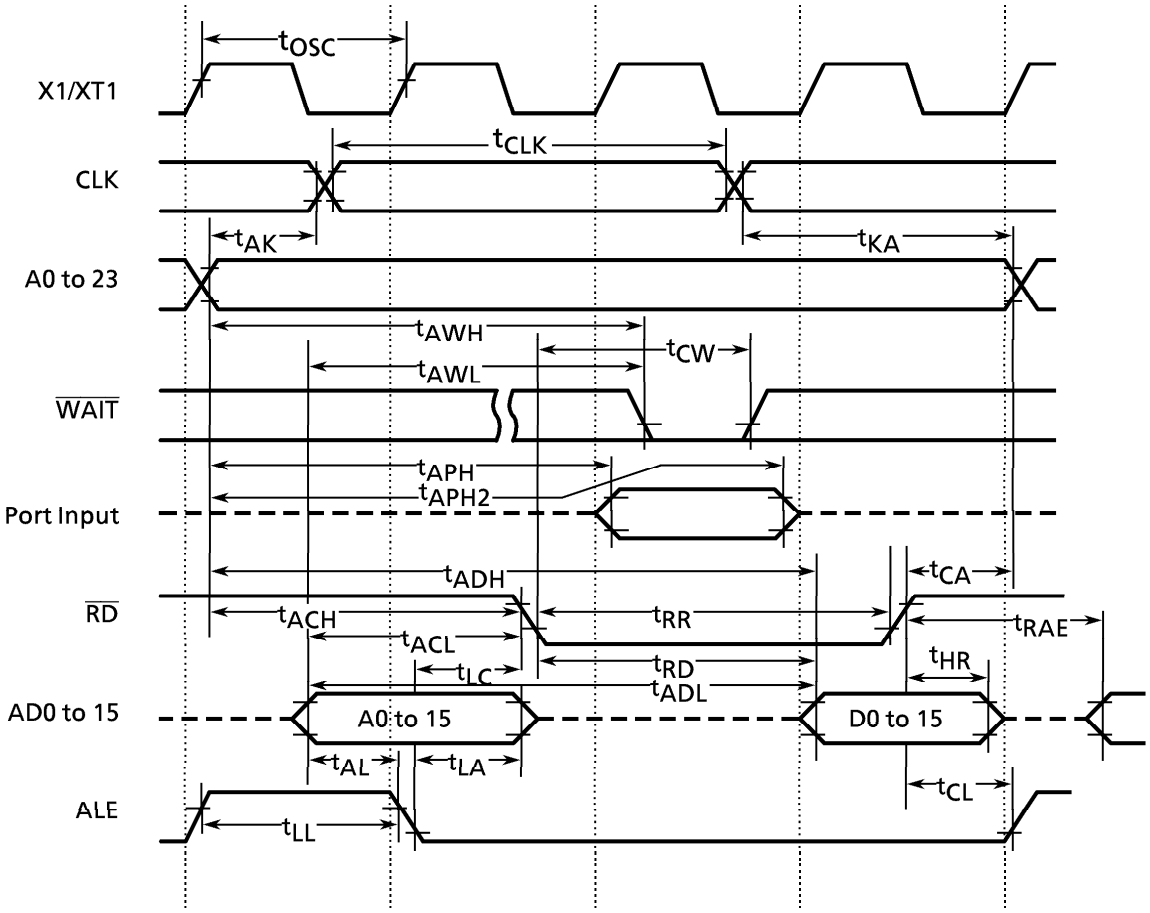
(2) Vcc = 3 V ± 10%

No.	Parameter	Symbol	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	Osc. Period (= x)	t_{OSC}	80	31250	80		ns
2	CLK Width	t_{CLK}	2x − 40		120		ns
3	A0 to A23 Valid→ CLK Hold	t_{AK}	0.5x − 30		10		ns
4	CLK Valid→ A0 to A23 Hold	t_{KA}	1.5x − 80		40		ns
5	A0 to A15 Valid→ ALE Fall	t_{AL}	0.5x − 35		5		ns
6	ALE Fall→ A0 to A15 Hold	t_{LA}	0.5x − 35		5		ns
7	ALE High Width	t_{LL}	x − 60		20		ns
8	ALE Fall→ $\overline{RD}$/$\overline{WR}$ Fall	t_{LC}	0.5x − 35		5		ns
9	$\overline{RD}$/$\overline{WR}$ Rise→ ALE Rise	t_{CL}	0.5x − 40		0		ns
10	A0 to A15 Valid→ $\overline{RD}$/$\overline{WR}$ Fall	t_{ACL}	x − 50		30		ns
11	A0 to A23 Valid→ $\overline{RD}$/$\overline{WR}$ Fall	t_{ACH}	1.5x − 50		70		ns
12	$\overline{RD}$/$\overline{WR}$ Rise→ A0 to A23 Hold	t_{CA}	0.5x − 40		0		ns
13	A0 to A15 Valid→ D0 to D15 Input	t_{ADL}		3.0x − 110		130	ns
14	A0 to A23 Valid→ D0 to D15 Input	t_{ADH}		3.5x − 125		155	ns
15	$\overline{RD}$ Fall →D0 to D15 Input	t_{RD}		2.0x − 115		45	ns
16	$\overline{RD}$ Low Pulse Width	t_{RR}	2.0x − 40		120		ns
17	$\overline{RD}$ Rise→ D0 to D15 Hold	t_{HR}	0		0		ns
18	$\overline{RD}$ Rise→ A0 to A15output	t_{RAE}	x − 25		55		ns
19	$\overline{WR}$ Low Pulse Width	t_{WW}	2.0x − 40		120		ns
20	D0 to D15 Valid→ $\overline{WR}$ Rise	t_{DW}	2.0x − 120		40		ns
21	$\overline{WR}$ Rise →D0 to D15 Hold	t_{WD}	0.5x − 40		0		ns
22	A0 to A23 Valid→ $\overline{WAIT}$ Input $(^{1\ WAIT}_{+n\ mode})$	t_{AWH}		3.5x − 130		150	ns
23	A0 to A15 Valid→ $\overline{WAIT}$ Input $(^{1\ WAIT}_{+n\ mode})$	t_{AWL}		3.0x − 100		140	ns
24	$\overline{RD}$/$\overline{WR}$ Fall→$\overline{WAIT}$ Hold $(^{1\ WAIT}_{+n\ mode})$	t_{CW}	2.0x + 0		160		ns
25	A0 to A23 Valid→ Port input	t_{APH}		2.5x − 120		80	ns
26	A0 to A23 Valid→ Port Hold	t_{APH2}	2.5x + 50		250		ns
27	$\overline{WR}$ Rise→ Port Valid	t_{CP}		200		200	ns

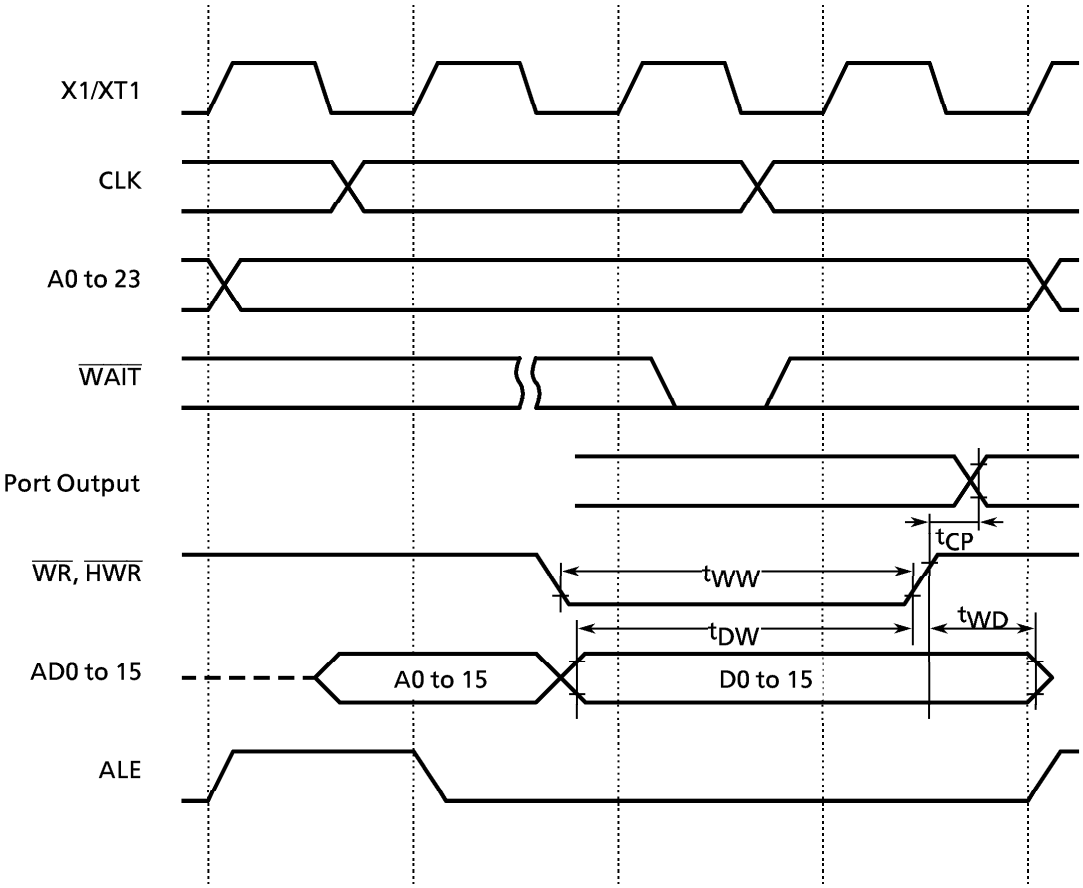
AC Measuring Conditions

- Output Level: High 0.7 × V_{CC}/Low 0.3 × V_{CC}, CL = 50 pF
- Input Level: High 0.9 × V_{CC}/Low 0.1 × V_{CC}

(1) Read Cycle


X1/XT1
CLK
A0 to 23
WAIT
Port Input
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tAWL
tCW
tAPH
tAPH2
tADH
tCA
tACH
tRR
tRAE
tACL
tLC
tRD
tADL
tHR
A0 to 15
D0 to 15
tAL
tLA
tCL
tLL

(2) Write Cycle



4.4 Serial Channel Timing

(1) I/O Interface Mode

① SCLK Input Mode

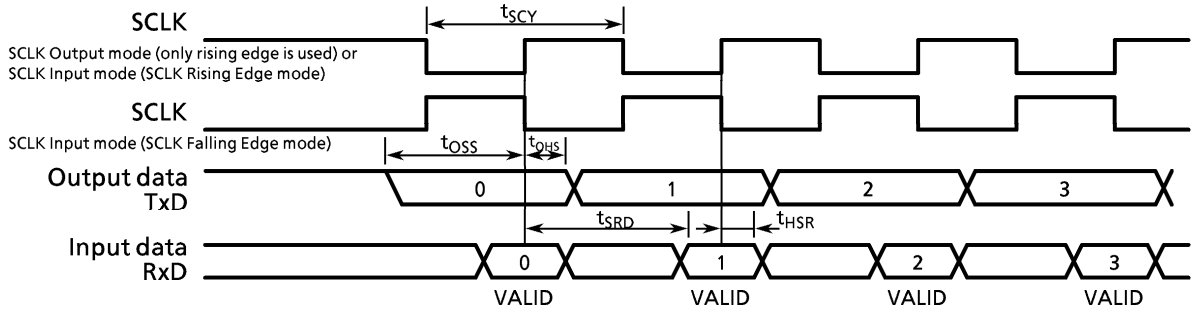
Parameter	Symbol	Variable		32.768 MHz (Note)		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK Cycle	t_{SCY}	16X		488 μs		1.28		0.8		μs
Output Data → Rising Edge or Falling Edge* of SCLK	t_{OSS}	$t_{SCY}/2 - 5X - 50$		91.5 μs		190		100		ns
SCLK Rising Edge or Falling Edge* → Output Data Hold	t_{OHS}	5X – 100		152 μs		300		150		ns
SCLK Rising Edge or Falling Edge* → Input Data Hold	t_{HSR}	0		0		0		0		ns
SCLK Rising Edge or Falling Edge* → Effective Data Input	t_{SRD}		$t_{SCY} - 5X - 100$		336 μs		780		450	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.
∗) The rising edge is used in SCLK Rising mode.
The falling edge is used SCLK Falling mode.

② SCLK Output Mode

Parameter	Symbol	Variable		32.768 MHz (Note)		10 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK Cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.28	655.36	0.8	409.6	μs
Output Data → SCLK Rising Edge	t_{OSS}	$t_{SCY} - 2X - 150$		427 μs		970		550		ns
SCLK Rising Edge→ Output Data Hold	t_{OHS}	2X – 80		60 μs		80		20		ns
SCLK Rising Edge→ Input Data Hold	t_{HSR}	0		0		0		0		ns
SCLK Rising Edge→ Effective Data Input	t_{SRD}		$t_{SCY} - 2X - 150$		428 μs		970		550	ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.



(2) UART Mode (SCLK0, 1 External Input)

Parameter	Symbol	Variable		32.768 kHz (Note)		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
SCLK Cycle	t_{SCY}	4x + 20		122 μs		340		220		ns
SCLK Low Level Pulse Width	t_{SCYL}	2x + 5		6 μs		165		105		ns
SCLK High Level Pulse Width	t_{SCYH}	2x + 5		6 μs		165		105		ns

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.

4.5 AD Conversion Characteristics (Vss = 0 V, AVcc = Vcc, AVss = Vss, Ta = – 40 to 85°C)

AVcc = Vcc, AV_{SS} = V_{SS}

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage (+)	V_{REFH}	V_{CC} = 5 V ± 10%	V_{CC} - 1.5V	V_{CC}	V_{CC}	V
		V_{CC} = 3 V ± 10%	V_{CC} - 0.2V	V_{CC}	V_{CC}	
Analog Reference Voltage (–)	V_{REFL}	V_{CC} = 5 V ± 10%	V_{SS}			
		V_{CC} = 3 V ± 10%	V_{SS}			
Analog Input Voltage Range	V_{AIN}		V_{REFL}		V_{REFH}	
Analog Current for Analog Reference Voltage <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)	V_{CC} = 5 V ± 10%		1.6	2.0	mA
		V_{CC} = 3 V ± 10%		1.0	1.5	
<VREFON> = 0		V_{CC} = 2.7 to 5.5 V		0.02	5.0	μA
Error (not including quantizing errors)	—	V_{CC} = 5 V ± 10%		± 1.0	± 3.0	LSB
		V_{CC} = 3 V ± 10%		± 1.0	± 5.0	

Note 1: $1LSB = (V_{REFH} - V_{REFL}) / 2^{10}$ [V]

Note 2: Minimum operation frequency
The operation of the AD converter is guaranteed only when fc (high-frequency oscillator) is used. (It is not guaranteed when fs is used.) Additionally, it is guaranteed when the clock frequency whith is selected by the clock gear is 4 MHz or more.

Note 3: The value I_{CC} includes the current which flows through the AV_{CC} pin.

4.6 LCD Driver Characteristics

Charge and Pump Characteristics	Symbol	Min	Typ.	Max	Unit
Reference input voltage	V_{L1}	0.9		1.83	V
Output voltage V2 pin	V_{L2}		2 × V_{L1}		V
V3 pin	V_{L3}		3 × V_{L1}		V
External capacity C0, C1	C_{PMP}	0.1		1.0	μF
V1 pin	C_{VL1}	0.1		1.0	μF
V2 pin	C_{VL2}	0.1		1.0	μF
V3 pin	C_{VL3}	0.1		1.0	μF

Note: Output voltage and External capacity are not loaded.

4.7 Event Counter (TI0, TI2, TI4, TI6, TI8 to B)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Cycle	t_{VCK}	8X + 100		740		500		ns
Low Level Clock Pulse Width	t_{VCKL}	4X + 40		360		240		ns
High Level Clock Pulse Width	t_{VCKH}	4X + 40		360		240		ns

4.8 Interrupt and Capture

(1) $\overline{NMI}$, INT0 to 4 interrupts, KEY interrupt

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Low Level Pulse Width	t_{INTAL}	4X		320		200		ns
High Level Pulse Width	t_{INTAH}	4X		320		200		ns

(2) INT7 to B interrupts, capture

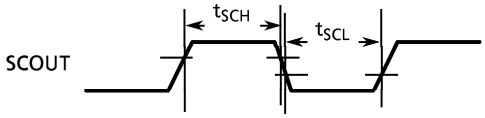
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Low Level Pulse Width	t_{INTBL}	4X + 100		420		300		ns
High Level Pulse Width	t_{INTBH}	4X + 100		420		300		ns

4.9 SCOUT pin AC Characteristics

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
High-Level Pulse Width V_{CC} = 5 V ± 10%	t_{SCH}	0.5X − 10		30		15		ns
High-Level Pulse Width V_{CC} = 3 V ± 10%		0.5X − 20		20		−	−	
Low-Level Pulse Width V_{CC} = 5 V ± 10%	t_{SCL}	0.5X − 10		30		15		ns
Low-Level Pulse Width V_{CC} = 3 V ± 10%		0.5X − 20		20		−	−	

Measurement condition

- Output level: High 2.2 V / Low 0.8 V, CL = 10 pF

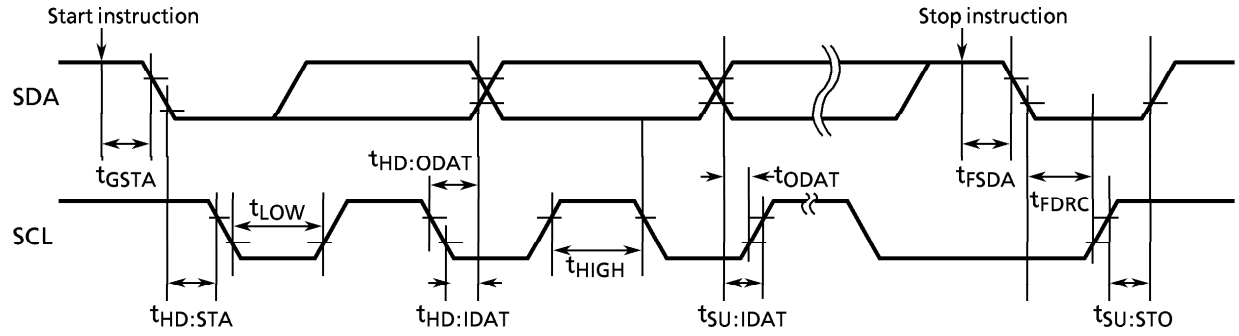


4.10 Timing Chart for Serial Bus Interface

(1) I^2C Bus Mode

Parameter	Symbol	Variable			Unit
		Min	Typ.	Max	
START instruction → SDA Falling Edge	t_{GSTA}	3X			s
Start Condition Hold Time	$t_{HD:STA}$	2^nX			s
SCL Low Level Pulse Width	t_{LOW}	2^nX			s
SCL High Level Pulse Width	t_{HIGH}	2^nX + 12X			s
Data Hold Time (Input)	$t_{HD:IDAT}$	0			ns
Data Setup Time (Input)	$t_{SU:IDAT}$	250			ns
Data Hold Time (Output)	$t_{HD:ODAT}$	7X		11X	s
Data Valid → SCL Rising Edge	t_{ODAT}		$2^nX - t_{HD:ODAT}$		s
STOP instruction → SDA Falling Edge	t_{FSDA}	3X			s
SDA Falling Edge → SCL Rising Edge	t_{FDRC}	2^nX			s
Stop Condition Hold Time	$t_{SU:STO}$	2^nX + 16X			s

Note: SBICR1<SCK2 to 0> sets n.



(2) Clock Synchronous 8-bit SIO Mode (Serial Bus Interface)

① SCK Input Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK Cycle	t_{SCY2}	2^5X		s
SCK Falling Edge → Output Data Hold	t_{OHS2}	6X		s
Output Data Valid → SCK Rising Edge	t_{OSS2}	t_{SCY2} − 6X		s
SCK Rising Edge → Input Data Hold	t_{HSR2}	6X		ns
Input Data Valid → SCK Rising Edge	t_{ISS2}	0		ns

② SCK Output Mode

Parameter	Symbol	Variable		Unit
		Min	Max	
SCK Cycle	t_{SCY2}	2^5X	$2^{11}X$	s
SCK Falling Edge → Output Data Hold	t_{OHS2}	2X		s
Output Data Valid → SCK Rising Edge	t_{OSS2}	t_{SCY2} − 2X		s
SCK Rising Edge → Input Data Hold	t_{HSR2}	2X		s
Input Data Valid → SCK Rising Edge	t_{ISS2}	0		ns