FAIRCHILD

SEMICONDUCTOR™

August 1984
Revised January 2000

MM74HC4066
Quad Analog Switch

General Description

The MM74HC4066 devices are digitally controlled analog switches utilizing advanced silicon-gate CMOS technology. These switches have low "ON" resistance and low "OFF" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the MM74HC4066 switches contain linearization circuitry which lowers the "ON" resistance and increases switch linearity. The MM74HC4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when LOW. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

■ Typical switch enable time: 15 ns
■ Wide analog input voltage range: 0–12V
■ Low "ON" resistance: 30 typ. (MM74HC4066)
■ Low quiescent current: 80 μA maximum (74HC)
■ Matched switch characteristics
■ Individual switch controls

Ordering Code:

| Order Number	Package Number	Package Description
MM74HC4066M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC4066SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4066MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4066N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Schematic Diagram
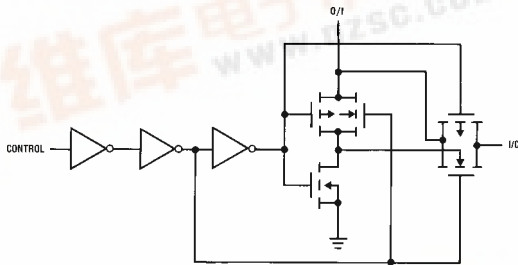
Connection Diagram

Top View
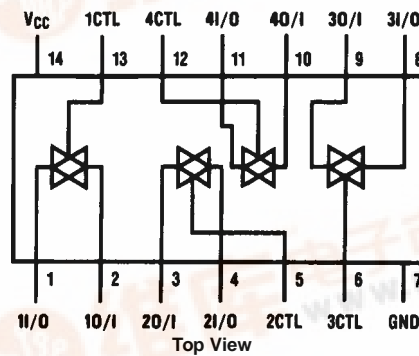
Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 9.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C Typ	T_A = 25°C Guaranteed Limits	T_A = −40 to 85°C Guaranteed Limits	T_A = −55 to 125°C Guaranteed Limits	Units
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	5.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			9.0V		2.7	2.7	2.7	V
			12.0V		3.6	3.6	3.6	V
R_{ON}	Maximum "ON" Resistance (Note 5)	V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} to GND (Figure 1)	4.5V	100	170	200	220	Ω
			9.0V	50	85	105	110	Ω
			12.0	30	70	85	90	Ω
		V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC}or GND (Figure 1)	2.0V	120	180	215	240	Ω
			4.5V	50	80	100	120	Ω
			9.0V	35	60	75	80	Ω
			12.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL} = V_{IH} V_{IS} = V_{CC} to GND	4.5V	10	15	20	20	Ω
			9.0V	5	10	15	15	Ω
			12.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN} = V_{CC} or GND V_{CC} = 2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{CTL} = V_{IL} (Figure 3)	6.0V	10	±60	±600	±600	nA
			9.0V	15	±80	±800	±800	nA
			12.0V	20	±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{IS} = V_{CC} to GND V_{CTL} = V_{IH} V_{OS} = OPEN (Figure 2)	6.0V	10	±40	±150	±150	nA
			9.0V	15	±50	±200	±200	nA
			12.0V	20	±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA
			9.0V		4.0	40	80	μA
			12.0V		8.0	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case on resistance (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–GND) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V V_{EE} = 0V–12V, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		T_A = –40 to 85°C	T_A = –55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V	25	50	30	75	ns
			4.5V	5	10	13	15	ns
			9.0V	4	8	10	12	ns
			12.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	2.0V	30	100	125	150	ns
			4.5V	12	20	25	30	ns
			9.0V	6	12	15	18	ns
			12.0V	5	10	13	15	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	R_L = 1 kΩ	2.0V	60	168	210	252	ns
			4.5V	25	36	45	54	ns
			9.0V	20	32	40	48	ns
			12.0V	15	30	38	45	
f_{MAX}	Minimum Frequency Response (Figure 7) 20 log (V_O/V_I) = –3 dB	R_L = 600Ω V_{IS} = 2 V_{PP} at (V_{CC}/2) (Note 6) (Note 7)	4.5V	40				MHz
			9.0V	100				MHz
	Crosstalk Between any Two Switches (Figure 8)	R_L = 600Ω, F = 1 MHz (Note 7) (Note 8)	4.5V	–52				dB
			9.0V	–50				dB
	Peak Control to Switch Feedthrough Noise (Figure 9)	R_L = 600Ω, F = 1 MHz C_L = 50 pF	4.5V	100				mV
			9.0V	250				mV
	Switch OFF Signal Feedthrough Isolation (Figure 10)	R_L = 600Ω, F = 1 MHz $V_{(CT)}V_{IL}$ (Note 7) (Note 8)	4.5V	–42				dB
			9.0V	–44				dB
THD	Total Harmonic Distortion (Figure 11) V_{IS} = 4 V_{PP} V_{IS} = 8 V_{PP}	R_L = 10 kΩ, C_L = 50 pF, F = 1 kHz	4.5V	.013				%
			9.0V	.008				%
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			20				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND		0.5				pF
C_{PD}	Power Dissipation Capacitance			15				pF

Note 6: Adjust 0 dBm for F = 1 kHz (Null R_L/R_{ON} Attenuation).

Note 7: V_{IS} is centered at V_{CC}/2.

Note 8: Adjust input for 0 dBm.

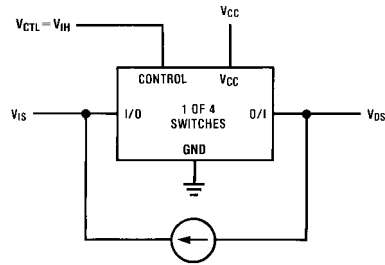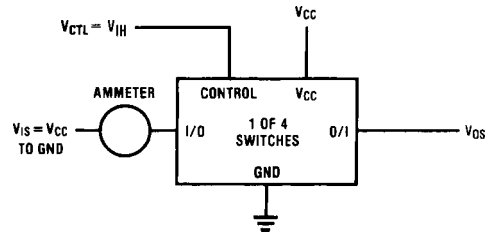# AC Test Circuits and Switching Time Waveforms

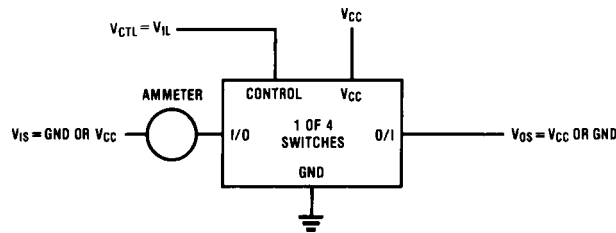FIGURE 1. "ON" Resistance

FIGURE 2. "ON" Channel Leakage Current
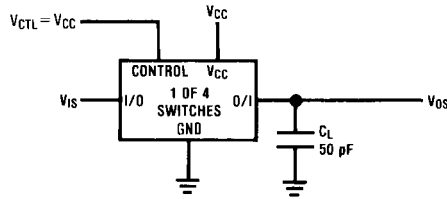
FIGURE 3. "OFF" Channel Leakage Current

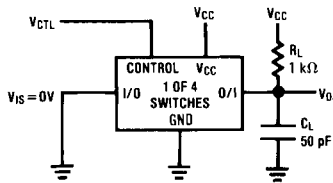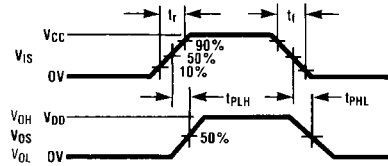FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

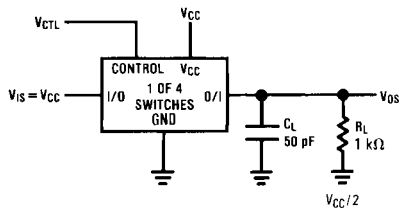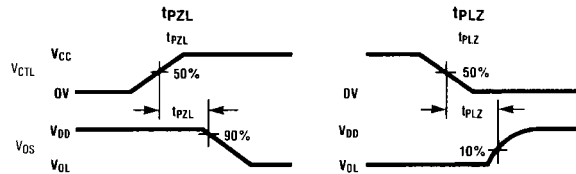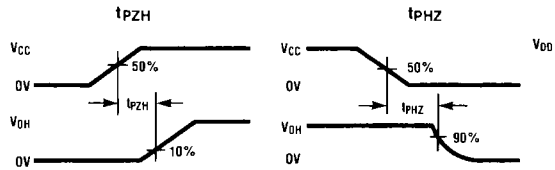FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

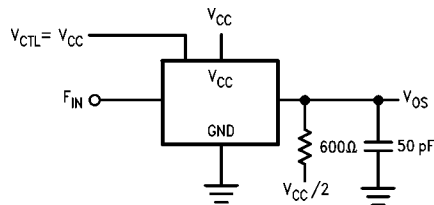# AC Test Circuits and Switching Time Waveforms (Continued)
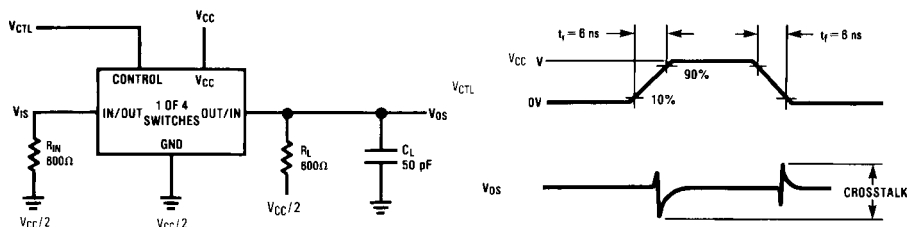
FIGURE 7. Frequency Response

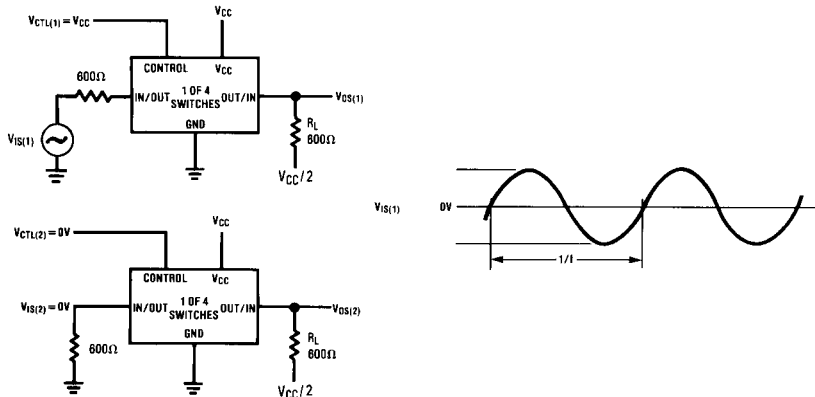**FIGURE 8. Crosstalk: Control Input to Signal Output**
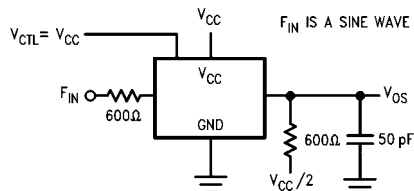
FIGURE 9. Crosstalk Between Any Two Switches
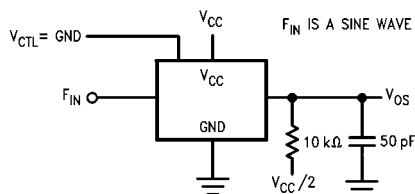
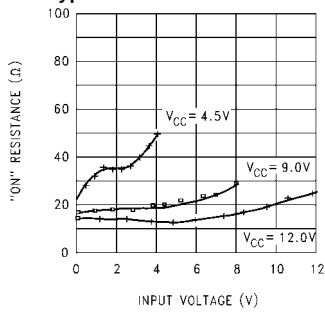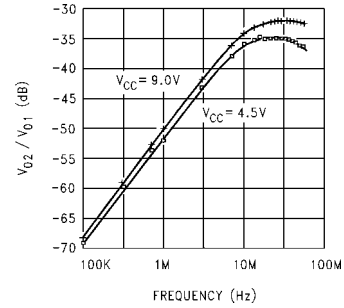**FIGURE 10. Switch OFF Signal Feedthrough Isolation**

FIGURE 11. Sinewave Distortion

Typical Performance Characteristics

Typical "ON" Resistance

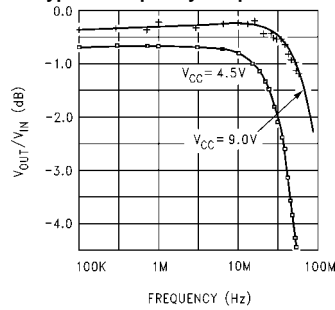### Typical Crosstalk Between Any Two Switches
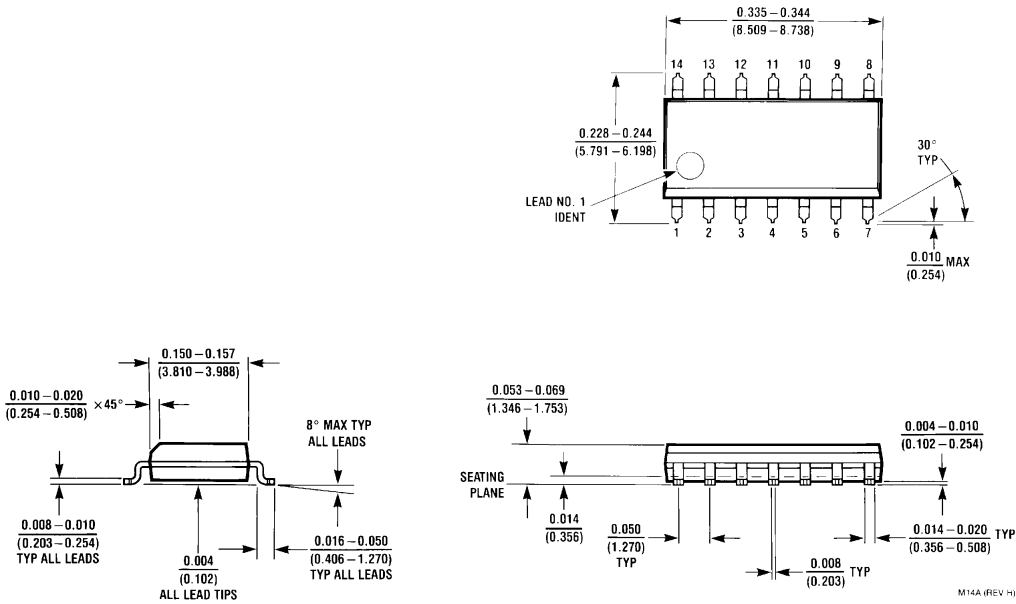

Typical Frequency Response

Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} cur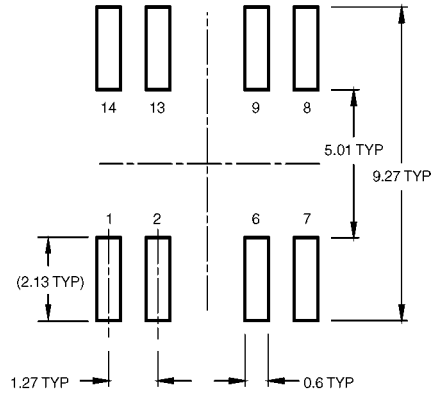rent when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO. 1
IDENT

1 2 3 4 5 6 7

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020 TYP
(0.356 − 0.508)

M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A

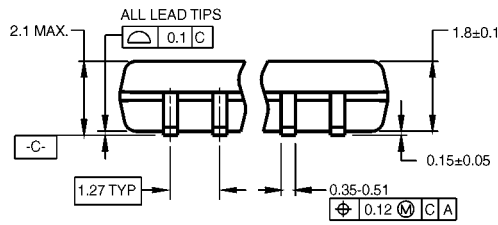## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1
-A-

1.1 TYP

14   8

7.8

3.9

5.3±0.1
-B-

PIN #1 IDENT.   1   7

0.2 C B A
ALL LEAD TIPS

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

1   2   6   7

(2.13 TYP)

1.27 TYP   0.6 TYP

ALL LEAD TIPS
2.1 MAX.   0.1 C

-C-

1.27 TYP

1.8±0.1

0.15±0.05

0.35-0.51

0.12 M C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25
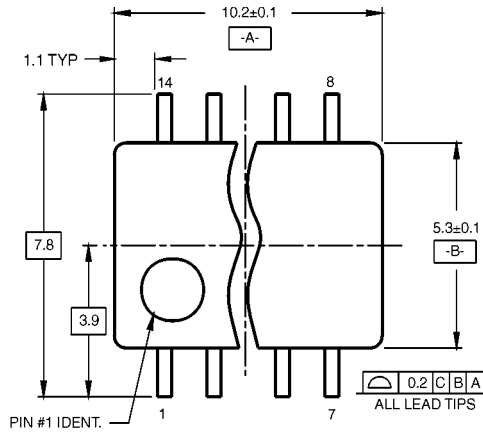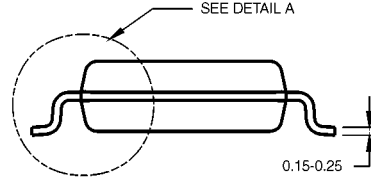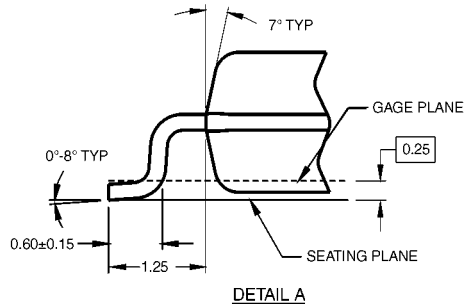
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
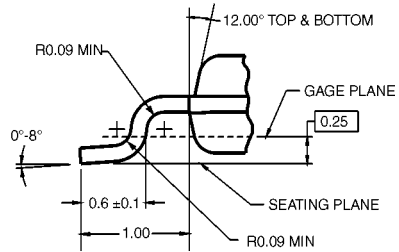
M14DRevB1

7° TYP

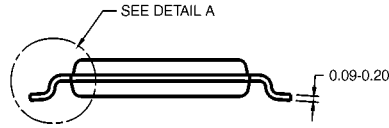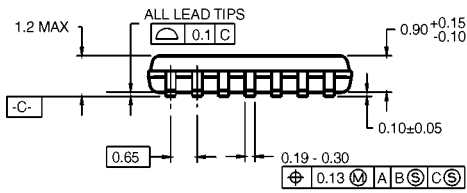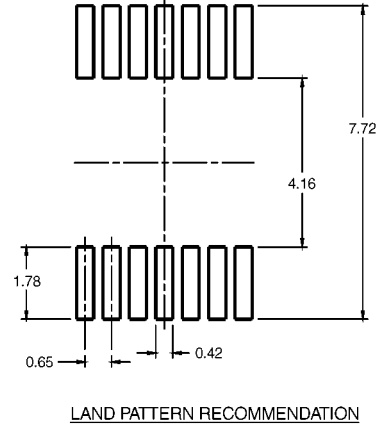GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A

14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

5.0±0.1
-A-

0.43 TYP

14

8

6.4

3.2

4.4±0.1
-B-

PIN #1 IDENT.

1

7

△ 0.2 C B A
ALL LEAD TIPS

7.72

4.16

1.78

0.65

0.42

LAND PATTERN RECOMMENDATION

1.2 MAX

ALL LEAD TIPS
△ 0.1 C

0.90 +0.15 -0.10

-C-

0.65

0.19 - 0.30

0.10±0.05

⊕ 0.13 Ⓜ A BⓈ CⓈ

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.09 MIN

GAGE PLANE

0.25

0°-8°

0.6 ±0.1

SEATING PLANE

1.00

R0.09 MIN

DETAIL A
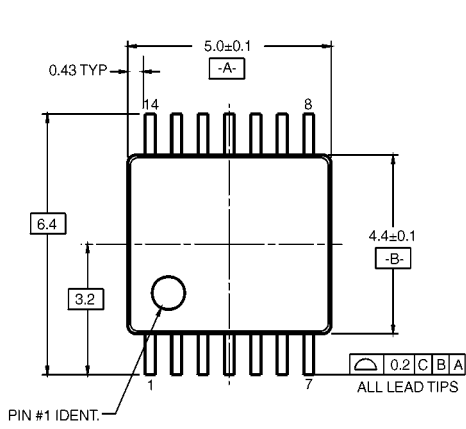
NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
   REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND
   TIE BAR EXTRUSIONS.
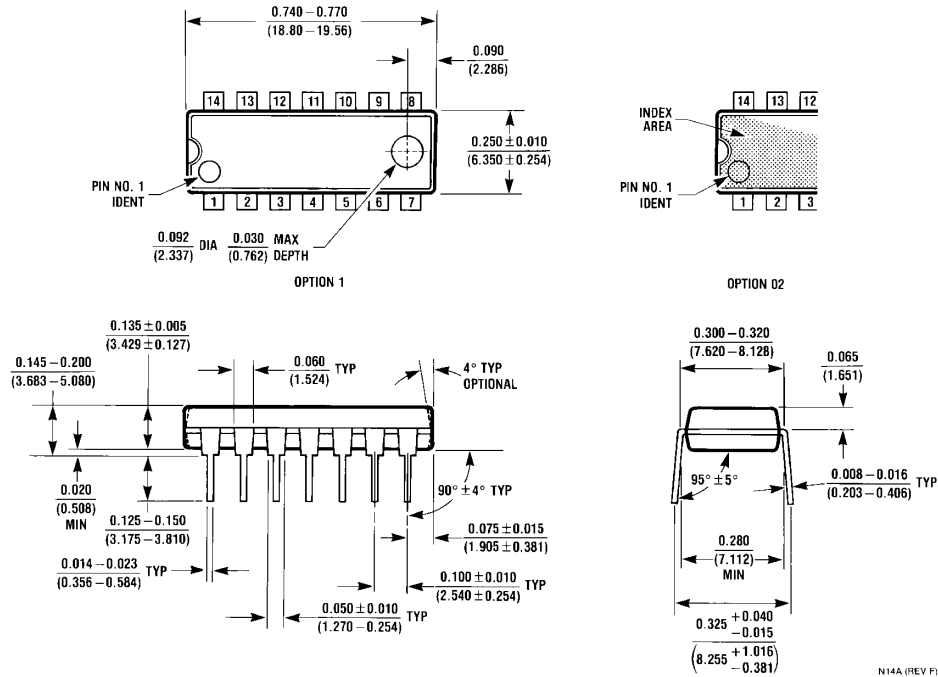D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC14RevC3

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.740 − 0.770
(18.80 − 19.56)

0.090
(2.286)

14 13 12 11 10 9 8

0.250 ± 0.010
(6.350 ± 0.254)

PIN NO. 1
IDENT

1 2 3 4 5 6 7

0.092
(2.337) DIA   0.030
(0.762) MAX DEPTH

OPTION 1

INDEX
AREA

14 13 12

PIN NO. 1
IDENT

1 2 3

OPTION 02

0.135 ± 0.005
(3.429 ± 0.127)

0.145 − 0.200
(3.683 − 5.080)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.020
(0.508)
MIN

0.125 − 0.150
(3.175 − 3.810)

90° ± 4° TYP

0.075 ± 0.015
(1.905 ± 0.381)

0.014 − 0.023
(0.356 − 0.584) TYP

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.050 ± 0.010
(1.270 − 0.254) TYP

0.300 − 0.320
(7.620 − 8.128)

0.065
(1.651)

95° ± 5°

0.008 − 0.016
(0.203 − 0.406) TYP

0.280
(7.112)
MIN

0.325 +0.040
−0.015

(8.255 +1.016
−0.381)

N14A (REV F)

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com