FAIRCHILD
SEMICONDUCTOR™

September 1983
Revised February 1999

MM74HC245A
Octal 3-STATE Transceiver

General Description

The MM74HC245A 3-STATE bidirectional buffer utilizes advanced silicon-gate CMOS technology, and is intended for two-way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device has an active LOW enable input $\overline{G}$ and a direction control input, DIR. When DIR is HIGH, data flows from the A inputs to the B outputs. When DIR is LOW, data flows from the B inputs to the A outputs. The MM74HC245A transfers true data from one bus to the other.

This device can drive up to 15 LS-TTL Loads, and does not have Schmitt trigger inputs. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 µA maximum (74 HC)
- 3-STATE outputs for connection to bus oriented systems
- High output drive: 6 mA (minimum)
- Same as the 645

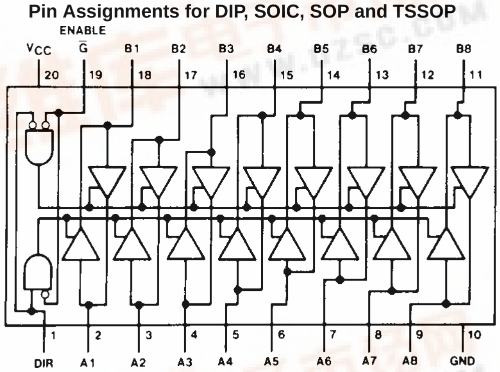
Ordering Code:

Order Number	Package Number	Package Description
MM74HC245AWM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC245ASJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC245AMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC245AN	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



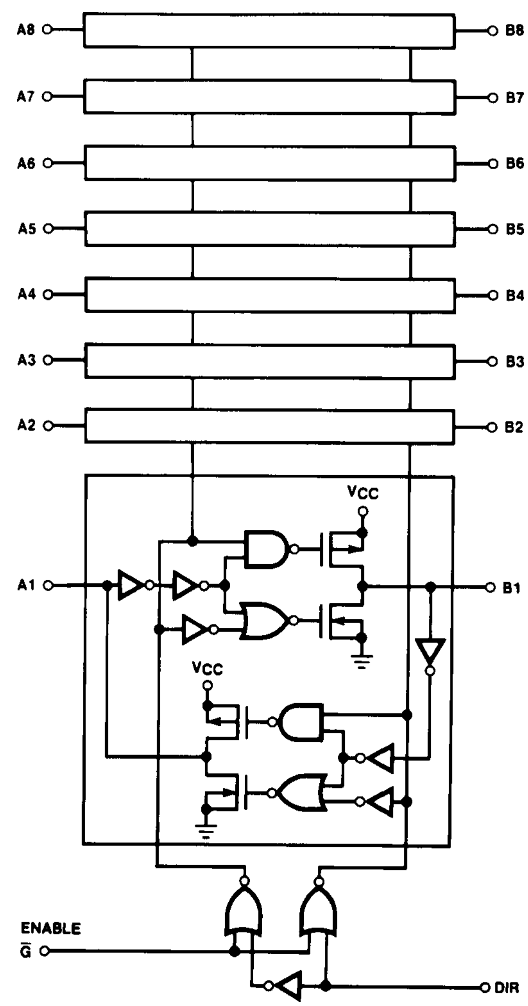
Top View

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = HIGH Level
L = LOW Level
X = Irrelevant

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	–0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	–1.5 to V_{CC} +1.5V
DC Input/Output Voltage (V_{IN}, V_{OUT})	–0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	–65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	–40	+85	°C
Input Rise/Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: –12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		T_A = –40 to 85°C	T_A = –55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	$V_{IN} = V_{CC}$ to GND	6.0V		±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum 3-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND Enable $\overline{G} = V_{IH}$	6.0V		±0.5	±5.0	±10	µA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0\ \mu A$	6.0V		8.0	80	160	µA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC} = 5V$, $T_A = 25°C$, $t_r = t_f = 6ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 45$ pF	12	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ $C_L = 45$ pF	24	35	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 5$ pF	18	25	ns

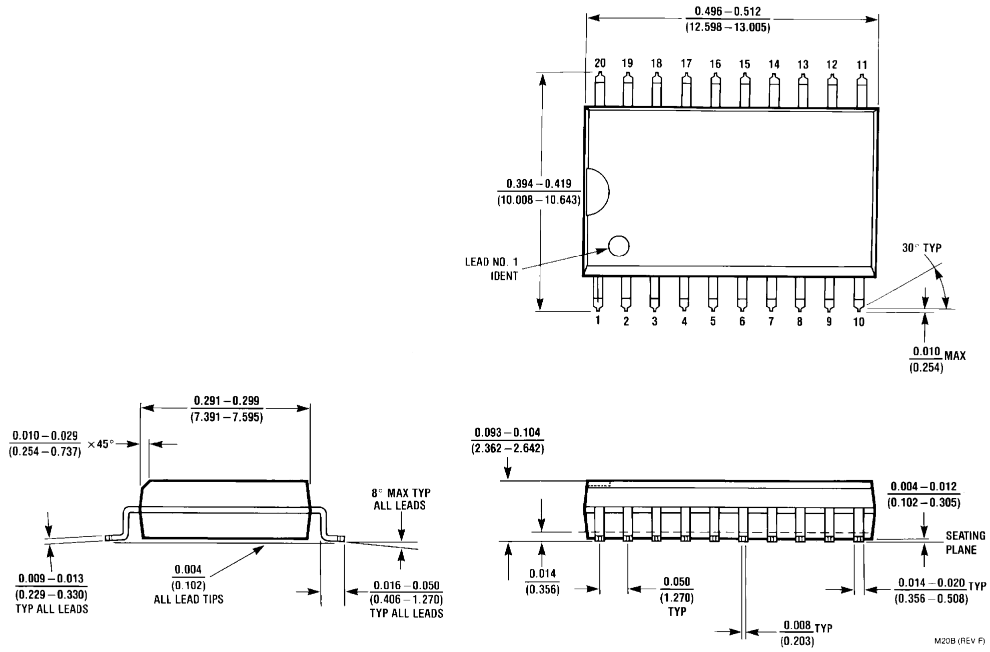
AC Electrical Characteristics

$V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6ns$ (unless otherwise specified)

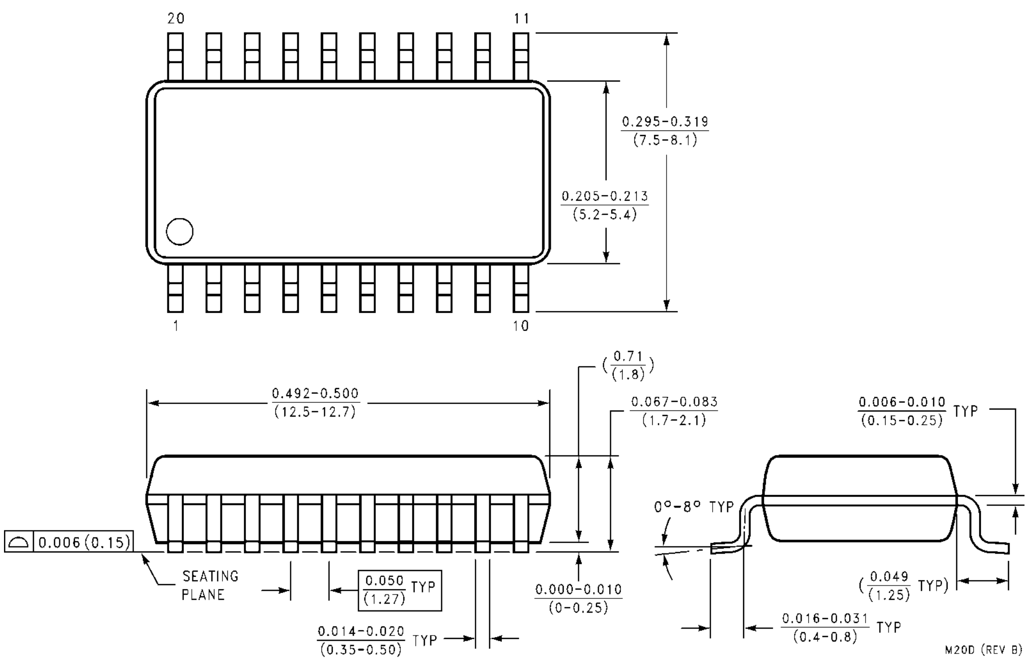
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 50$ pF	2.0V	31	90	113	135	ns
		$C_L = 150$ pF	2.0V	41	96	116	128	ns
		$C_L = 50$ pF	4.5V	13	18	23	27	ns
		$C_L = 150$ pF	4.5V	17	22	28	33	ns
		$C_L = 50$ pF	6.0V	11	15	19	23	ns
		$C_L = 150$ pF	6.0V	14	19	23	28	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ						
		$C_L = 50$ pF	2.0V	71	190	240	285	ns
		$C_L = 150$ pF	2.0V	81	240	300	360	ns
		$C_L = 50$ pF	4.5V	26	38	48	57	ns
		$C_L = 150$ pF	4.5V	31	48	60	72	ns
		$C_L = 50$ pF	6.0V	21	32	41	48	ns
		$C_L = 150$ pF	6.0V	25	41	51	61	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 50$ pF	2.0V	39	135	169	203	ns
			4.5V	20	27	34	41	ns
			6.0V	18	23	29	34	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time	C_L=50 pF	2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$G = V_{IL}$		50				pF
		$\overline{G} = V_{IH}$		5				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

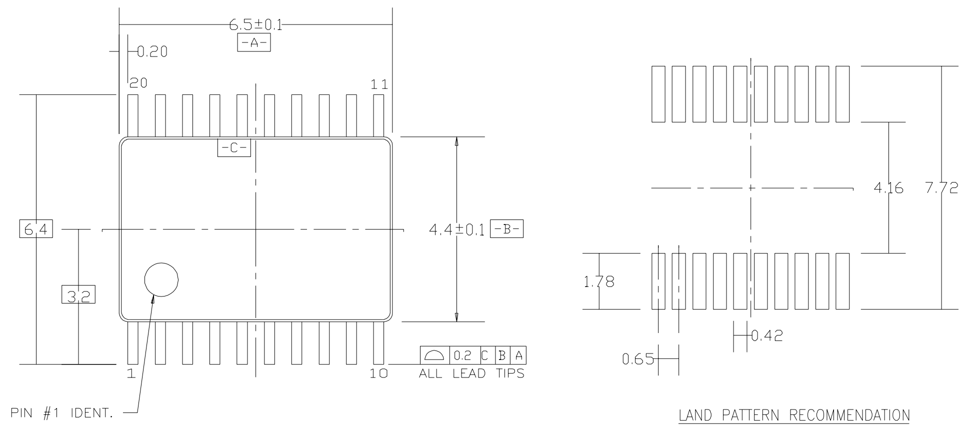


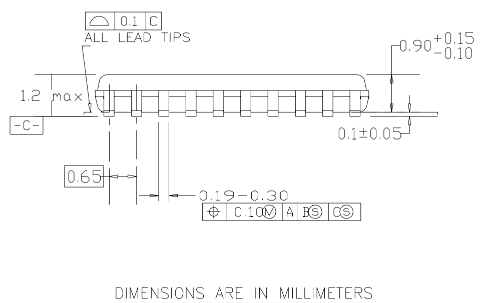
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

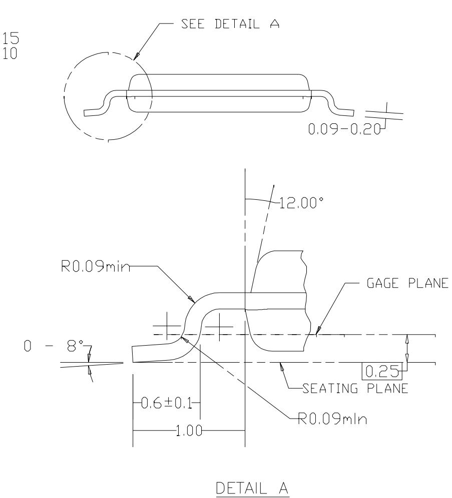


20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)







NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

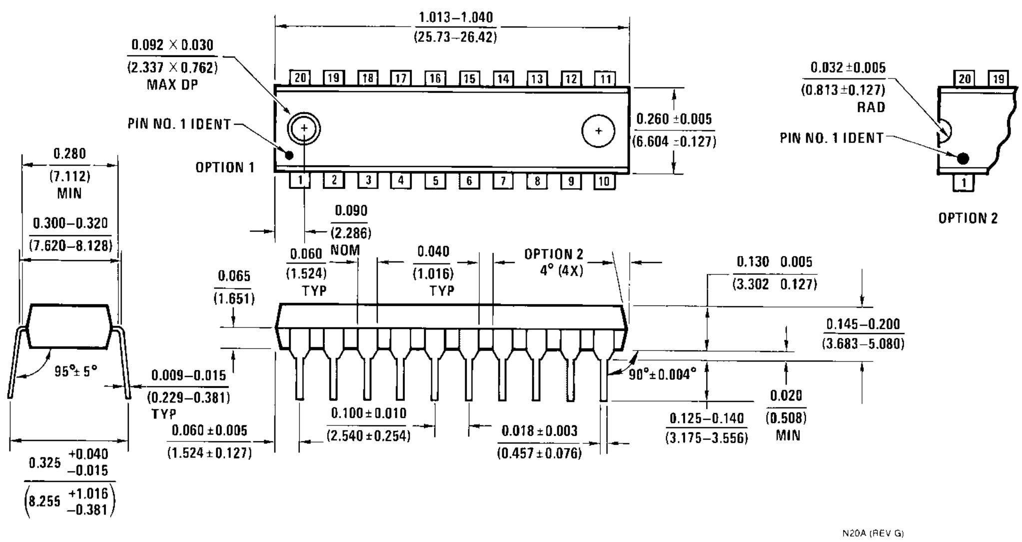
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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