

September 1983  
Revised February 1999

## MM74HC174

### Hex D-Type Flip-Flops with Clear

**General Description**

The MM74HC174 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC174 is functionally as well as pin compatible to the 74LS174. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

**Features**

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1  $\mu$ A maximum
- Low quiescent current: 80  $\mu$ A (74HC Series)
- Output drive: 10 LSTTL loads

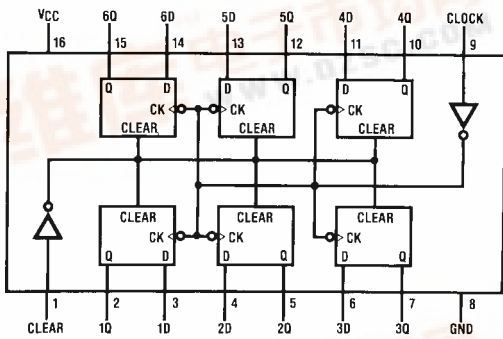
**Ordering Code:**

Order Number	Package Number	Package Description
MM74HC174M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC174MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC174N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

**Connection Diagram**

Pin Assignments for DIP, SOIC, SOP and TSSOP



**Truth Table**

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	$Q_0$

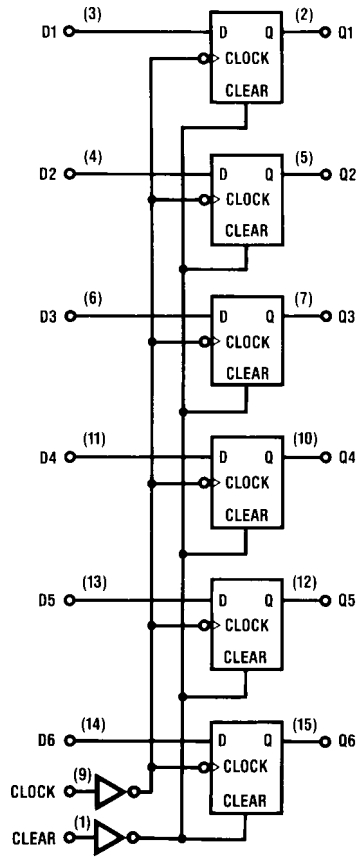
H = HIGH Level (steady state)  
L = LOW Level (steady state)  
X = Don't Care  
↑ = Transition from LOW-to-HIGH level  
 $Q_0$  = The level of Q before the indicated steady state input conditions were established.

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### Logic Diagram





### AC Electrical Characteristics

 $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15pF, t_r = t_f = 6 ns$ 

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency		50	30	MHz
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay, Clock or Clear to Output		16	30	ns
$t_{REM}$	Minimum Removal Time, Clear to Clock		-2	5	ns
$t_S$	Minimum Setup Time Data to Clock		10	20	ns
$t_H$	Minimum Hold Time Clock to Data		0	5	ns
$t_W$	Minimum Pulse Width Clock or Clear		10	16	ns

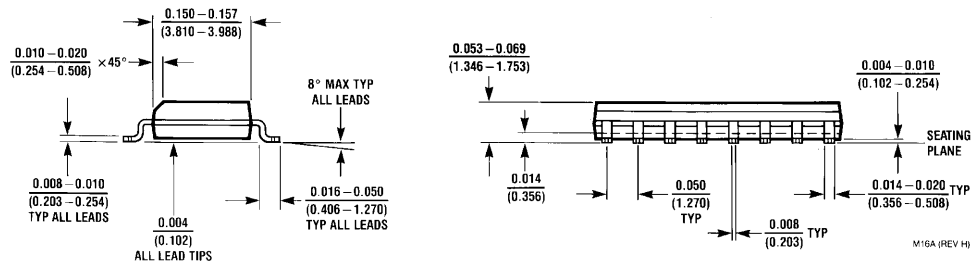
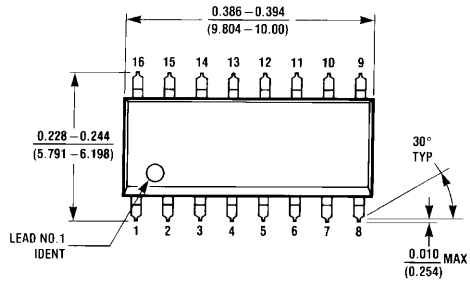
### AC Electrical Characteristics

 $C_L = 50 pF, t_r = t_f = 6 ns$  (unless otherwise specified)

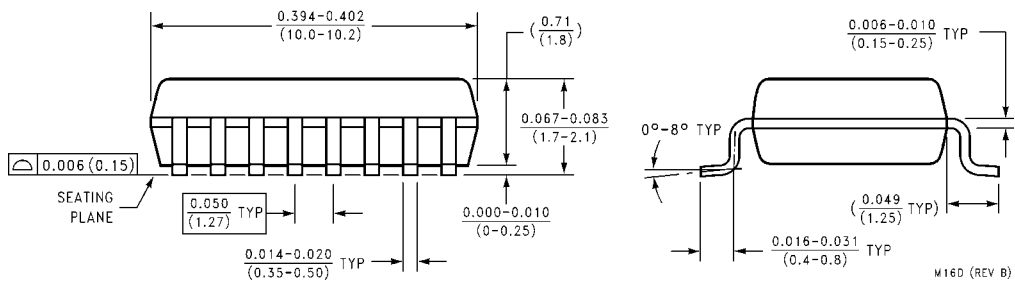
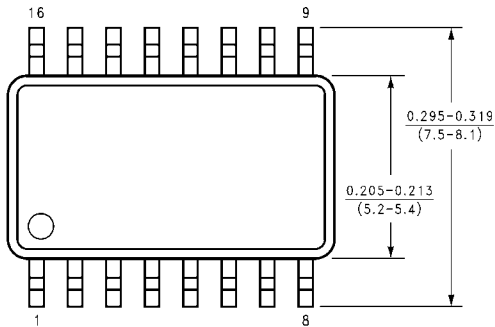
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			Units	
				Typ	Guaranteed Limits			
$f_{MAX}$	Maximum Operating Frequency		2.0V	5	4	3	MHz	
			4.5V	27	21	18	MHz	
			6.0V	31	24	20	MHz	
$t_{PHL}, t_{PLH}$	Maximum Propagation Delay Clock or Clear to Output		2.0V	55	165	206	248	ns
			4.5V	18	33	41	49	ns
			6.0V	16	28	35	42	ns
$t_{REM}$	Minimum Removal Time Clear to Clock		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
$t_S$	Minimum Setup Time Data to Clock		2.0V	42	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	10	17	21	25	ns
$t_H$	Minimum Hold Time Clock to Data		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
$t_W$	Minimum Pulse Width Clock or Clear		2.0V	35	80	106	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
$t_{TLH}, t_{THL}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
$t_r, t_f$	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
$C_{PD}$	Power Dissipation Capacitance (Note 5)	(per package)		136			pF	
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

**Physical Dimensions** inches (millimeters) unless otherwise noted

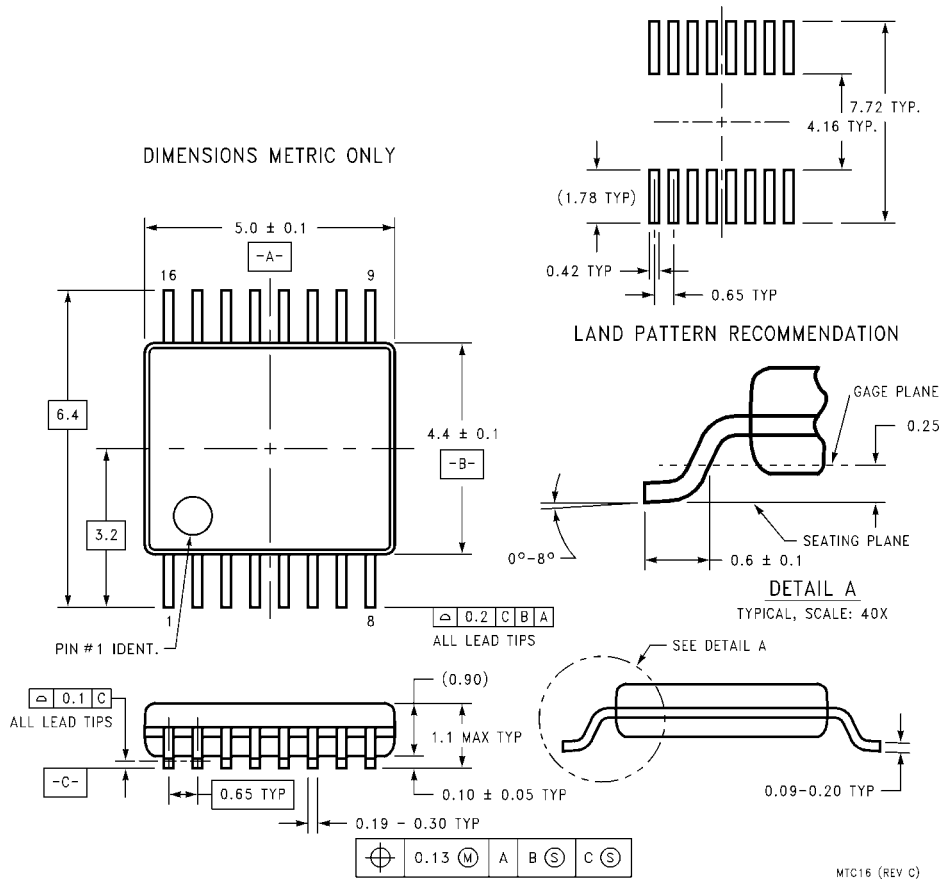


**16-Lead Small Outline Integrated Circuit (SOIC) JEDEC MS-012, 0.150" Narrow Package Number M16A**



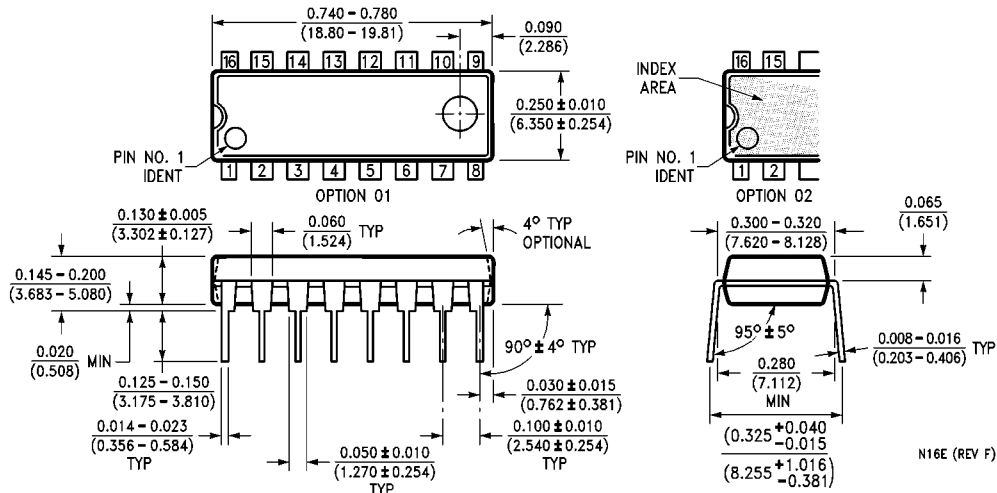
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E**

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