

September 1983

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SEMICONDUCTOR

MM74HC174 Hex D-Type Flip-Flops with Clear

General Description

The MM74HC174 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flipflops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC174 is functionally as well as pin compatible to the 74LS174. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

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Features

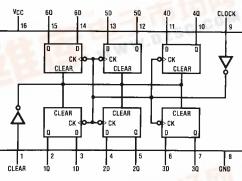
- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74HC Series)
- Output drive: 10 LSTTL loads

Ordering Code:

Order Number	Package Number	ackage Number Package Description				
MM74HC174M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow				
MM74HC174SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide				
MM74HC174MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide				
MM74HC174N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide				
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.						
		WWW.				

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Truth Table

(Each Flip-Flop)							
		Outputs					
	Clear	Clock	D	Q			
	L	Х	Х	L			
	Н	Ŷ	Н	Н			
	н	↑	L	L			
	н	L	Х	Q ₀			

H = HIGH Level (steady state)

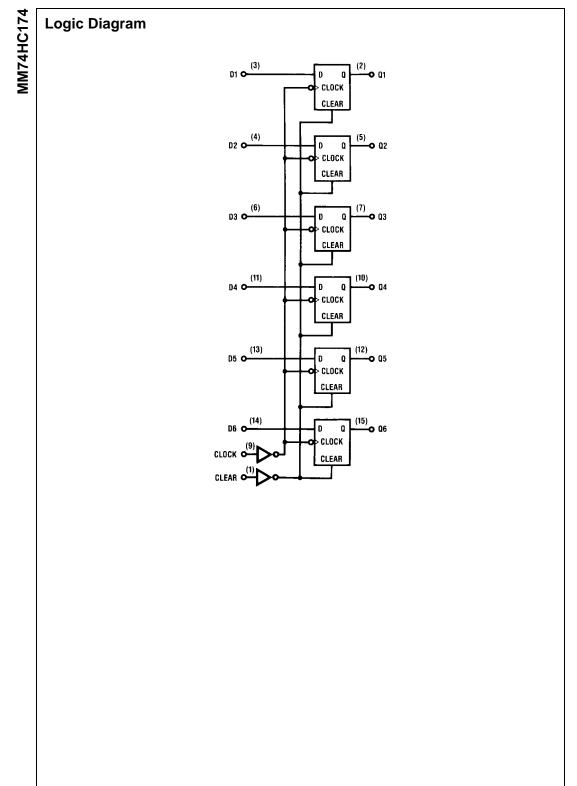
L = LOW Level (steady state) X = Don't Care

↑ = Transition from LOW-to-HIGH level

Q0 = The level of Q before the indicated steady state input conditions were established.







Absolute Maximum Ratings(Note 1) (Note 2)

Recommended Operating Conditions

Supply Voltage (V _{CC})	-0.5 to +7.0V
DC Input Voltage (V _{IN})	-1.5 to $V_{CC}{+}1.5V$
DC Output Voltage (V _{OUT})	–0.5 to V_{CC} +0.5V
Clamp Diode Current (I _{IK} , I _{OK})	±20 mA
DC Output Current, per pin (I _{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I _{CC})	±50 mA
Storage Temperature Range (T _{STG})	$-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation (P _D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (TL)	
(Soldering 10 seconds)	260°C

	Min	Max	Units	
Supply Voltage (V _{CC})		6	V	
DC Input or Output Voltage				
(V _{IN} , V _{OUT})	0	V_{CC}	V	
Operating Temperature Range (T _A)		+85	°C	
Input Rise or Fall Times				
$(t_r, t_f) V_{CC} = 2.0 V$		1000	ns	
$V_{CC} = 4.5V$		500	ns	
$V_{CC} = 6.0V$		400	ns	
Note 1: Absolute Maximum Patings are those v	alues he	wood wh	ich dam-	

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground. Note 3: Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{cc}	T _A = 25°C		$T_{A}=-40$ to $85^{\circ}C$	$T_{A}=-55$ to $125^{\circ}C$	Units
Symbol			•cc	Тур		Guaranteed Limits		Units
VIH	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
VIL	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH} \text{ or } V_{IL}$						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	160	μA
	Supply Current	$I_{OUT} = 0 \ \mu A$						

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{O2}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

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AC Electrical Characteristics

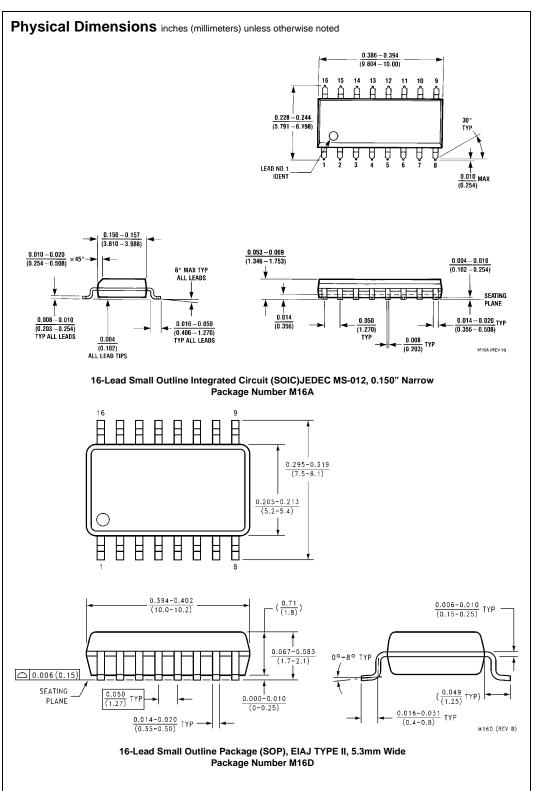
V _{CC} = 5V, T _A =	= 25° C, C _L = 15pF, t _r = t _f = 6 ns				
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
f _{MAX}	Maximum Operating		50	30	MHz
	Frequency				
t _{PHL} , t _{PLH}	Maximum Propagation		16	30	ns
	Delay, Clock or Clear to Output				
t _{REM}	Minimum Removal Time,		-2	5	ns
	Clear to Clock				
t _S	Minimum Setup Time		10	20	ns
	Data to Clock				
t _H	Minimum Hold Time		0	5	ns
	Clock to Data				
t _W	Minimum Pulse Width		10	16	ns
	Clock or Clear				

AC Electrical Characteristics

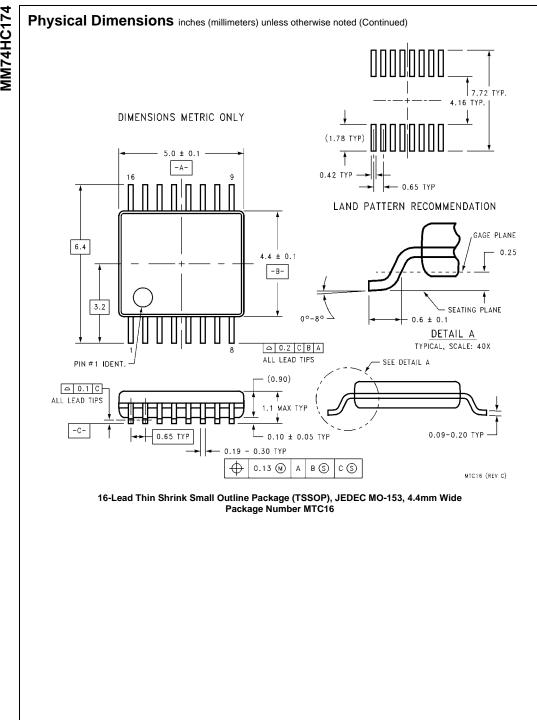
 $C_{L} = 50 \text{ pF}, t_{r} = t_{f} = 6 \text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	v _{cc}	T _A = 25°C		$T_A = -40$ to $85^{\circ}C$	$T_A = -55$ to $125^{\circ}C$	Units
			•cc	Тур		Guaranteed L	imits	Units
f _{MAX}	Maximum Operating		2.0V		5	4	3	MHz
	Frequency		4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t _{PHL} , t _{PLH}	Maximum Propagation		2.0V	55	165	206	248	ns
	Delay Clock or Clear to Output		4.5V	18	33	41	49	ns
			6.0V	16	28	35	42	ns
t _{REM}	Minimum Removal Time		2.0V	1	5	5	5	ns
	Clear to Clock		4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
ts	Minimum Setup Time		2.0V	42	100	125	150	ns
	Data to Clock		4.5V	12	20	25	30	ns
			6.0V	10	17	21	25	ns
t _H	Minimum Hold Time		2.0V	1	5	5	5	ns
	Clock to Data		4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t _W	Minimum Pulse Width		2.0V	35	80	106	120	ns
	Clock or Clear		4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
t _{TLH} , t _{THL}	Maximum Output Rise		2.0V	30	75	95	110	ns
	and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t _r , t _f	Maximum Input Rise and		2.0V		1000	1000	1000	ns
	Fall Time		4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C _{PD}	Power Dissipation	(per package)		136				pF
	Capacitance (Note 5)							
CIN	Maximum Input	T		5	10	10	10	pF
	Capacitance							

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.



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