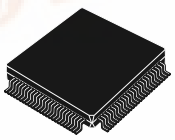
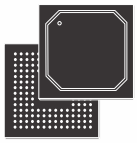
STLC90115
STLC90114

ZipperWire™ VDSL DMT Chip Set

PRODUCT BRIEF





TQFP100 **BGA416**

ORDERING NUMBERS:

STLC90114 **STLC90115**

1 FEATURES

- Adaptive frequency-domain equalization for better robustness in environment with bridged-taps.
- Applicable to both ends of loop: LT and NT.
- Protection against 250µs duration impulsive noises thanks to Programmable Reed-Solomon Codec RS (N, K) and configurable triangular interleaver.
- Implements Discrete Multitone (DMT) modulation and Digital Frequency Division Duplexing (FDD) for deployment flexibility.
- Embedded Operation Channel messages (EOC) for continuous and on-line monitoring on the communication link between LT and NT.
- Support all frequency band plans (998, 997 and Fx) specified in ETSI, ANSI and ITU-T standard draft documents.
- Fast and/or slow data-path selectable at start-up.
- Selection of frequency band plan by software under Network Management (NM) control.
- ATM Transmission Convergence layer (ATM-TC) with Utopia interface (level 2).
- Support analogue bandwidth up to 12 MHz with an embedded 4096-tone IFFT/FFT processor.
- 64kps user rate granularity.
- Embedded modem control Software for line parameters set-up, communication link initialization, show time monitoring and telemetry information collection (BER, SNR, standard deviation).
- Generation of deep frequency notches under NM control.
- Mapping/demapping functions supporting constellation size up to 16384 points (14 bits).
- Protection against two simultaneous; RF HAM ingress
- Adaptive bit-loading algorithm for maximal use of the channel capacity.
- Accurate PSD monitoring and adaptation to comply to reference PSD masks specified in ETSI and ANSI standard draft documents.
- Control and Maintenance via a Operation and Maintenance API from an external controller true the embedded CTRL-E interface.

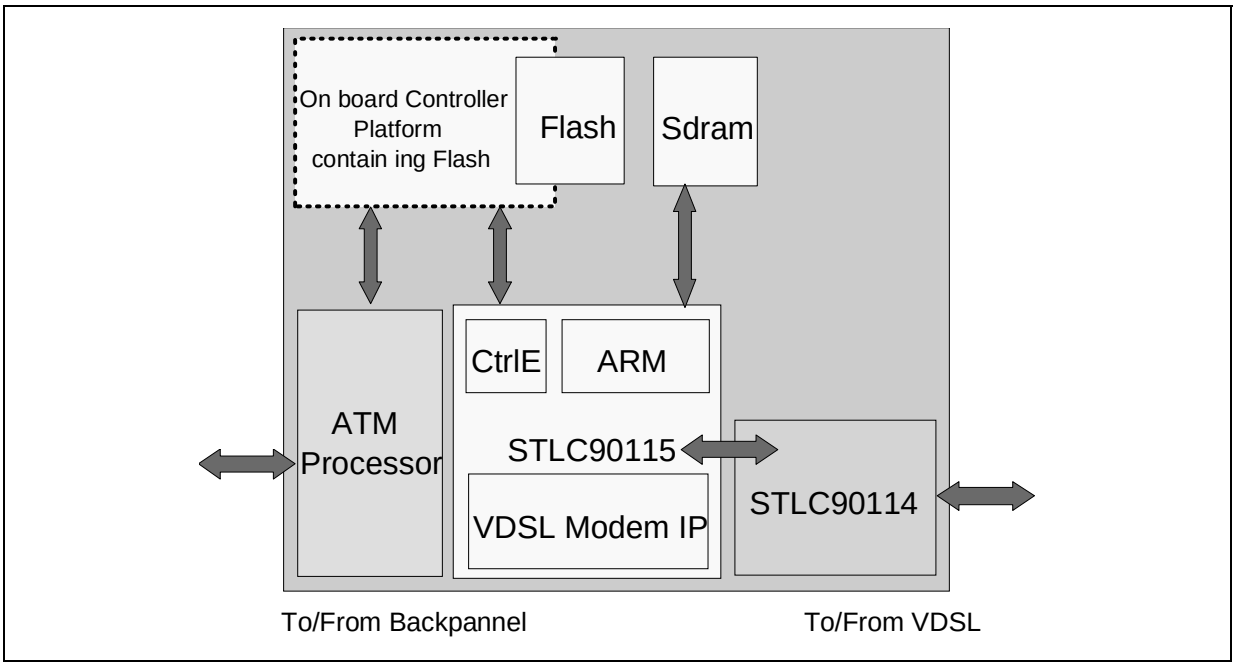
2 APPLICATIONS

- Central office and customer premises equipment
- DSL access Multiplexers
- Integrated access devices

3 GENERAL BLOCK DIAGRAM

An on-board-controller platform has complete control over the configuration. Figure 1 shows a typical configuration. This on-board-controller platform also contains the Flash with the VDSL software.

Figure 1. A typical configuration of an on-board controller platform.



The STLC90115 includes an internal ARM processor core connected to an external SDRAM. The boot process will be under control of the external OBC who will use the code from its Flash to initialize the SDRAM.

- **ATM interface:** Utopia "level 2" interface is integrated with the STLC90115 interface
- **Flash memory:** interfaces to an external flash memory.
- **SDRAM controller:** interfaces to an external SDRAM memory.
- **General Purpose I/O (GPIO):** ports that can be driven or read by the OBC

4 THE ZIPPERWIRE VDSL MODEM CHIPSET

ZipperWire is a two-chip VDSL Modem Transceiver with embedded transceiver controller. The kit also includes the necessary modem firmware running on the Transceiver Controller. The chipset directly interfaces with ATM systems to allow ATM traffic to be transported at high speed on copper pairs with minimum overhead.

4.1 The Modem Environment

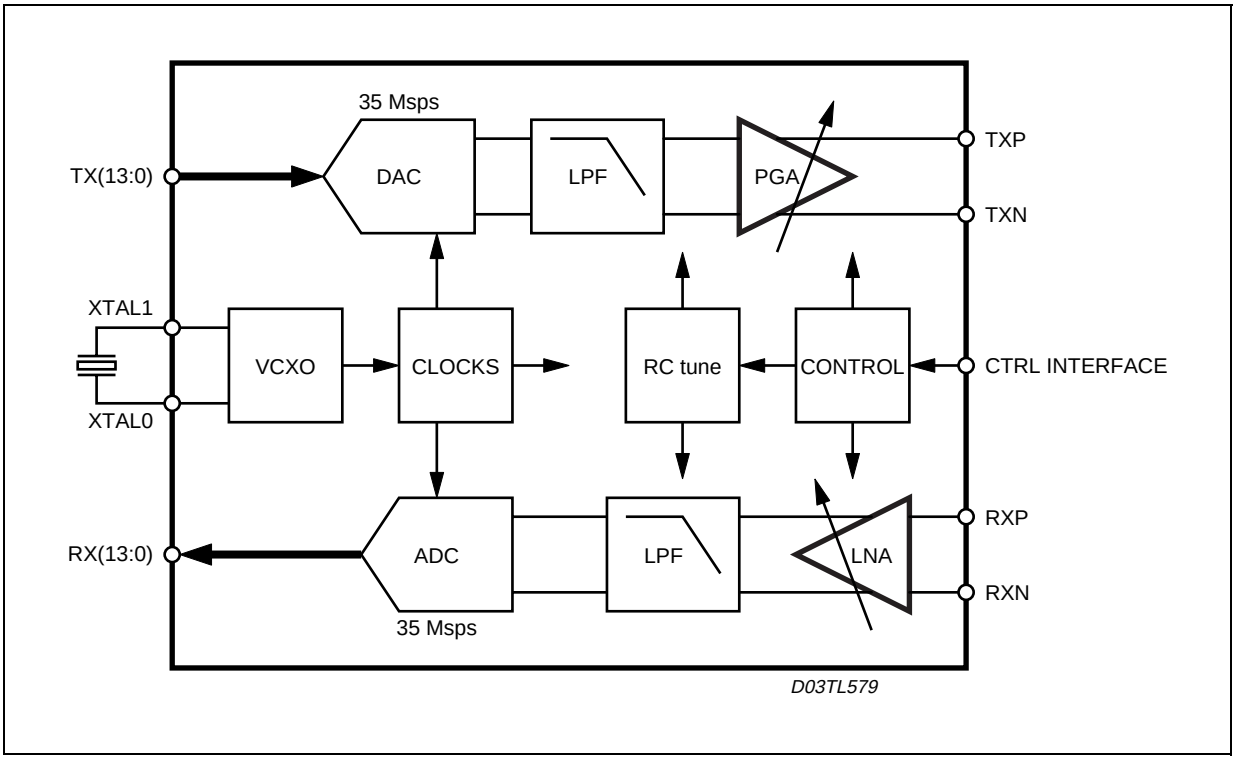
The same chipset is used at both sides of the link. An external VDSL-compatible line driver is used to drive the twisted pair. Finally, a splitter* is needed to split the base band signal from the modulated VDSL signal.

4.2 The Chipset Functions

The chip functions are depicted in the block diagram of the VDSL modem presented in Fig. 1 The functions included in each IC are as follows:

4.2.1 Analog Front-end Circuit (STLC90114)

Figure 2. A block diagram of the analog front end circuit (STLC90114).

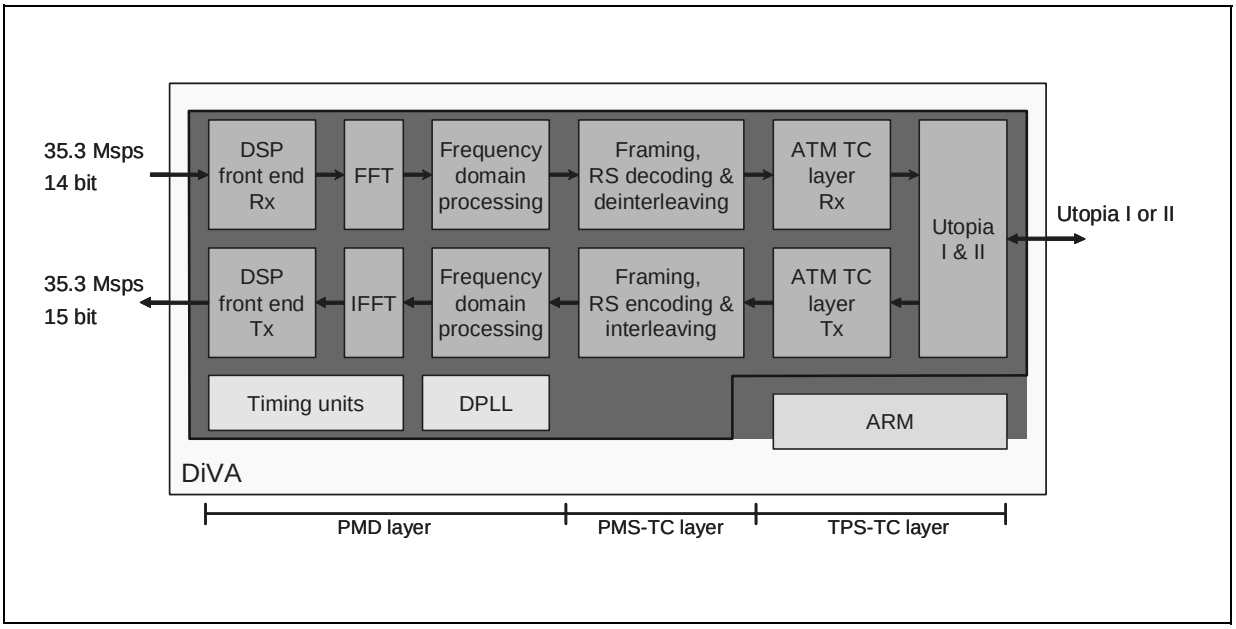


This CMOS IC contains the analog functions required in the transceiver:

- [0..12MHz] receive and transmit signal frequency band
- 35MHz 14bit digital to analog conversion
- 35MHz 14bit analog to digital conversion
- Programmable gain amplifier in the TX path for optimum transmit power setting; the PGA is a pre-amplifier for the external line driver
- RX filtering for noise reduction; TX filtering for slew rate reduction
- RC tuning for filter cut-off frequency control
- Clock generation based on a voltage controlled crystal oscillator; fine tuning by means of external capacitors.
- Serial control interface to configure the component in normal mode and in test mode
- 100-pin TQFP package (14x14mm)
- Power consumption 500mW Typ.
- BiCMOS6 technology (0.35µm)
- Single 3.0V up to 3.6V supply
- Extended temperature range

4.2.2 Modem/Framer/Controller (STLC90115)

Figure 3. A block diagram of the DMT modem, framer and controller (STLC90115) showing the receive and transmit paths.



The STLC90115 can be used in a hardware implementation for both central office (VTU-O) and remote applications (VTU-R). No special mode setting is required, due to the programmability of the different functions. In the STLC90115 the receive (RX) and transmit (TX) paths are separated.

Common parts are OBC or OCC, performance monitor and test functions. Control and configuration of the STLC90115 is by an external processor. All programmable coefficients and parameters are loaded by the OBC or OCC.

The VDSL initialization procedure is also controlled by the OBC or OCC. Such rapid control functions as pilot tone tracking and the DMT symbol time alignment are implemented in the hardware. (e.g. a DPLL with programmable filters and gains.)

Receive path

STLC90115 functions in the receive direction:

- Decimation of the RX signal (35.328 MHz) to a sampling rate of 17.664
- Receive Windowing
- Time domain to Frequency conversion with FFT
- Radio Frequency Interference Canceling
- Rotor and Frequency domain Equalizing
- Demapping of the DMT carriers to a digital bit stream
- Error and noise monitoring on individual carriers and pilot tones
- DPLL function for tracking the received signal frequency deviations
- Adaptive FEQ coefficient update scheme
- Reed Solomon decoding and de-interleaving
- Cell specific functions
- Utopia level 1 & 2 interface (& SLAP interface)

Transmit path

STLC90115 functions in the transmit direction:

- Utopia level 1 & 2 interface (& SLAP interface)
- Cell specific functions
- Reed Solomon encoding + interleaving
- Mapping a digital bit stream on DMT carriers
- Rotor and Frequency domain gain correction;
- Spectral Shaping
- Frequency to Time domain conversion with IFFT,
- Time Domain DMT symbol composing and filtering;
- Transmit Windowing
- Interpolation of the TX signal programmable from a 17.664 MHz towards 35.328 MHz.

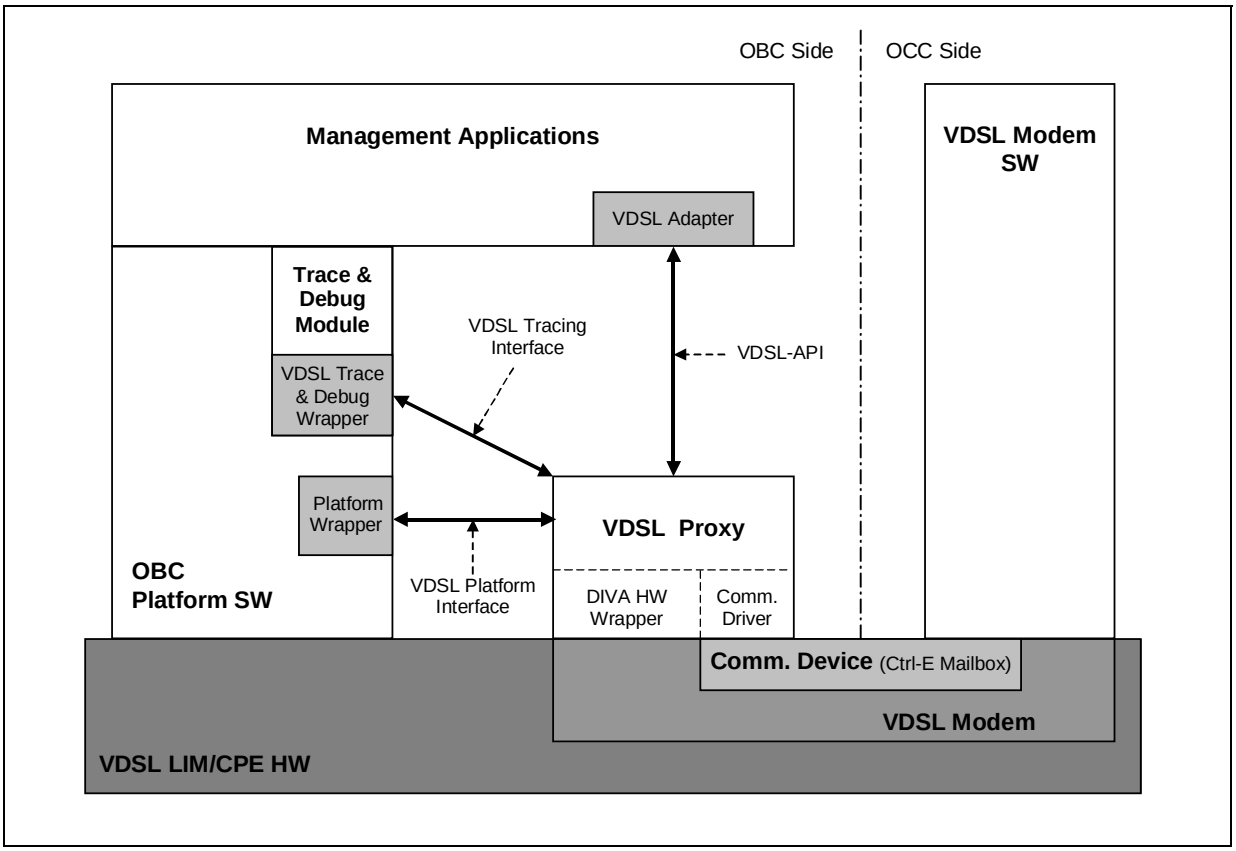
Control of Transceiver Chip Operations:

The STLC90115 runs the firmware controlling the operations of the VDSL transceiver (AFE, DMT modem, Framer). During modem initialization, the controller computes and sets up parameters for all programmable DMT functions, filters and equalizers. The controller is able to run in different rate-adaptive modes as defined by the operator and can run programs for the VTU-O (master mode) or for the VTU-R (slave-mode) sides. The controller also implements the EOC and VOC protocols. During operation, the STLC90115 performs continuous line monitoring and initiates consecutive actions as specified by the operator (e.g. bit swapping, dynamic bit-rate adaptation...). It also collects performance and error information for use by management entities.

Interface to Management Entities

The STLC90115 also runs the communication protocol to interface with external management entities. A specific VDSL modem control interface is available to ease the integration with both systems HW and FW. This "CTRLE communication channel" is used to transfer information and commands between modem and management entities. The STLC90115 provides direct HW connection to external components (processors, SARs, Muxes,...) through an 8-bit parallel bus for the control path. An API for the external management function is provided or the Operation and Maintenance of the VDSL chipset. This API significantly reduces the software design in cycle. The following simplified VDSL LIM/CPE software reference model is used to describe the external SW interfaces of the VDSL Modem.

Figure 4. VDSL LIM/CPE SW Reference Model



The following main software units/modules are identified in Figure 4, as far as the external software interfaces of the VDSL modems are concerned:

- **Management Applications:** These are platform specific manager SW items (e.g. equipment manager, alarm manager, VDSL transport manager, etc.) which are responsible for the configuration, fault and performance management of the VDSL Modem.
- **OBC Platform SW:** This unit provides common platform services (e.g. OS, communications, trace & debug, etc.) to the other SW items running on the OBC.
- **Trace & Debug Module:** This is a module of OBC Platform SW that provides generic trace & debug services.
- **VDSL Modem SW:** This is the monolithic VDSL Modem SW unit running on the OCC. It contains the VDSL Transceiver SW, VDSL specific Manager SW and also their underlying OCC Platform SW (BSP, OS, OS wrapper, etc.).
- **VDSL Proxy:** This is a proxy agent that runs on the OBC and implements the VDSL-API (on behalf of the VDSL Modem SW). It also acts as a HW wrapper for the VDSL Modem.
- **VDSL Adapter:** This modules allows the platform specific Management Applications to be integrated with the VDSL Modem SW over the generic VDSL-API. It must be necessary to use such a module in order to be able to integrate the VDSL Modem SW that is platform independent, with the Management Applications, if those applications are not designed to use the generic VDSL-API directly.
- **VDSL Trace & Debug Wrapper:** This module acts as a wrapper for the VDSL specific trace & debug services such that, those services can be accessed via the generic trace & debug module of the OBC Platform SW.
- **Platform Wrapper:** This module provides the specific platform services required by the VDSL Proxy that is implemented as platform independent.

5 BUILDING SYSTEMS WITH THE ZipperWire VDSL CHIPSET

ST has taken great care in defining ZipperWire to ease its integration into system designs. In particular, this is achieved:

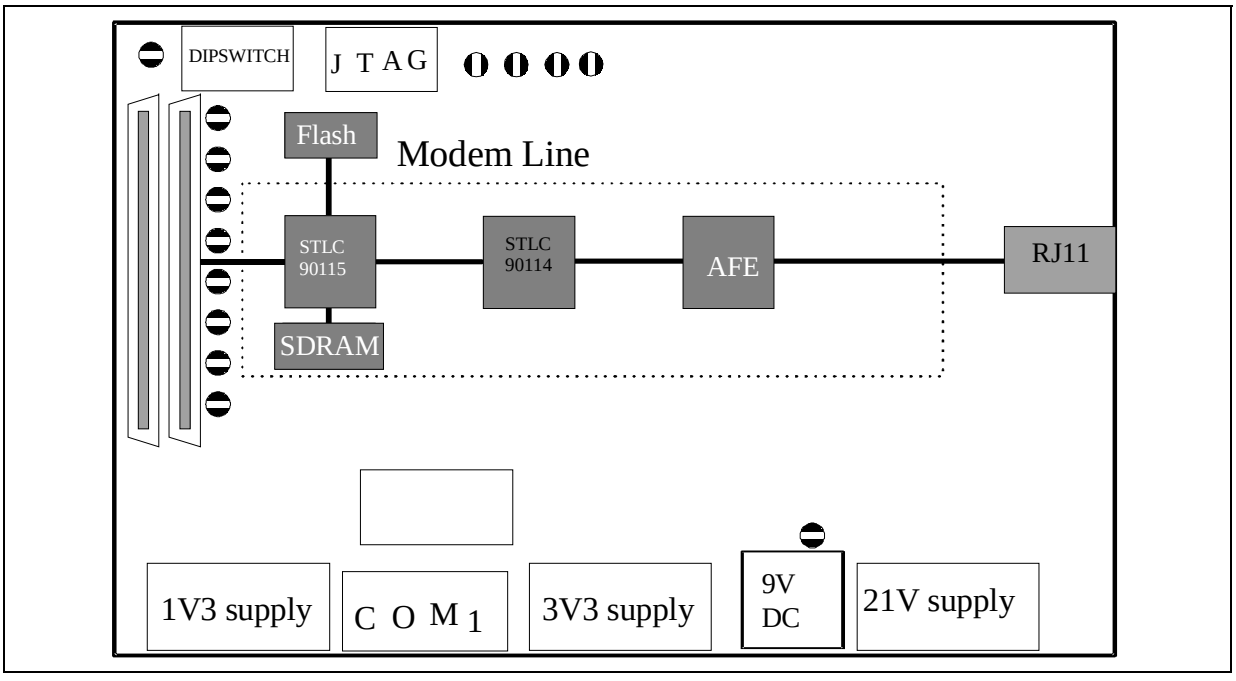
- at the Hardware level: by using standard interfaces both for data transfer (ATM Utopia) and for control (8-bit parallel)
- at the Firmware level: by clearly separating the modem firmware, run on the embedded Transceiver Controller from other systems related and application-specific functions. The boundary between the two domains provides a simple modem control protocol (CTRLE).

This "packaged modem" approach provides a self-contained VDSL modem solution, allowing system manufacturers to concentrate on system issues. External interfaces remain the same so that there is no impact on external system HW and SW elements.

ZipperWire comes in a complete package with firmware, schematics, Bill of Materials, Operations and Maintenance API for the OBC, and layout information for the VDSL modem part. It is further supported by a full development environment consisting of:

- Evaluation boards - can be used both on VTU-O and VTU-R sides
- VDSL test and control firmware running on PC with GUI

Figure 5.



6 ZipperWire EVALUATION BOARD

The Zipperwire evaluation board provides the following interfaces:

- Utopia level 2 Rx/Tx
- RS-232 Command shell
- JTAG 14-pin
- VDSL line RJ-11
- Power supply 9V DC unregulated
- DIP switches for LT/NT and flash selection
- LEDs