PSD4000 FAMILY

Flash Programmable System Devices For 16-bit MCUs

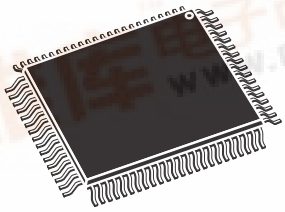
DATA BRIEFING

FEATURES SUMMARY

Members of the PSD4000 Family provide an integrated solution to 16-bit MCU based applications that includes configurable memories, PLD logic and I/O:

- Dual Bank Flash Memories
  - 4 or 8 Mbit of Primary Flash Memory
  - 256 or 512 Kbit Secondary Flash Memory
  - Concurrent operation: read from one memory while erasing and writing the other
- 64 or 256 Kbit SRAM (Battery Backed)
- PLD with Macrocells
  - Over 3000 Gates of PLD: CPLD and DPLD
  - CPLD with 16 Output Macrocells (OMCs) and 24 Input Macrocells (IMCs)
  - DPLD – user defined internal chip select decoding
- Seven I/O Ports with 52 I/O pins
  - 52 individually configurable I/O port pins that can be used for the following functions:
  - MCU I/Os
  - PLD I/Os
  - Latched MCU address output
  - Special function I/Os
  - I/O ports may be configured as open-drain outputs
- In-System Programming (ISP) with JTAG
  - Built-in JTAG compliant serial port allows full-chip In-System Programmability
  - Efficient manufacturing allow easy product testing and programming
  - Use low cost FlashLINK cable with PC
- Page Register
  - Internal page register that can be used to expand the microcontroller address space by a factor of 256

Figure 1. Packages



TQFP80 (U)

- Programmable power management
- High Endurance:
  - 100,000 Erase/Write Cycles of Flash Memory
  - 1,000 EraseWrite Cycles of PLD
  - 15 Year Data Retention
- Single Supply Voltage
  - 5V (±10%)
  - 3.3V (±10%)

SUMMARY DESCRIPTION

The PSD family of memory systems for microcontrollers (MCUs) brings In-System-Programmability (ISP) to Flash memory and programmable logic. The result is a simple and flexible solution for embedded designs. PSD devices combine many of the peripheral functions found in MCU based applications.

PSD devices integrate an optimized Macrocell logic architecture. The Macrocell was created to address the unique requirements of embedded system designs. It allows direct connection between the system address/data bus, and the internal PSD registers, to simplify communication between the MCU and other supporting devices.

The PSD family offers two methods to program the PSD Flash memory while the PSD is soldered to the circuit board: In-System Programming (ISP) via JTAG, and In-Application Programming (IAP).

In-System Programming (ISP) via JTAG

An IEEE 1149.1 compliant JTAG In-System Programming (ISP) interface is included on the PSD enabling the entire device (Flash memories, PLD, configuration) to be rapidly programmed while soldered to the circuit board. This requires no MCU participation, which means the PSD can be programmed anytime, even when completely blank.

The innovative JTAG interface to Flash memories is an industry first, solving key problems faced by designers and manufacturing houses, such as:

- First time programming.

  Program blank Flash PSDs directly on the circuit board.

- Inventory build-up of pre-programmed devices.

  Build your hardware with blank PSDs soldered directly to the board and then custom program just before they are shipped to the customer. No more labels on chips, and no more wasted inventory.

- Expensive sockets.

  Solder the PSD directly to the circuit board. Program first time and subsequent times with JTAG. No need to handle devices and bend the fragile leads.

In-Application Programming (IAP)

Two independent Flash memory arrays are included so that the MCU can execute code from one while erasing and programming the other. Robust product firmware updates in the filed are possible over any communication channel (CAN, Ethernet, UART, J1850, etc) using this unique architecture. Designers are relieved of these problems:

- Simultaneous read and write to Flash memory.

  The PSD allows the MCU to operate the two Flash memory blocks concurrently, reading code from one while erasing and programming the other during IAP.

- Complex memory mapping.

  A programmable Decode PLD (DPLD) is embedded in the PSD. The concurrent PSD memories can be mapped anywhere in MCU address space, segment by segment with extermely high address resolution. As an option, the secondary Flash memory can be swapped out of the system memory map when IAP is complete. A built-in page register breaks the MCU address limit.

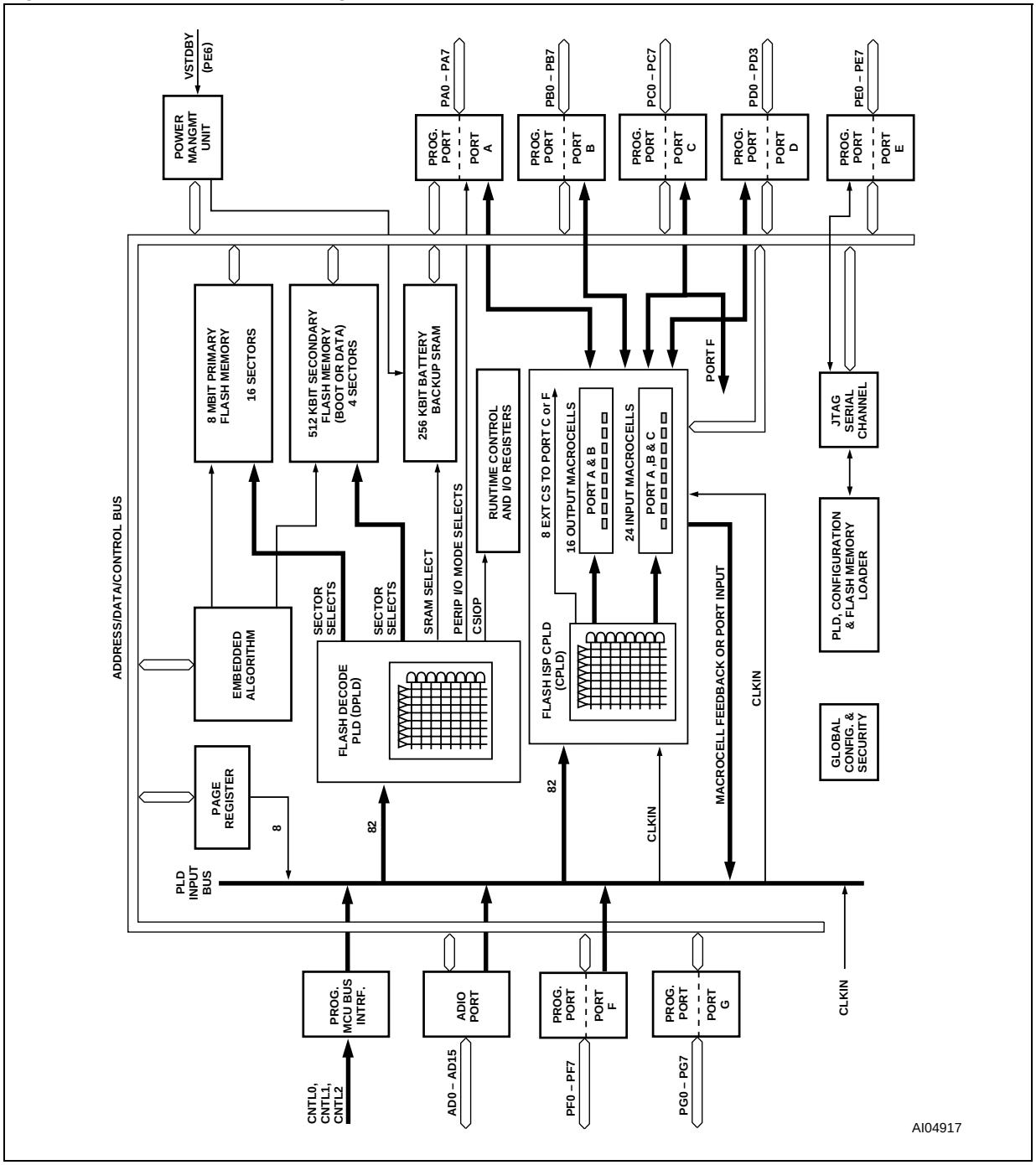
- Separate Program and Data space.

  The PSD provides means to reclassify Flash memory as Data space during IAP, then back to Program space when complete. This solves an inherint problem with concurrent programming in 8051 based designs.

PSDsoft Express

PSDsoft Express, a software development tool from ST, guides you through the design process step-by-step making it possible to complete an embedded MCU design capable of ISP/IAP in just hours. Select your MCU and PSDsoft Express takes you through the remainder of the design with point and click entry, covering PSD selection, pin definitions, programmable logic inputs and outpus, MCU memory map definition, ANSI-C code generation for your MCU, and merging your MCU firmware with the PSD design. When complete, two different device programmers are supported directly from PSDsoft Express: FlashLINK (JTAG) and PSDpro.

Figure 2. PSD4256G6 Block Diagram



Note: Additional address lines can be brought in to the device via Port A, B, C, D or F.

Figure 2 shows the block diagram for the PSD42xx family (specifically, the PSD4256G6). The PSD41xx family has a similar block diagram, but with a simpler General Purpose PLD in place of the Complex PLD (CPLD).

PSD ARCHITECTURAL OVERVIEW

PSD devices contain several major functional blocks. Figure 2 shows the architecture of the PSD device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions and are user configurable.

Memory

Each of the memory blocks is briefly discussed in the following paragraphs. A more detailed discussion can be found in the data sheet.

- The 4 or 8 Mbit primary Flash memory is the main memory of the PSD. It is divided into 16 equally-sized sectors that are individually selectable.
- The 256 or 512 Kbit secondary Flash memory is divided into 4 equally-sized sectors that are individually selectable.
- The 64 or 256 Kbit SRAM is intended for use as a scratch-pad memory or as an extension to the MCU SRAM. If an external battery is connected to the PSD's Voltage Stand-by (VSTBY, PE6) signal, data is retained in the event of power failure.

Each memory block can be located in a different address space as defined by the user. The access times for all memory types includes the address latching and DPLD decoding time.

PLDs

The device contains two PLD blocks, the Decode PLD (DPLD) and the Complex PLD (CPLD), as shown in Table 1, each optimized for a different function. The functional partitioning of the PLDs reduces power consumption, optimizes cost/performance, and eases design entry.

The DPLD is used to decode addresses and to generate Sector Select signals for the PSD internal memory and registers. The DPLD has combinatorial outputs, while the CPLD can implement more general user-defined logic functions. The CPLD has 16 Output Macrocells (OMC) and 8 combinatorial outputs. The PSD also has 24 Input Macrocells (IMC) that can be configured as inputs to the PLDs. The PLDs receive their inputs from the PLD Input Bus and are differentiated by their output destinations, number of product terms, and Macrocells.

The PLDs consume minimal power. The speed and power consumption of the PLD is controlled by the Turbo bit in PMMR0 and other bits in PMMR2. These registers are set by the MCU at run-time. There is a slight penalty to PLD propagation time when not in the Turbo mode.

I/O Ports

The PSD has 52 I/O pins divided among seven ports (Port A, B, C, D, E, F and G). Each I/O pin can be individually configured for different functions. Ports can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for MCUs using multiplexed address/data buses

The JTAG pins can be enabled on Port E for In-System Programming (ISP).

Table 1. PLD I/O

Name	Inputs	Outputs	Product Terms
Decode PLD (DPLD)	82	17	43
Complex PLD (CPLD)	82	24	150

MCU Bus Interface

The PSD easily interfaces easily with most 16-bit MCUs, either with multiplexed or non-multiplexed address/data buses. The device is configured to respond to the MCU's control pins, which are also used as inputs to the PLDs.

ISP via JTAG Port

In-System Programming (ISP) can be performed through the JTAG signals on Port E. This serial interface allows complete programming of the entire PSD device. A blank device can be completely programmed. The JTAG signals (TMS, TCK, TSTAT, $\overline{\text{TERR}}$, TDI, TDO) can be multiplexed with other functions on Port E.

In-System Programming (ISP)

Using the JTAG signals on Port E, the entire PSD device (memory, logic, configuration) can be programmed or erased without the use of the MCU.

In-Application Programming (IAP)

The primary Flash memory can also be programmed, or re-programmed, in-system by the MCU executing the programming algorithms out of the secondary Flash memory, or SRAM. The secondary Flash memory can be programmed the same way by executing out of the primary Flash memory. Table 2 indicates which programming methods can program different functional blocks of the PSD.

Page Register

The 8-bit Page Register expands the address range of the MCU by up to 256 times. The paged address can be used as part of the address space to access external memory and peripherals, or internal memory and I/O. The Page Register can also be used to change the address mapping of the Flash memory blocks into different memory spaces for IAP.

Power Management Unit (PMU)

The Power Management Unit (PMU) gives the user control of the power consumption on selected functional blocks based on system requirements. The PMU includes an Automatic Power-down (APD) Unit that turns off device functions during MCU inactivity. The APD Unit has a Power-down mode that helps reduce power consumption.

The PSD also has some bits that are configured at run-time by the MCU to reduce power consumption of the CPLD. The Turbo bit in PMMR0 can be reset to 0 and the CPLD latches its outputs and goes to Stand-by mode until the next transition on its inputs.

Additionally, bits in PMMR2 can be set by the MCU to block signals from entering the CPLD to reduce power consumption. See the section entitled “PSD Register Description and Address Offsets” on page 9 for more details.

Table 2. Methods of Programming Different Functional Blocks of the PSD

Functional Block	JTAG-ISP	Device Programmer	IAP
Primary Flash Memory	Yes	Yes	Yes
Secondary Flash memory	Yes	Yes	Yes
PLD Array (DPLD and CPLD)	Yes	Yes	No
PSD Configuration	Yes	Yes	No

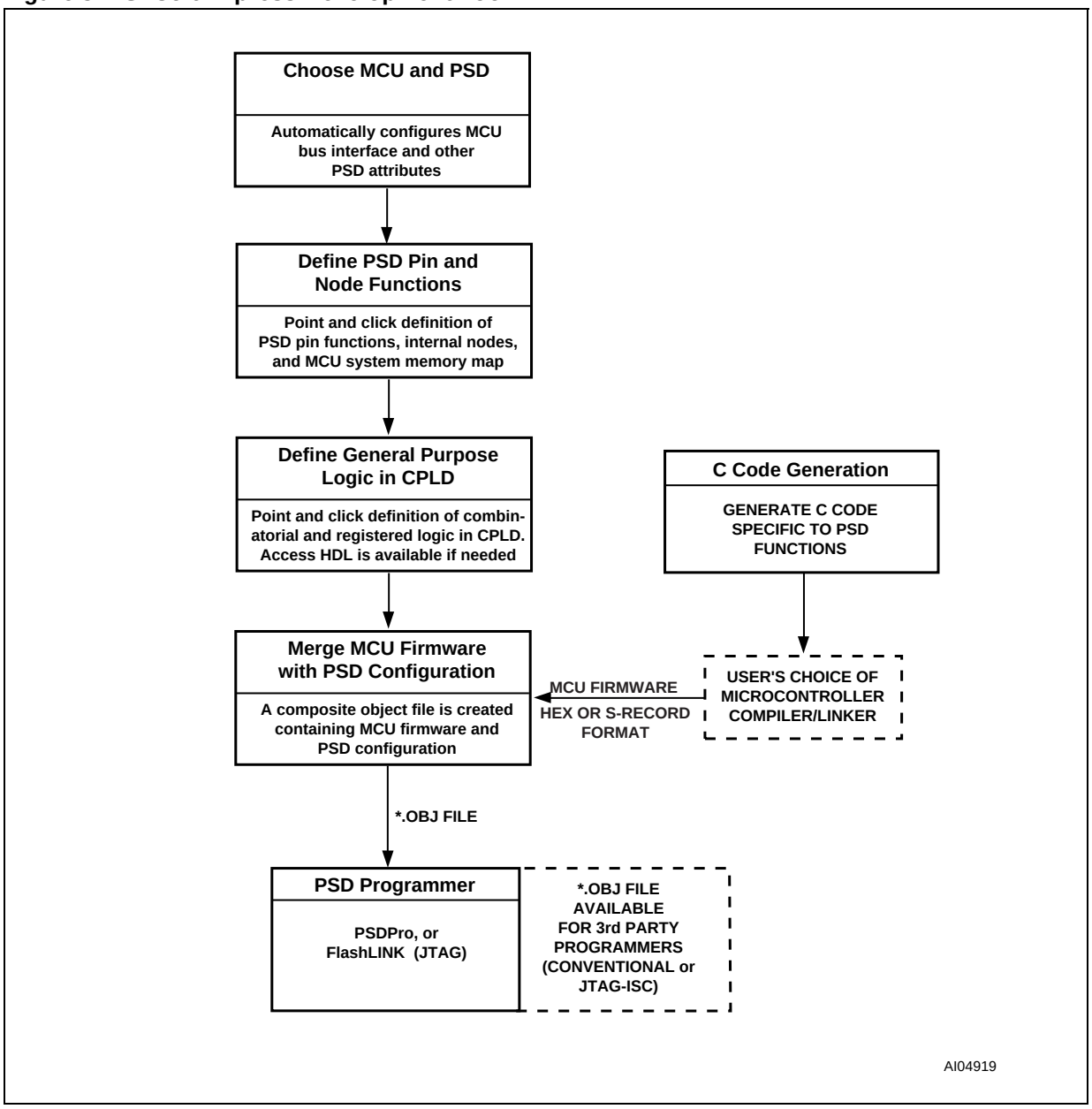
DEVELOPMENT SYSTEM

The PSD4000 Family is supported by PSDsoft Express, a Windows-based software development tool (Windows-95, Windows-98, Windows-2000, Windows-NT). A PSD design is quickly and easily produced in a point and click environment. The designer does not need to enter Hardware Description Language (HDL) equations, unless desired, to define PSD pin functions and memory map information. The general design flow is shown in Figure 3. PSDsoft Express is available from our web site:

www.st.com/psd

PSDsoft Express directly supports two low cost device programmers form ST: PSDpro and FlashLINK (JTAG). Both of these programmers may be purchased through your local distributor/ representative, or directly from our web site using a credit card. The PSD is also supported by thid party device programmers. See our web site for the current list.

Figure 3. PSDsoft Express Development Tool



PIN DESCRIPTION

Table 3 describes the signal names and signal functions of the PSD. Those that have multiple names or functions are defined using PSDsoft Express.

Table 3. Pin Description (for the TQFP package)

Pin Name	Type	Description
ADIO0-ADIO15	I/O	This is the lower Address/Data port. Connect your MCU address or address/data bus according to the following rules: 1. If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect AD0-AD7 to this port. 2. If your MCU does not have a multiplexed address/data bus, connect A0-A7 to this port. 3. If you are using an 80C51XA in burst mode, connect A4/D0 through A11/D7 to this port. ALE or AS latches the address. The PSD drives data out only if the read signal is active and one of the PSD functional blocks has been selected. The addresses on this port are passed to the PLDs.
CNTL0-CNTL2	I	Configurable MCU control signals.
$\overline{\text{Reset}}$	I	Active Low input. Resets I/O Ports, PLD Macrocells and some of the Configuration Registers and JTAG registers. Must be Low at Power-up. Reset also aborts any Flash memory Program or Erase cycle that is currently in progress.
PA0-PA7	I/O CMOS or Open Drain	These pins make up Port A. These port pins are configurable and can have the following functions: 1. MCU I/O – standard output or input port. 2. CPLD Macrocell (McellA0-McellA7) outputs. 3. Latched, transparent or registered PLD inputs (can also be PLD input for address A16 and above).
PB0-PB7	I/O CMOS or Open Drain	These pins make up Port B. These port pins are configurable and can have the following functions: 1. MCU I/O – standard output or input port. 2. CPLD Macrocell (McellB0-McellB7) outputs. 3. Latched, transparent or registered PLD inputs (can also be PLD input for address A16 and above).
PC0-PC7	I/O CMOS or Slew Rate	These pins make up Port C. These port pins are configurable and can have the following functions: 1. MCU I/O – standard output or input port. 2. External Chip Select (ECS0-ECS7) outputs. 3. Latched, transparent or registered PLD inputs (can also be PLD input for address A16 and above).
PD0-PD3	I/O CMOS or Open Drain	These pins make up Port D. This port pin can be configured to have the following functions: 1. $\overline{\text{ALE}}$/AS input – latches address on ADIO0-ADIO15. 2. $\overline{\text{AS}}$ input – latches address on ADIO0-ADIO15 on the rising edge. 3. MCU I/O – standard output or input port. 4. Transparent PLD input (can also be PLD input for address A16 and above). 5. CLKIN – clock input to the CPLD Macrocells, the APD Unit's Power-down counter, and the CPLD AND Array. 6. PSD Chip Select Input ($\overline{\text{CSI}}$). When Low, the MCU can access the PSD memory and I/O. When High, the PSD memory blocks are disabled to conserve power. The falling edge of this signal can be used to get the device out of Power-down mode. 7. $\overline{\text{WRH}}$ – for 16-bit data bus, write to high byte, active low.
PE0-PE7	I/O CMOS or Open Drain	These pins make up Port E. This port pin can be configured to have the following functions: 1. MCU I/O – standard output or input port. 2. Latched address output. 3. JTAG Serial Interface signals. 3. SRAM battery backup connections.

Pin Name	Type	Description
PF0-PF7	I/O CMOS or Open Drain	These pins make up Port F. These port pins are configurable and can have the following functions: 1. MCU I/O – standard output or input port. 2. External Chip Select (ECS0-ECS7) outputs, or inputs to CPLD. 3. Latched address outputs. 4. Address A1-A3 inputs in 80C51XA mode (PF0 is grounded) 5. Data bus port (D0-D7) in a non-multiplexed bus configuration. 6. Peripheral I/O mode. 7. MCU reset mode.
PG0-PG7	I/O CMOS or Open Drain	These pins make up Port G. These port pins are configurable and can have the following functions: 1. MCU I/O – standard output or input port. 2. Latched address outputs. 3. Data bus port (D8-D15) in a non-multiplexed bus configuration. 4. MCU reset mode.
V_{CC}		Supply Voltage
GND		Ground pins

PSD REGISTER DESCRIPTION AND ADDRESS OFFSETS

Table 4 shows the offset addresses to the PSD registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal PSD registers. Table 4 provides brief descriptions of the registers in CSIOP space. The following sections give a more detailed description.

Table 4. PSD4256G6 Register Address Offset

Register Name	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Other[1]	Description
Data In	00	01	10	11	30	40	41		Reads Port pin as input, MCU I/O input mode
Control					32	42	43		Selects mode between MCU I/O or Address Out
Data Out	04	05	14	15	34	44	45		Stores data for output to Port pins, MCU I/O output mode
Direction	06	07	16	17	36	46	47		Configures Port pin as input or output
Drive Select	08	09	18	19	38	48	49		Configures Port pins as either CMOS or Open Drain on some pins, while selecting high slew rate on other pins.
Input Macrocell	0A	0B		1A					Reads Input Macrocells
Enable Out	0C	0D	1C			4C			Reads the status of the output enable to the I/O Port driver
Output Macrocells A	20								Read – reads output of Macrocells A Write – loads Macrocell Flip-flops
Output Macrocells B		21							Read – reads output of Macrocells B Write – loads Macrocell Flip-flops
Mask Macrocells A	22								Blocks writing to the Output Macrocells A
Mask Macrocells B		23							Blocks writing to the Output Macrocells B
Flash Memory Protection 1								C0	Read only – Primary Flash Sector Protection
Flash Memory Protection 2								C1	Read only – Primary Flash Sector Protection
Flash Boot Protection								C2	Read only – PSD Security and Secondary Flash memory Sector Protection
JTAG Enable								C7	Enables JTAG Port
PMMR0								B0	Power Management Register 0
PMMR2								B4	Power Management Register 2
Page								E0	Page Register
VM								E2	Places PSD memory areas in Program and/or Data space on an individual basis.
Memory_ID0								F0	Read only – SRAM and Primary memory size
Memory_ID1								F1	Read only – Secondary memory type and size

Note: 1. Other registers that are not part of the I/O ports.

Figure 4. An Example of a Typical 16-bit Multiplexed Bus Interface

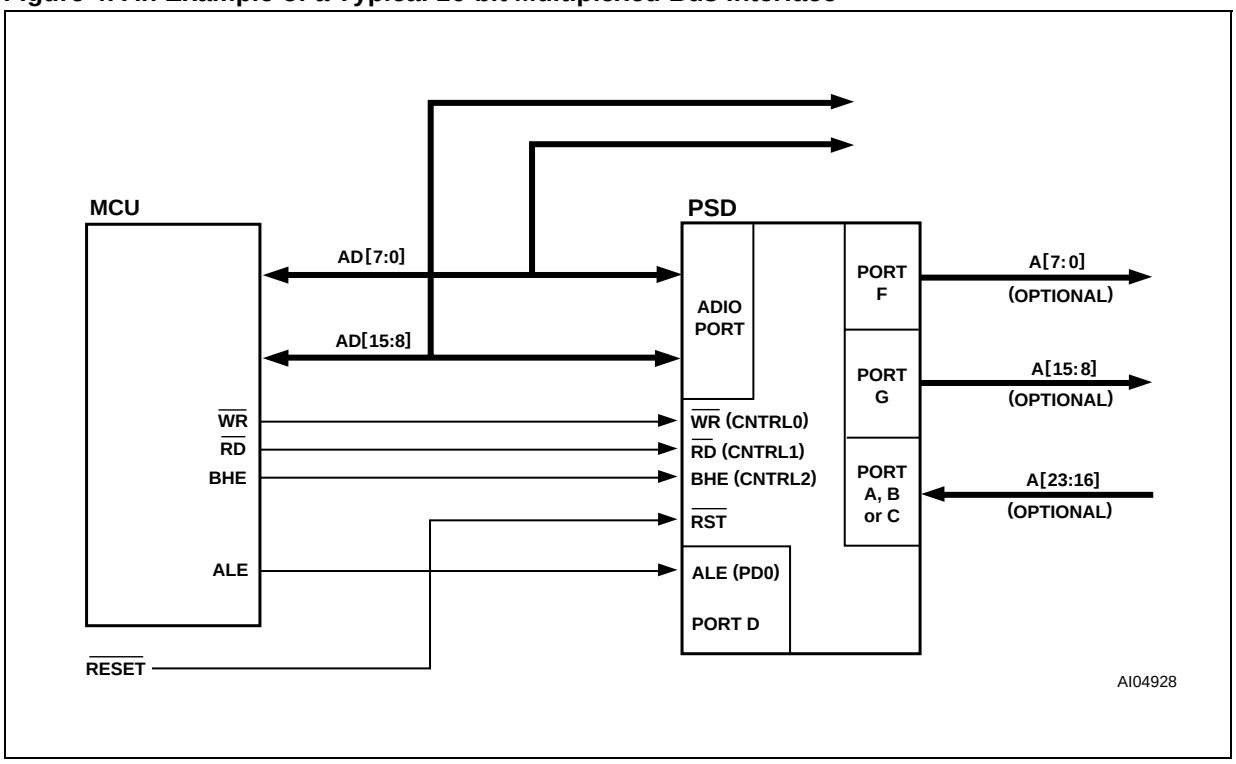
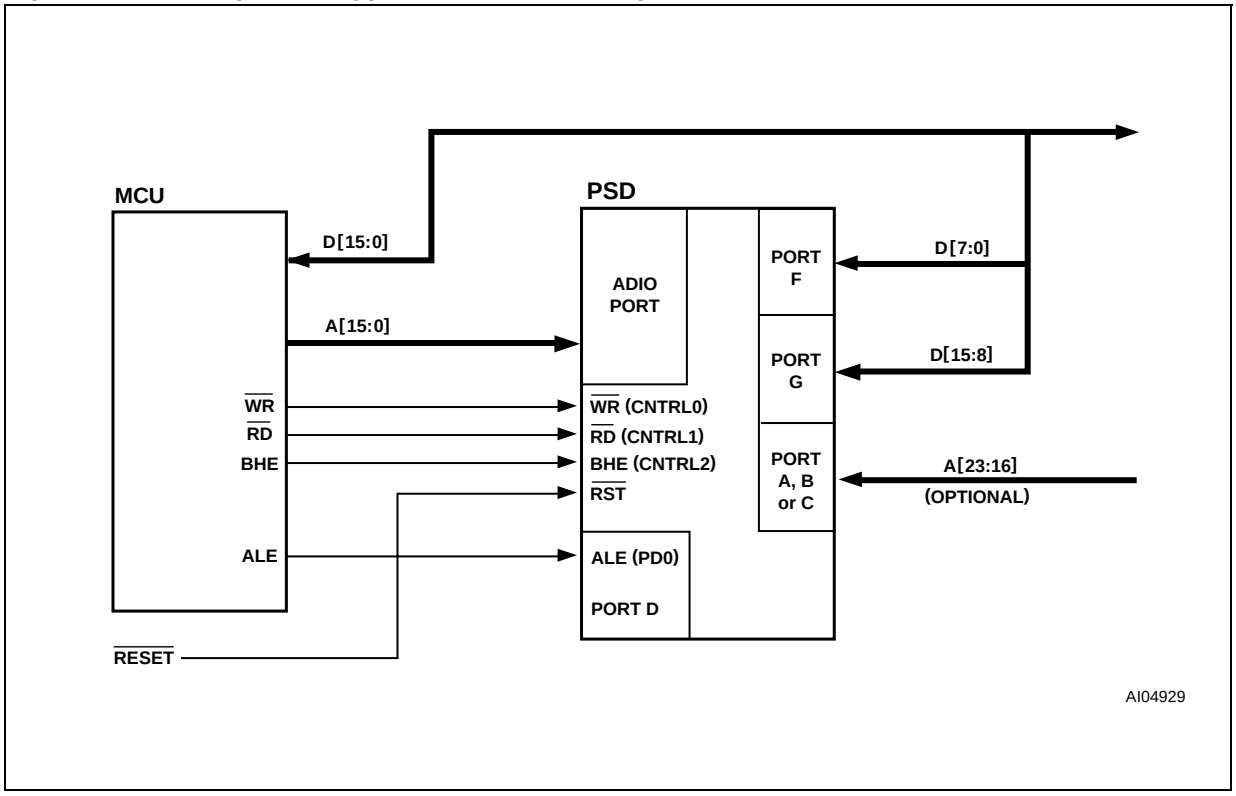


Figure 5. An Example of a Typical 16-bit Non-Multiplexed Bus Interface



POWER MANAGEMENT

The PSD device offers configurable power saving options. These options may be used individually or in combinations, as follows:

- All memory blocks in a PSD (primary Flash memory, secondary Flash memory, and SRAM) are built with power management technology. In addition to using special silicon design methodology, power management technology puts the memories into standby mode when address/data inputs are not changing (zero DC current). As soon as a transition occurs on an input, the affected memory "wakes up", changes and latches its outputs, then goes back to standby. The designer does *not* have to do anything special to achieve memory Stand-by mode when no inputs are changing—it happens automatically.

  The PLD sections can also achieve Stand-by mode when its inputs are not changing, as described for the Power Management Mode Registers (PMMR), later.
- The Automatic Power Down (APD) block allows the PSD to reduce to stand-by current automatically. The APD Unit also blocks MCU address/data signals from reaching the memories and PLDs. This feature is available on all PSD devices. The APD Unit is described in more detail in the full data sheet.

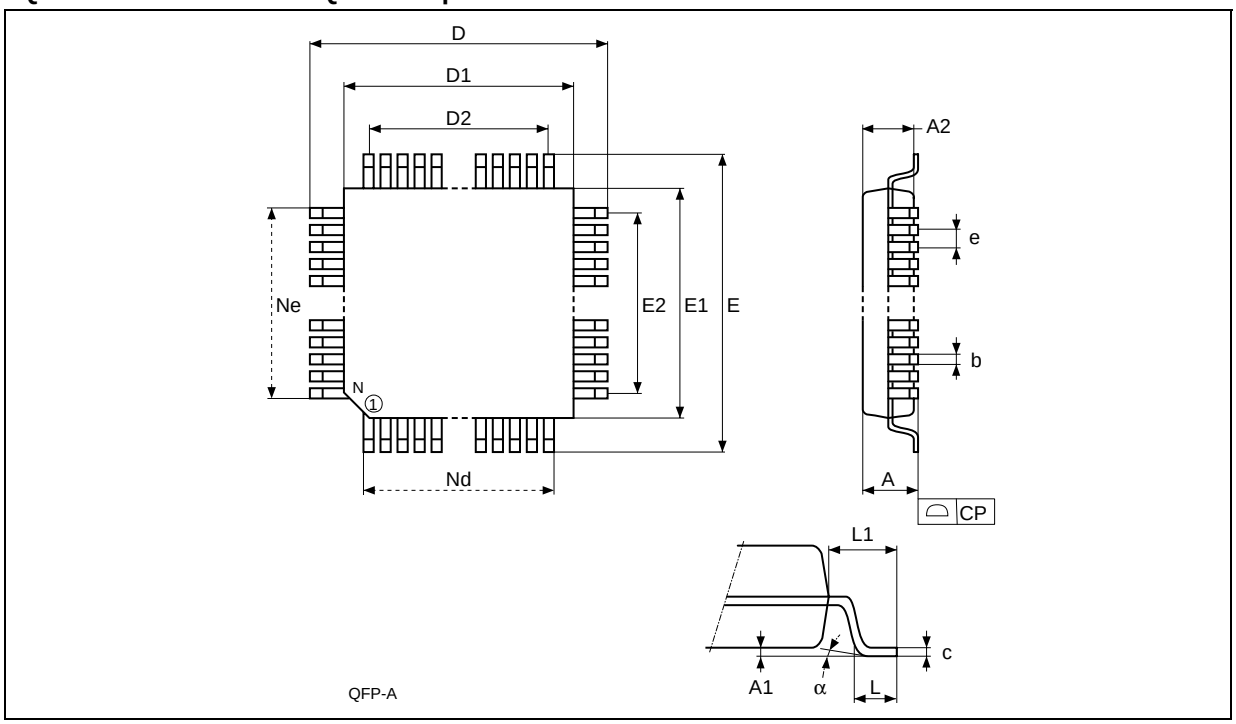
  Built in logic monitors the Address Strobe of the MCU for activity. If there is no activity for a certain period (the MCU is asleep), the APD Unit initiates Power-down mode (if enabled). Once in Power-down mode, all address/data signals are blocked from reaching the PSD memories and PLDs, and the memories are deselected internally. This allows the memories and PLDs to remain in Stand-by mode even if the address/data signals are changing state externally (noise, other devices on the MCU bus, etc.). Keep in mind that any unblocked PLD input signals that are changing states keeps the PLD out of Stand-by mode, but not the memories.
- PSD Chip Select Input ($\overline{CSI}$, PD2) can be used to disable the internal memories, placing them in Stand-by mode even if inputs are changing. This feature does not block any internal signals or disable the PLDs. This is a good alternative to using the APD Unit, especially if your MCU has a chip select output. There is a slight penalty in memory access time when PSD Chip Select Input ($\overline{CSI}$, PD2) makes its initial transition from deselected to selected.
- The Power Management Mode Registers (PMMR) can be written by the MCU at run-time to manage power. All PSD devices support "blocking bits" in these registers that are set to block designated signals from reaching both PLDs. Current consumption of the PLDs is directly related to the composite frequency of the changes on their inputs.

  Significant power savings can be achieved by blocking signals that are not used in DPLD or CPLD logic equations at run-time. PSDsoft Express creates a fuse map that automatically blocks the low address byte (A7-A0) or the control signals (CNTL0-CNTL2, ALE and Write Enable High-byte ($\overline{WRH}$/DBE, PD3)) if none of these signals are used in PLD logic equations.

  PSD devices have a Turbo bit in PMMR0. This bit can be set to turn the Turbo mode off (the default is with Turbo mode turned on). While Turbo mode is off, the PLDs can achieve Stand-by current when no PLD inputs are changing (zero DC current). Even when inputs do change, significant power can be saved at lower frequencies (AC current), compared to when Turbo mode is on. When the Turbo mode is on, there is a significant DC current component, and the AC component is higher.

PACKAGE MECHANICAL

TQFP80 - 80 lead Plastic Quad Flatpack



Note: Drawing is not to scale.

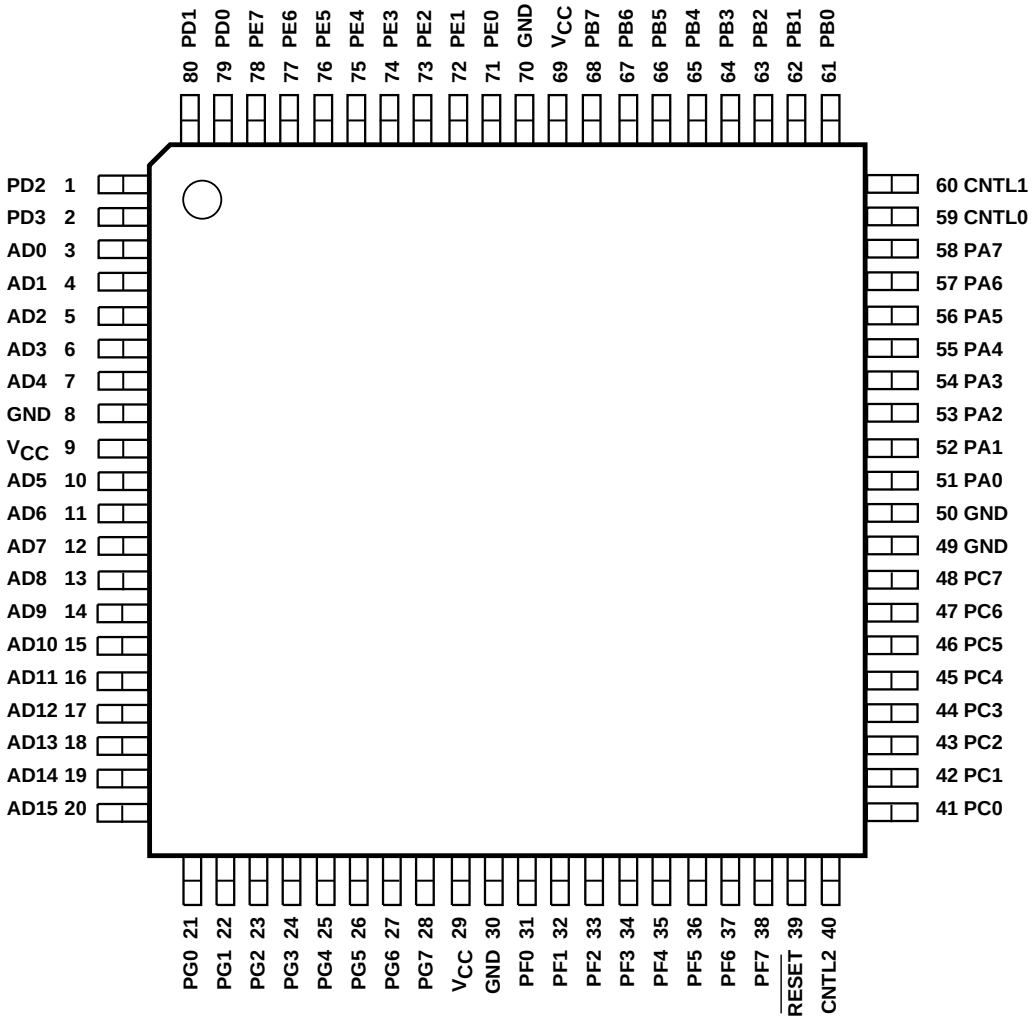
TQFP80 - 80 lead Plastic Quad Flatpack

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
α	3.5°	0.0°	7.0°	3.5°	0.0°	7.0°
b	0.220	0.170	0.270	0.0087	0.0067	0.0106
c		0.090	0.200		0.0035	0.0079
D	14.000			0.5512		
D1	12.000			0.4724		
D2	9.500	—	—	0.3740	—	—
E	14.000			0.5512		
E1	12.000			0.4724		
E2	9.500	—	—	0.3740	—	—
e	0.500	—	—	0.0197	—	—
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
CP	0.080			0.0031		
N	80			80		
Nd	20			20		
Ne	20			20		

Table 5. Pin Assignments – TQFP80

Pin No.	Pin Assignments	Pin No.	Pin Assignments	Pin No.	Pin Assignments	Pin No.	Pin Assignments
1	PD2	21	PG0	41	PC0	61	PB0
2	PD3	22	PG1	42	PC1	62	PB1
3	AD0	23	PG2	43	PC2	63	PB2
4	AD1	24	PG3	44	PC3	64	PB3
5	AD2	25	PG4	45	PC4	65	PB4
6	AD3	26	PG5	46	PC5	66	PB5
7	AD4	27	PG6	47	PC6	67	PB6
8	GND	28	PG7	48	PC7	68	PB7
9	V_{CC}	29	V_{CC}	49	GND	69	V_{CC}
10	AD5	30	GND	50	GND	70	GND
11	AD6	31	PF0	51	PA0	71	PE0
12	AD7	32	PF1	52	PA1	72	PE1
13	AD8	33	PF2	53	PA2	73	PE2
14	AD9	34	PF3	54	PA3	74	PE3
15	AD10	35	PF4	55	PA4	75	PE4
16	AD11	36	PF5	56	PA5	76	PE5
17	AD12	37	PF6	57	PA6	77	PE6
18	AD13	38	PF7	58	PA7	78	PE7
19	AD14	39	$\overline{\text{RESET}}$	59	CNTL0	79	PD0
20	AD15	40	CNTL2	60	CNTL1	80	PD1

Figure 6. TQFP Connections



PART NUMBERING

Table 6. Ordering Information Scheme

Example: PSD42 5 6 G 6 V – 90 U I T

Device Type

PSD42 = Flash PSD for 16-bit MCUs (with Complex PLD)
PSD41 = Flash PSD for 16-bit MCUs (with Simple PLD)

SRAM Size

0 = none	3 = 64 Kbit
1 = 16 Kbit	4 = 128 Kbit
2 = 32 Kbit	5 = 256 Kbit

Flash Memory Size

1 = 256 Kbit	4 = 2 Mbit
2 = 512 Kbit	5 = 4 Mbit
3 = 1 Mbit	6 = 8 Mbit

I/O Count

F = 27 I/O
G = 52 I/O

2nd Non Volatile Memory

1 = 256 Kbit EEPROM	2 = 256 Kbit Flash memory
3 = none	6 = 512 Kbit Flash memory

Operating Voltage

blank = V_{CC} = 4.5 to 5.5V
V = V_{CC} = 3.0 to 3.6V

Speed

70 = 70 ns	12 = 120 ns
90 = 90 ns	15 = 150 ns
	20 = 200 ns

Package

U = TQFP

Temperature Range

blank = 0 to 70 °C (commercial)
I = –40 to 85 °C (industrial)

Option

T = Tape & Reel Packing

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.