



# 74VHCT16374A

## 16-BIT D-TYPE FLIP FLOP WITH 3-STATE OUTPUTS NON INVERTING

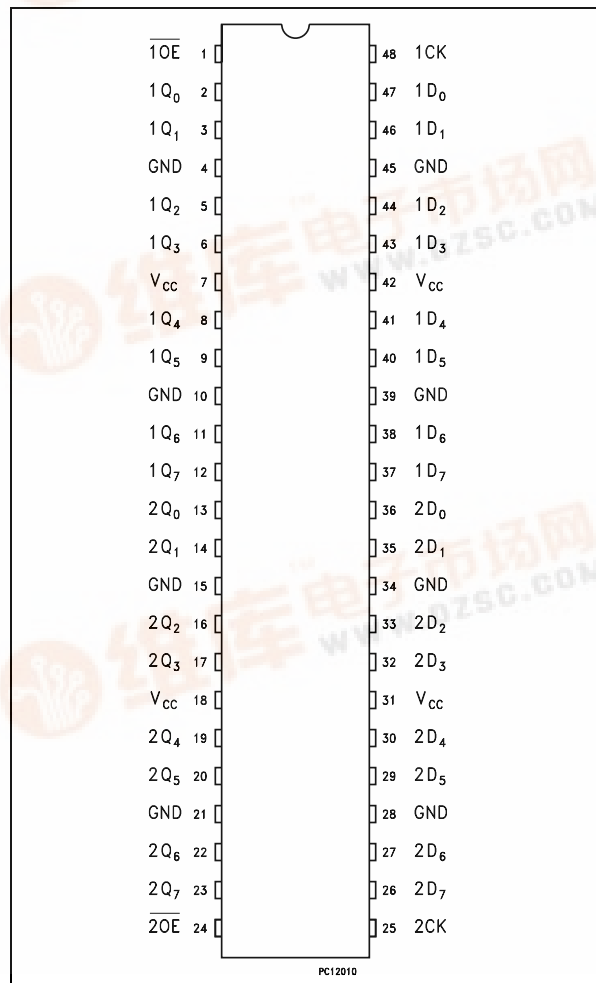
- HIGH SPEED:  
 $f_{MAX} = 185 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:  
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS:  
 $V_{IH} = 2\text{V (MIN.) } V_{IL} = 0.8 \text{ (MAX.)}$
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:  
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:  
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:  
 $V_{CC(OPR)} = 4.5\text{V to } 5.5\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16374
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE:  $V_{OLP} = 0.9\text{V (MAX.)}$



### ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74VHCT16374ATTR

### PIN CONNECTION



### DESCRIPTION

The 74VHCT16374A is an advanced high-speed CMOS 16 D-TYPE FLIP FLOP with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C<sup>2</sup>MOS technology.

These 16 bit D-TYPE flip-flop is controlled by two clock inputs (CK) and two output enable inputs ( $\overline{nOE}$ ). The device can be used as two 8-bit flip-flops or one 16-bit flip-flop.

On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs.

While the ( $\overline{OE}$ ) input is low, the outputs will be in a normal logic state (high or low logic level); while  $\overline{OE}$  is high, the outputs will be in a high impedance state.

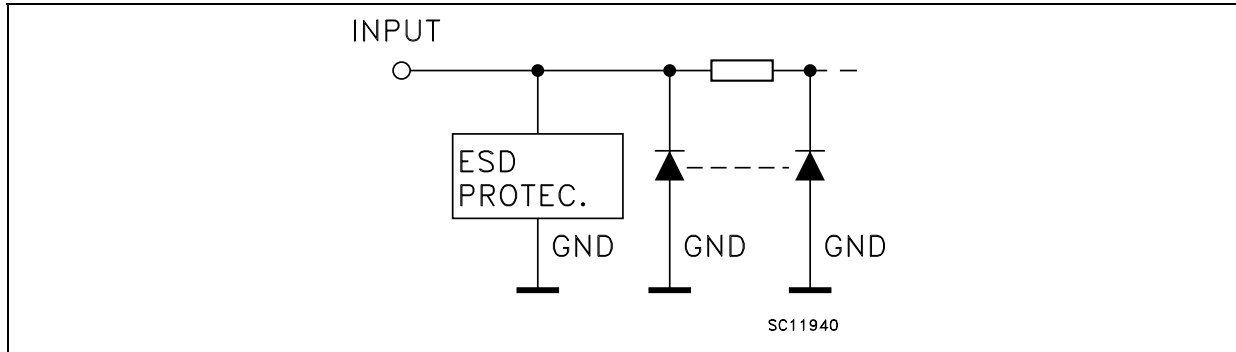
The output control does not affect the internal operation of flip-flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.



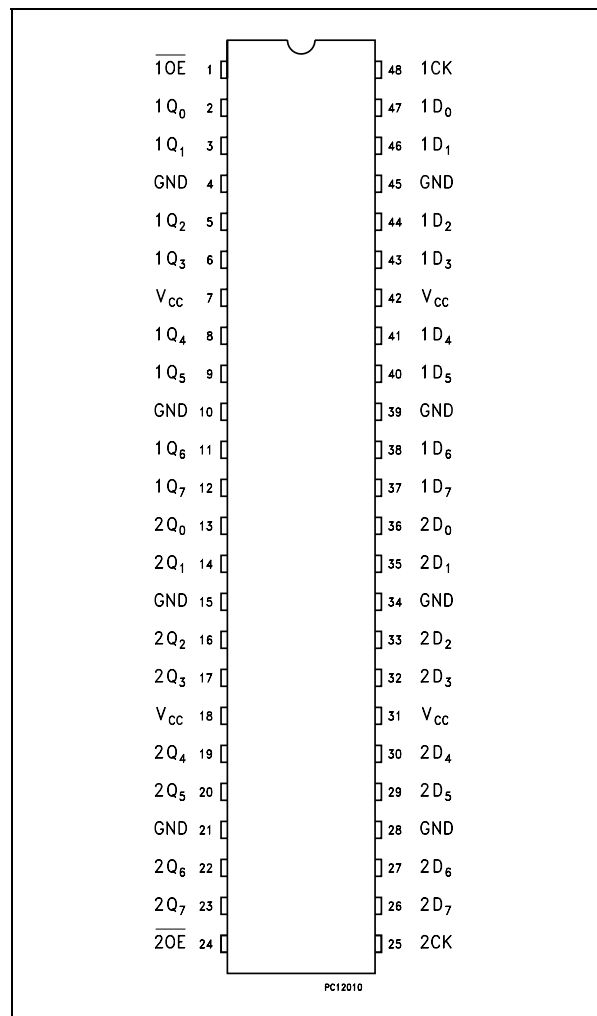
INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	1OE	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2OE	3 State Output Enable Input (Active LOW)
25	2CK	Clock Input (LOW-to-HIGH Edge Trigger)
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1CK	Clock Input (LOW-to-HIGH Edge Trigger)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V <sub>CC</sub>	Positive Supply Voltage

IEC LOGIC SYMBOLS

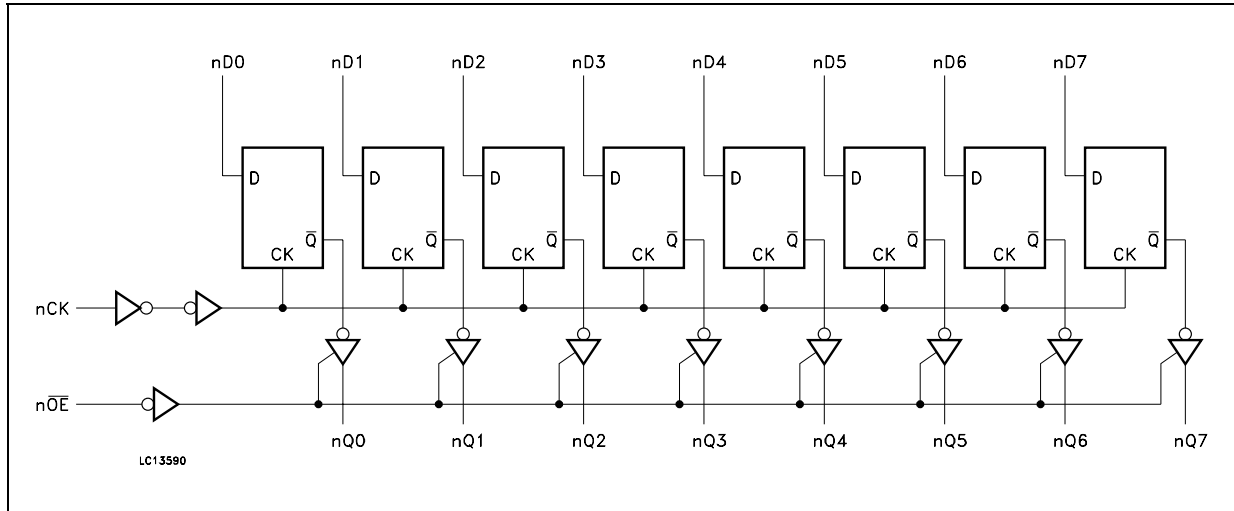


TRUTH TABLE

INPUTS			OUTPUTS
OE	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X : Don't Care  
Z : High Impedance

## LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	DC Input Diode Current	- 20	mA
$I_{OK}$	DC Output Diode Current	$\pm 20$	mA
$I_O$	DC Output Current	$\pm 25$	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current	$\pm 75$	mA
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$
$T_L$	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply Voltage	4.5 to 5.5	V
$V_I$	Input Voltage	0 to 5.5	V
$V_O$	Output Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time (note 1) ( $V_{CC} = 5.0 \pm 0.5V$ )	0 to 20	ns/V

1)  $V_{IN}$  from 0.8V to 2.0V

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### DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V <sub>OH</sub>	High Level Output Voltage	4.5	I <sub>O</sub> = -50 μA	4.4	4.5		4.4		4.4		V
		4.5	I <sub>O</sub> = -8 mA	3.94			3.8		3.7		
V <sub>OL</sub>	Low Level Output Voltage	4.5	I <sub>O</sub> = 50 μA		0.0	0.1		0.1		0.1	V
		4.5	I <sub>O</sub> = 8 mA			0.36		0.44		0.55	
I <sub>OZ</sub>	High Impedance Output Leakage Current	5.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND			±0.25		± 2.5		± 2.5	μA
I <sub>I</sub>	Input Leakage Current	0 to 5.5	V <sub>I</sub> = 5.5V or GND			± 0.1		± 1		± 1	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND			4		40		40	μA

### AC ELECTRICAL CHARACTERISTICS (Input t<sub>r</sub> = t<sub>f</sub> = 3ns)

Symbol	Parameter	Test Condition		Value						Unit		
		V <sub>CC</sub> (V)	C <sub>L</sub> (pF)		T <sub>A</sub> = 25°C			-40 to 85°C			-55 to 125°C	
					Min.	Typ.	Max.	Min.	Max.		Min.	Max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time CK to Q	5.0 <sup>(*)</sup>	15		5.6	9.4	1.0	10.5	1.0	10.5	ns	
		5.0 <sup>(*)</sup>	50		6.4	10.4	1.0	11.5	1.0	11.5		
t <sub>PZL</sub> t <sub>PZH</sub>	Output Enable Time	5.0 <sup>(*)</sup>	15	R <sub>L</sub> = 1KΩ	6.2	10.2	1.0	11.5	1.0	11.5	ns	
		5.0 <sup>(*)</sup>	50		7.3	11.2	1.0	12.5	1.0	12.5		
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time	5.0 <sup>(*)</sup>	50	R <sub>L</sub> = 1KΩ	7.0	11.2	1.0	12.0	1.0	12.0	ns	
t <sub>w</sub>	Clock Pulse Width HIGH or LOW	5.0 <sup>(*)</sup>			6.5			6.5		6.5	ns	
t <sub>s</sub>	Setup Time D to CK HIGH or LOW	5.0 <sup>(*)</sup>			2.5			2.5		2.5	ns	
t <sub>h</sub>	Hold Time D to CK HIGH or LOW	5.0 <sup>(*)</sup>			2.5			2.5		2.5	ns	
f <sub>MAX</sub>	Maximum Clock Frequency	5.0 <sup>(*)</sup>	15		90	140		110		80	MHz	
		5.0 <sup>(*)</sup>	50		85	130		75		75		
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew time (note 1)	5.0 <sup>(*)</sup>	50			1.0		1.0		1.0	ns	

(\*) Voltage range is 5.0V ± 0.5V

(Note 1 : Parameter guaranteed by design. t<sub>soLH</sub> = |t<sub>pLHm</sub> - t<sub>pLHn</sub>|; t<sub>soHL</sub> = |t<sub>pHLm</sub> - t<sub>pHLn</sub>|

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C <sub>IN</sub>	Input Capacitance				4	10		10		10	pF
C <sub>OUT</sub>	Output Capacitance				6						pF
C <sub>PD</sub>	Power Dissipation Capacitance (note 1)	5.0	f <sub>IN</sub> = 10MHz		21						pF

1) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I<sub>CC(opr)</sub> = C<sub>PD</sub> × V<sub>CC</sub> × f<sub>IN</sub> + I<sub>CC</sub>/16 (per Latch)

## DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V <sub>OLP</sub>	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C <sub>L</sub> = 50 pF		0.6	0.9					V
V <sub>OLV</sub>				-0.9	-0.6						
V <sub>IHD</sub>	Dynamic High Voltage Input (note 1, 3)	5.0		3.5							V
V <sub>ILD</sub>	Dynamic Low Voltage Input (note 1, 3)	5.0				1.5					V

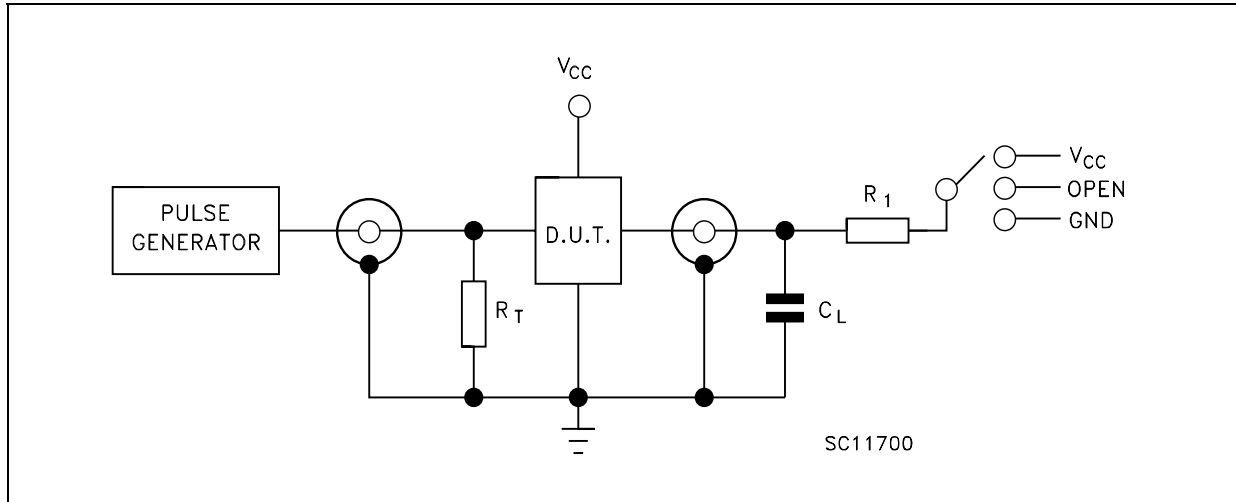
1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f=1MHz.

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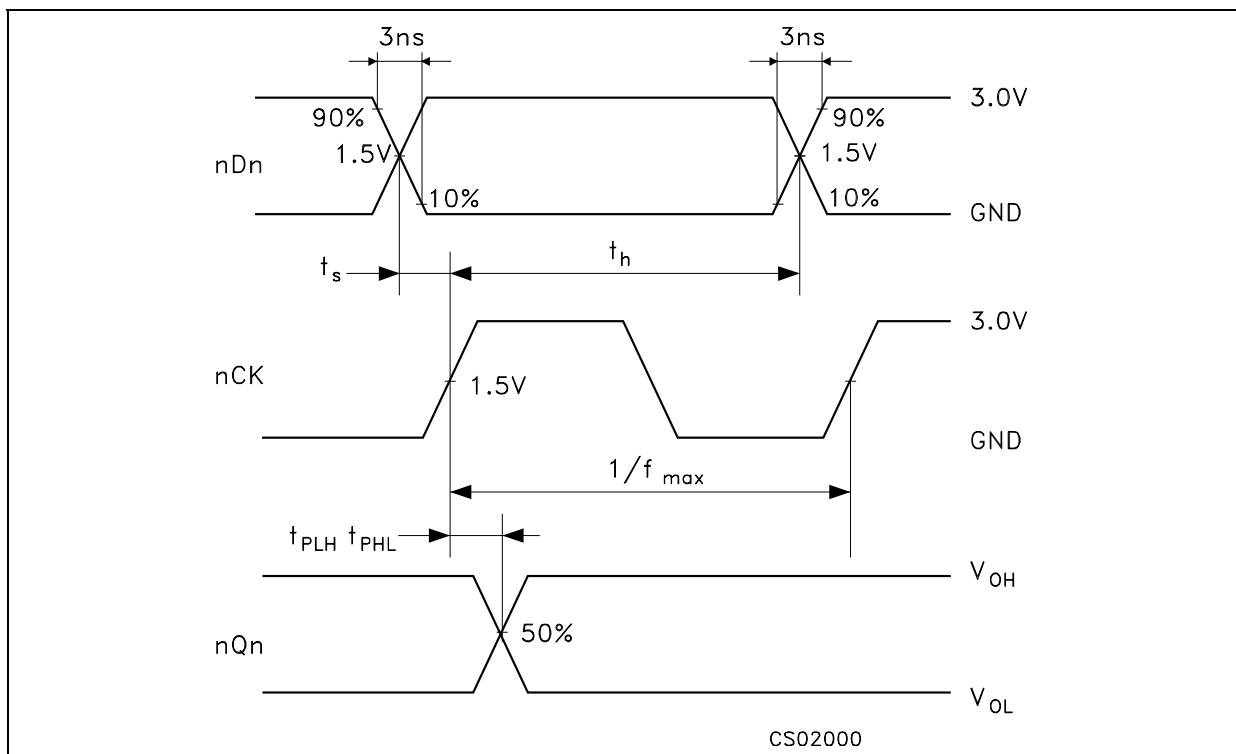
## TEST CIRCUIT

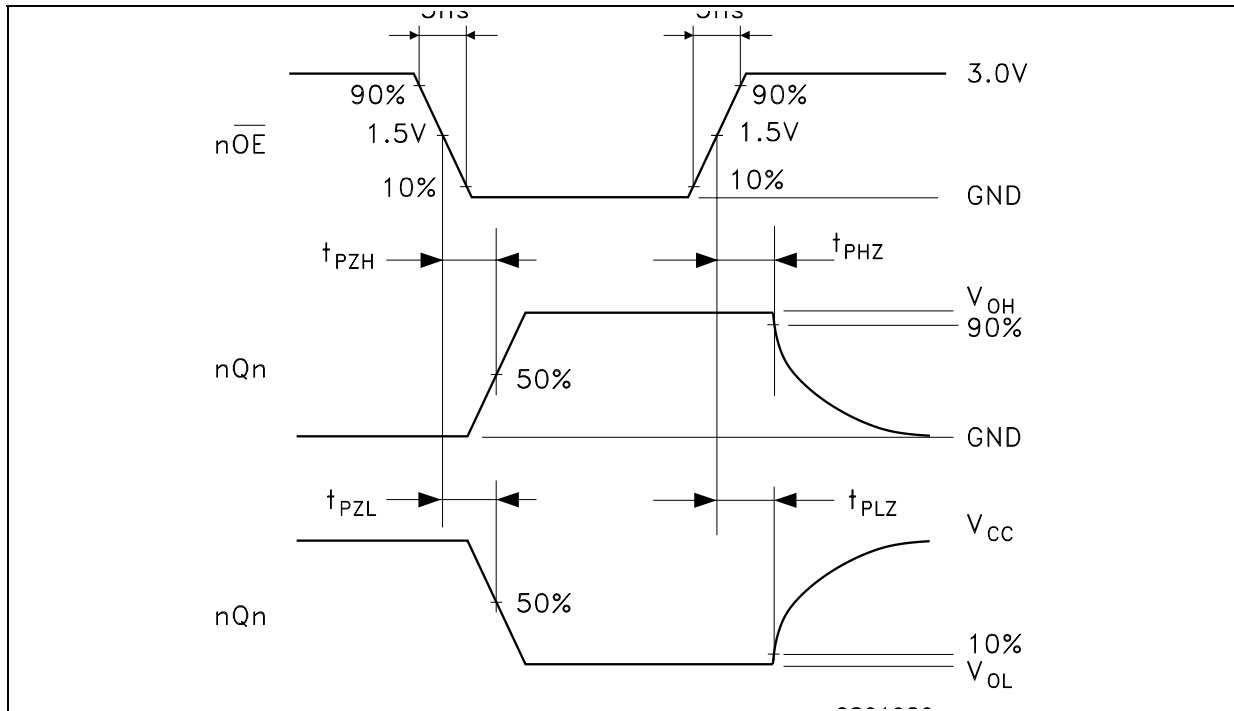
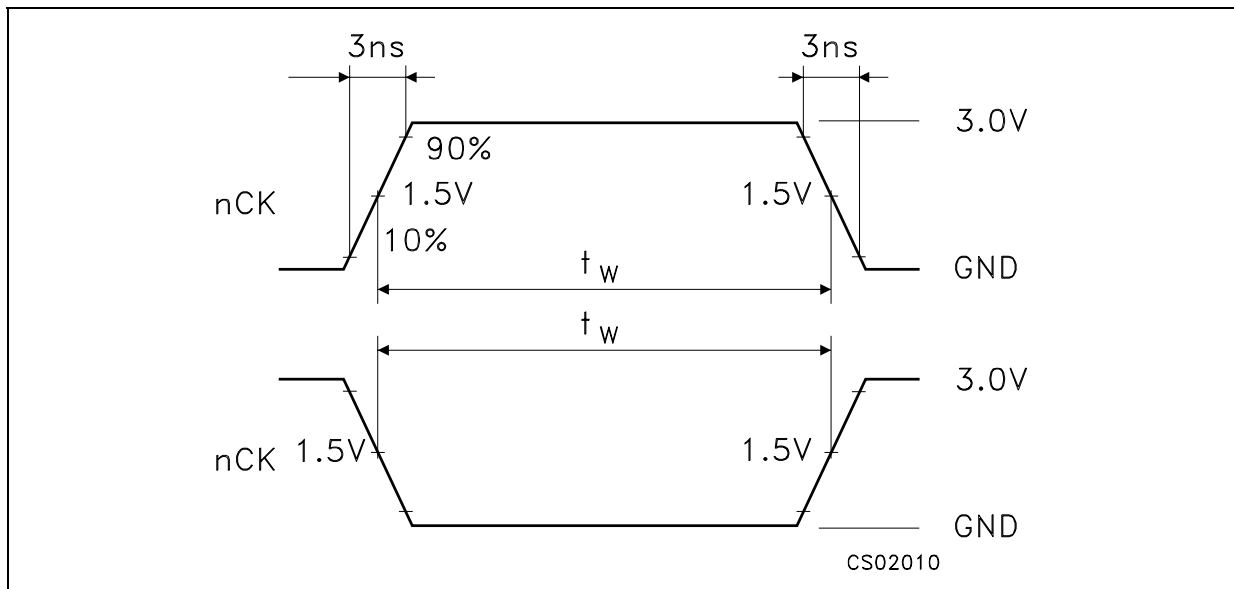


TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 15/50$  pF or equivalent (includes jig and probe capacitance)  
 $R_1 = R_T = 1K\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

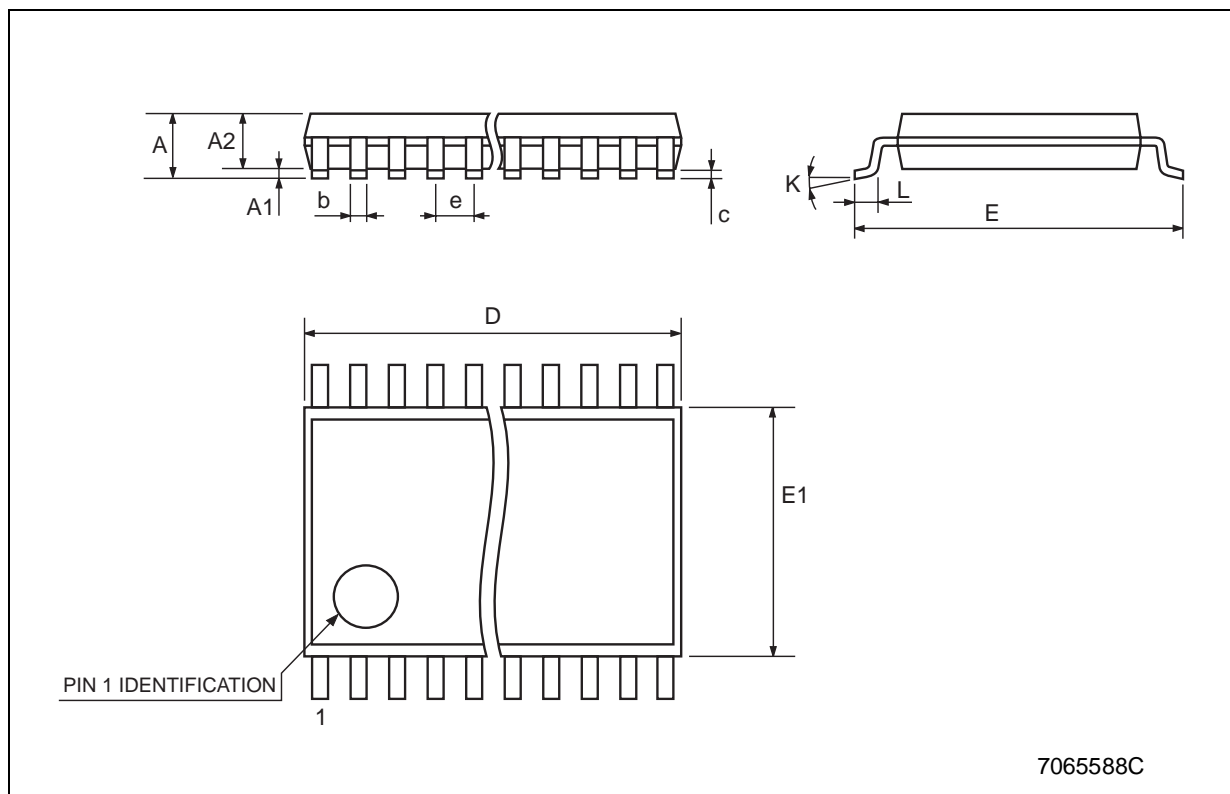
## WAVEFORM 1 : PROPAGATION DELAYS, SETUP AND HOLD TIMES, MAXIMUM CLOCK FREQUENCY ( $f=1MHz$ ; 50% duty cycle)



**WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME** ( $f=1\text{MHz}$ ; 50% duty cycle)**WAVEFORM 3 : CLOCK PULSE WIDTH** ( $f=1\text{MHz}$ ; 50% duty cycle)

## TSSOP48 MECHANICAL DATA

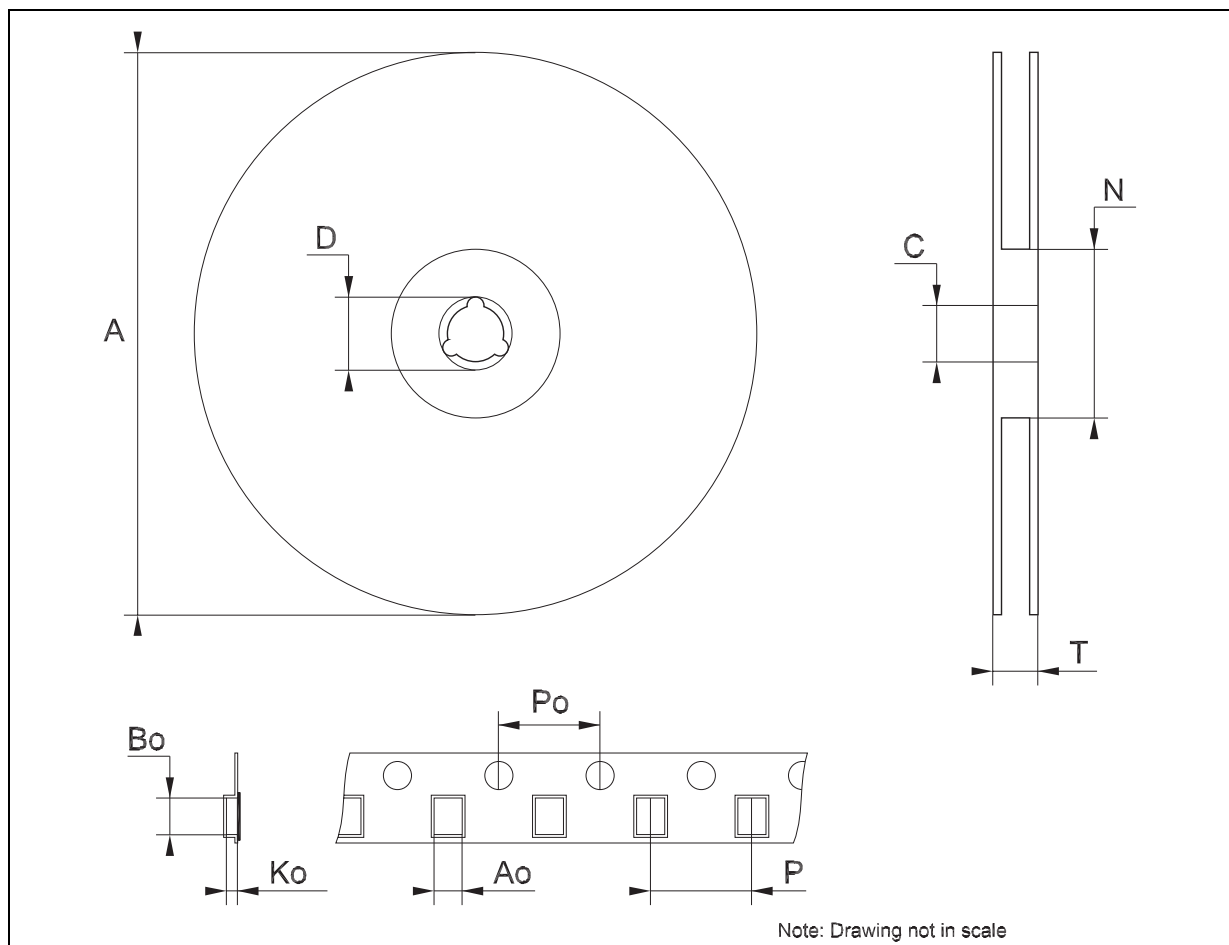
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030





## Tape &amp; Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



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