



# STP40NF10L

## N-CHANNEL 100V - 0.028Ω - 40A TO-220 LOW GATE CHARGE STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP40NF10L	100 V	< 0.033 Ω	40 A

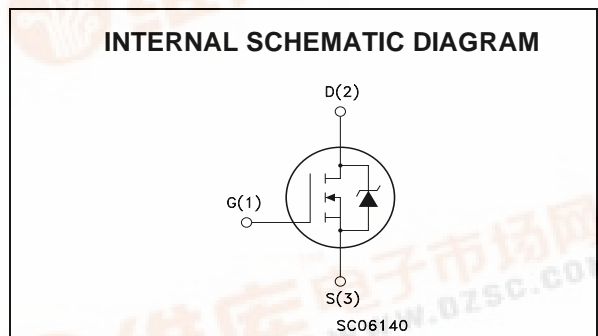
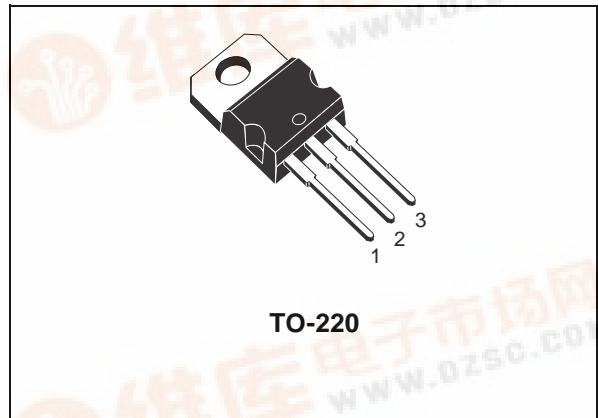
- TYPICAL R<sub>DS(on)</sub> = 0.028Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- APPLICATION ORIENTED CHARACTERIZATION

### DESCRIPTION

This Power Mosfet series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

### APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL
- AUTOMOTIVE



### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	100	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	100	V
V <sub>GS</sub>	Gate- source Voltage	± 17	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	40	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	25	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	160	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	150	W
	Derating Factor	1	W/°C
E <sub>AS</sub> (1)	Single Pulse Avalanche Energy	430	mJ
T <sub>stg</sub>	Storage Temperature	-65 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area

(1) Starting T<sub>j</sub> = 25°C, I<sub>D</sub> = 20A, V<sub>DD</sub> = 40V

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### THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	1	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300	°C

### ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 17V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.7	2.5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20 A V <sub>GS</sub> = 5V, I <sub>D</sub> = 20 A		0.028 0.030	0.033 0.036	Ω Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 20 A		25		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		2300		pF
C <sub>oss</sub>	Output Capacitance			290		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			125		pF

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50\text{ V}, I_D = 20\text{ A}$		25		ns
$t_r$	Rise Time	$R_G = 4.7\Omega, V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		82		ns
$Q_g$	Total Gate Charge	$V_{DD} = 80\text{ V}, I_D = 40\text{ A}, V_{GS} = 5\text{ V}$		46	64	nC
$Q_{gs}$	Gate-Source Charge			12		nC
$Q_{gd}$	Gate-Drain Charge			22		nC

**SWITCHING OFF**

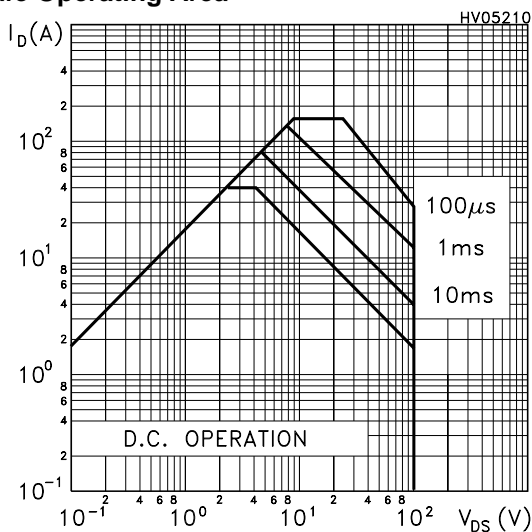
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 50\text{ V}, I_D = 20\text{ A},$		64		ns
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5\text{ V}$ (see test circuit, Figure 3)		24		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 80\text{ V}, I_D = 40\text{ A}$		51		ns
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 4.5\text{ V}$		29		ns
$t_c$	Cross-over Time	(see test circuit, Figure 3)		53		ns

**SOURCE DRAIN DIODE**

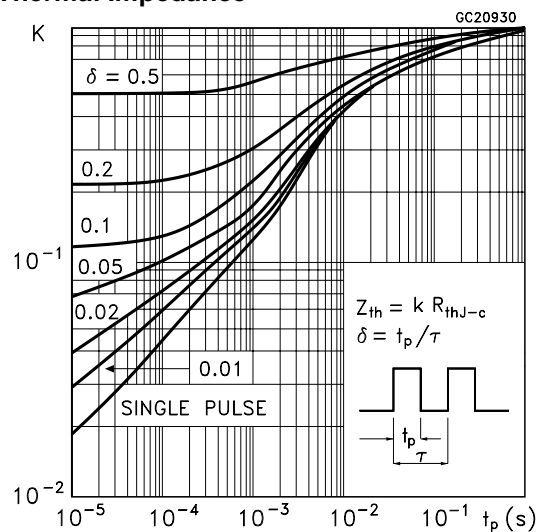
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				40	A
$I_{SDM} (1)$	Source-drain Current (pulsed)				160	A
$V_{SD} (2)$	Forward On Voltage	$I_{SD} = 40\text{ A}, V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 40\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$		110		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 30\text{ V}, T_j = 150^\circ\text{C}$		467		nC
$I_{RRM}$	Reverse Recovery Current	(see test circuit, Figure 5)		8		A

Note: 1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.

**Safe Operating Area**

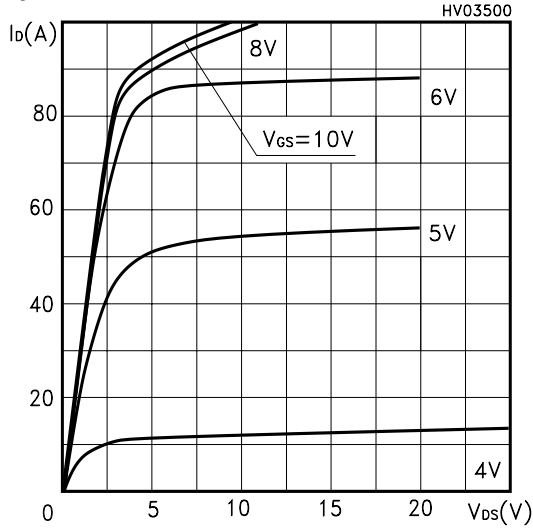


**Thermal Impedance**

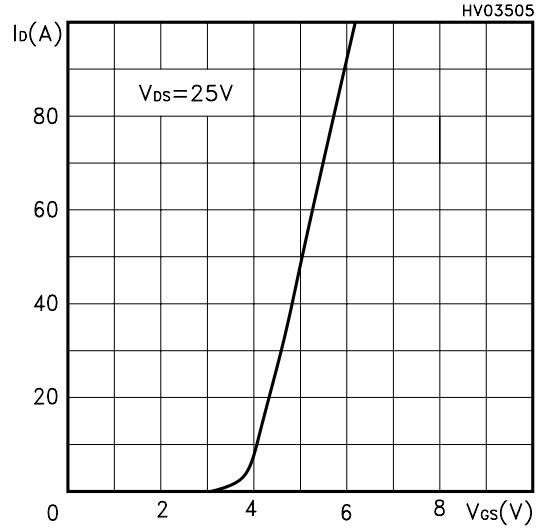


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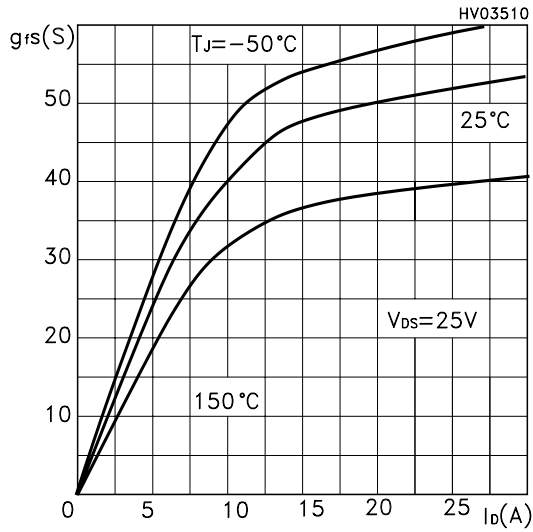
**Output Characteristics**



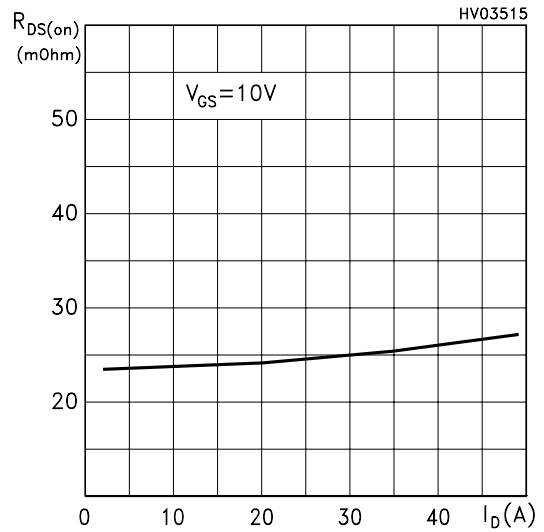
**Transfer Characteristics**



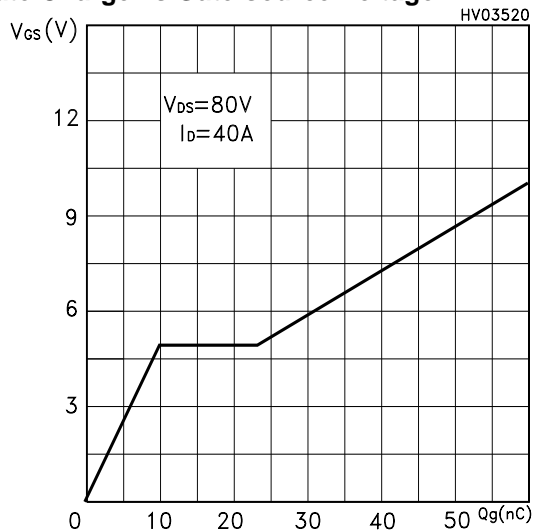
**Transconductance**



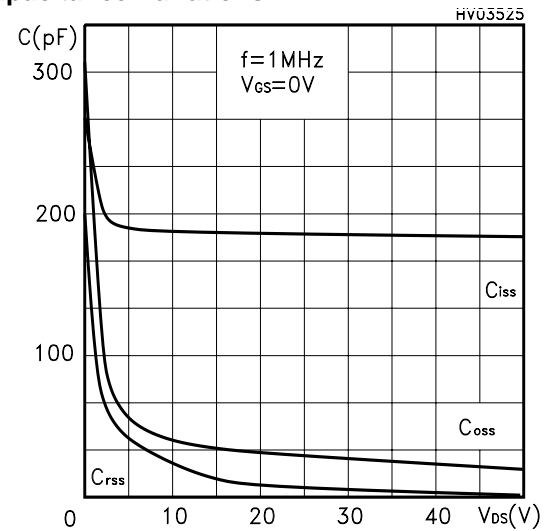
**Static Drain-source On Resistance**



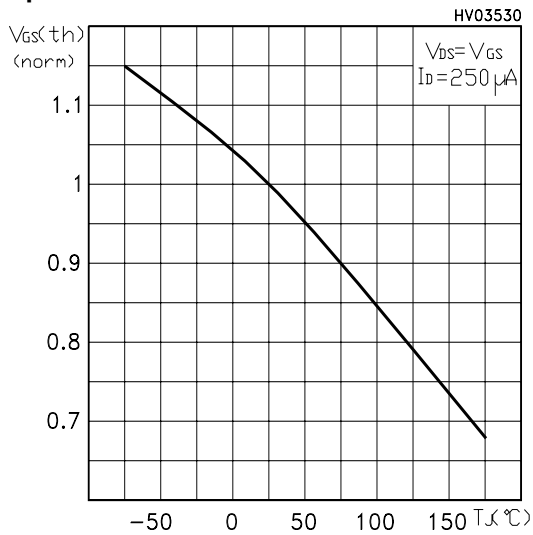
**Gate Charge vs Gate-source Voltage**



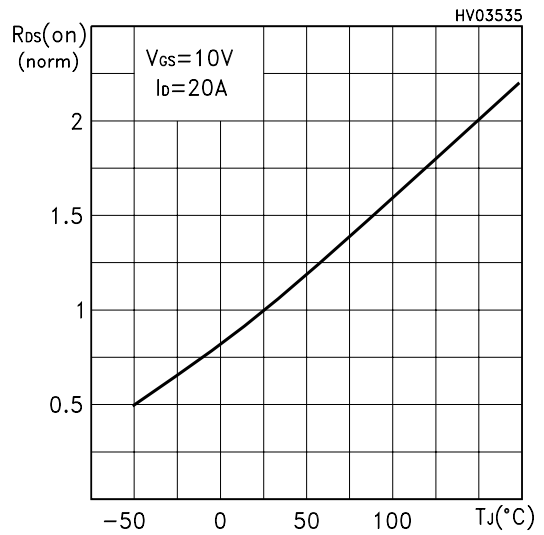
**Capacitance Variations**



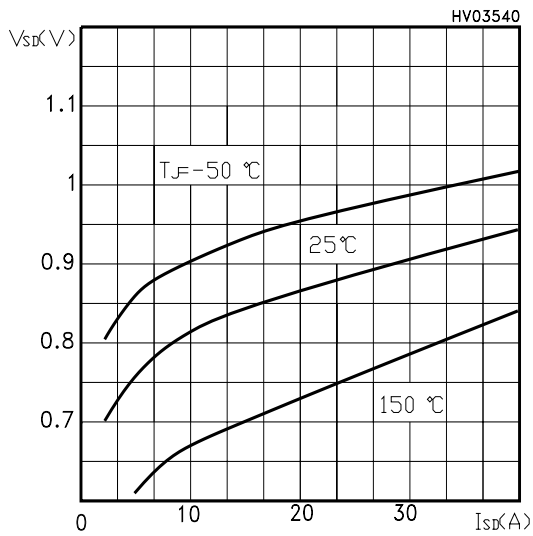
**Normalized Gate Threshold Voltage vs Temperature**



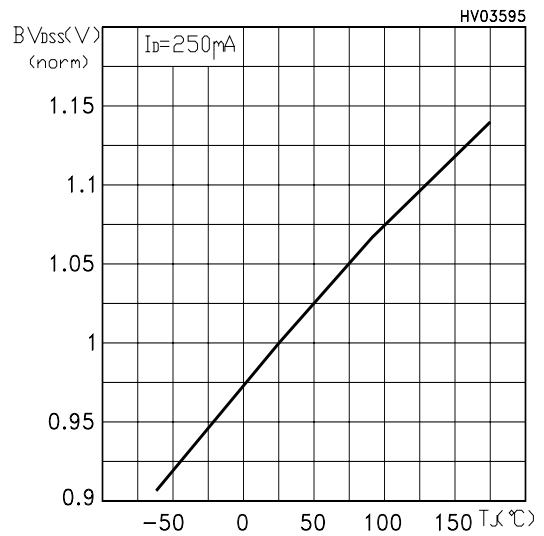
**Normalized On Resistance vs Temperature**



**Source-drain Diode Forward Characteristics**

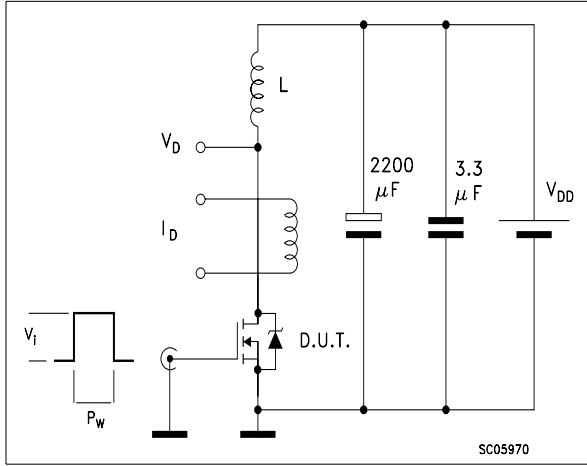


**Normalized Drain-Source Breakdown vs Temperature**

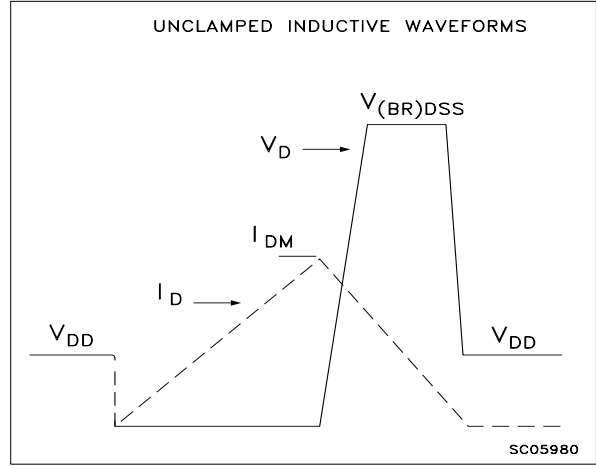


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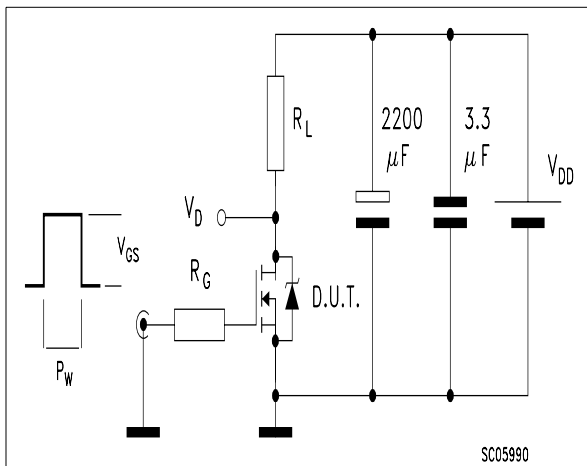
**Fig. 1: Unclamped Inductive Load Test Circuit**



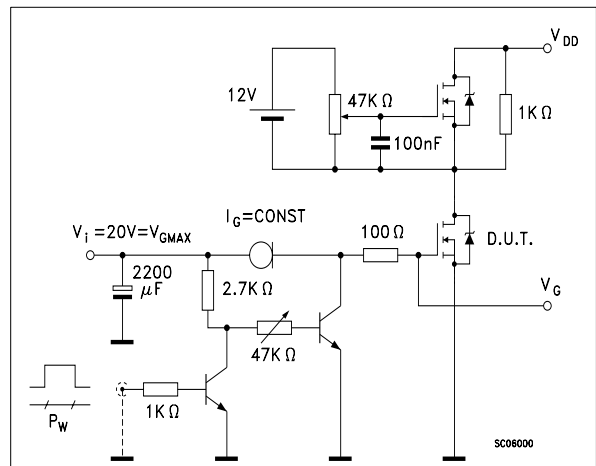
**Fig. 2: Unclamped Inductive Waveform**



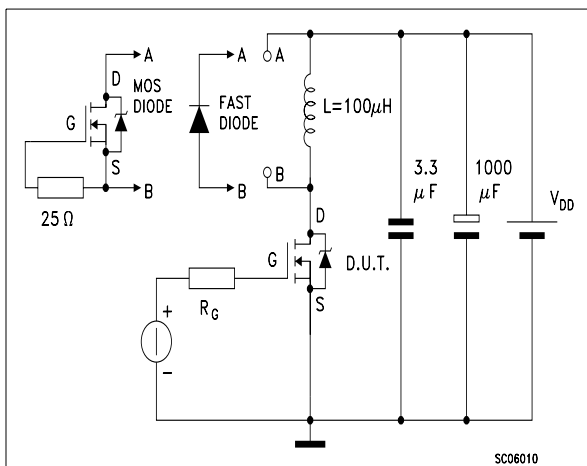
**Fig. 3: Switching Times Test Circuit For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

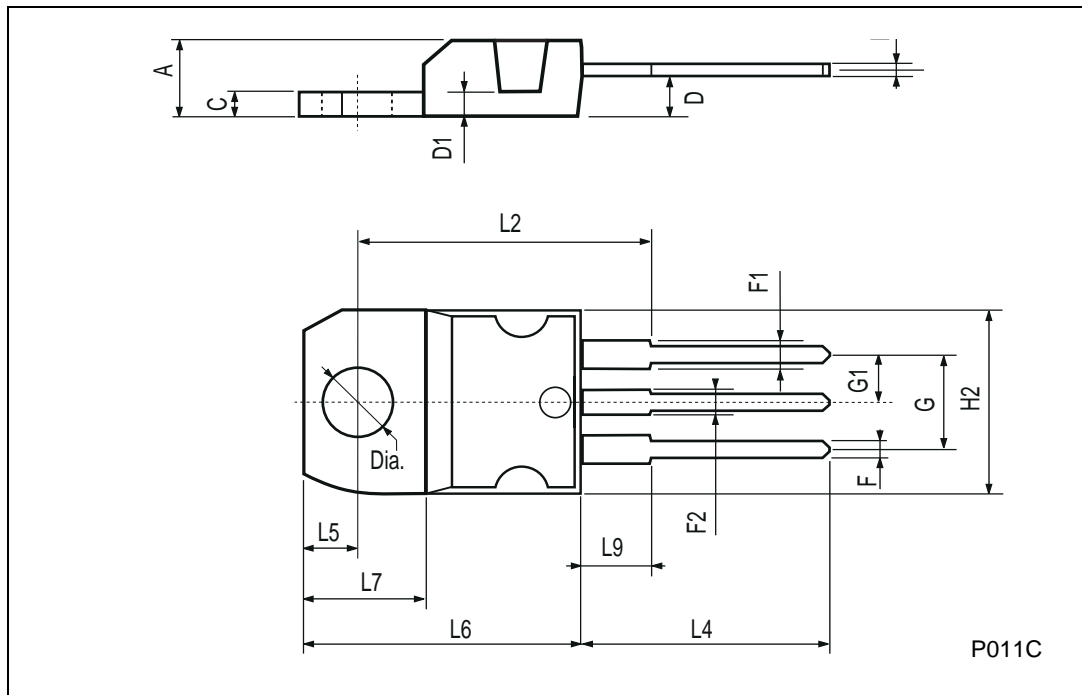


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



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