ESDALC6V1P6

QUAD LOW CAPACITANCE TRANSIL™ ARRAY FOR ESD PROTECTION

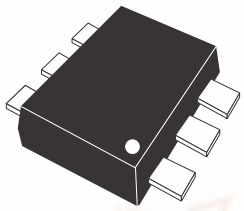
Application Specific Discretes
A.S.D.

MAIN APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

This device is particularly adapted to the protection of symmetrical signals.

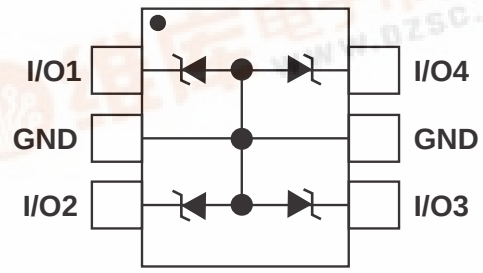


SOT666

FEATURES

- 4 UNIDIRECTIONAL TRANSIL™ FUNCTIONS.
- BREAKDOWN VOLTAGE V_{BR} = 6.1V MIN.
- LOW DIODE CAPACITANCE (12pF @ 0V)
- LOW LEAKAGE CURRENT < 500 nA
- VERY SMALL PCB AREA < 2.6 mm^2

FUNCTIONAL DIAGRAM



DESCRIPTION

The ESDALC6V1P6 is a monolithic array designed to protect up to 4 lines against ESD transients.

This device is ideal for applications where both reduced line capacitance and board space saving are required.

BENEFITS

- High ESD protection level.
- High integration.
- Suitable for high density boards.

COMPLIES WITH THE FOLLOWING STANDARDS :

- IEC61000-4-2 level 4: 15 kV (air discharge)
  8 kV (contact discharge)
- MIL STD 883E-Method 3015-7: class 3
  25kV HBM (Human Body Model)

ABSOLUTE RATINGS (T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Value	Unit
V_{PP}	ESD discharge - IEC61000-4-2 air discharge IEC61000-4-2 contact discharge		± 15 ± 8	kV
P_{PP}	Peak pulse power (8/20 µs) (see note 1)	T_j initial = Tamb	30	W
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		- 55 to + 150	°C
T_L	Maximum lead temperature for soldering during 10s at N/A		260	°C
T_{op}	Operating temperature range		- 40 to + 125	°C

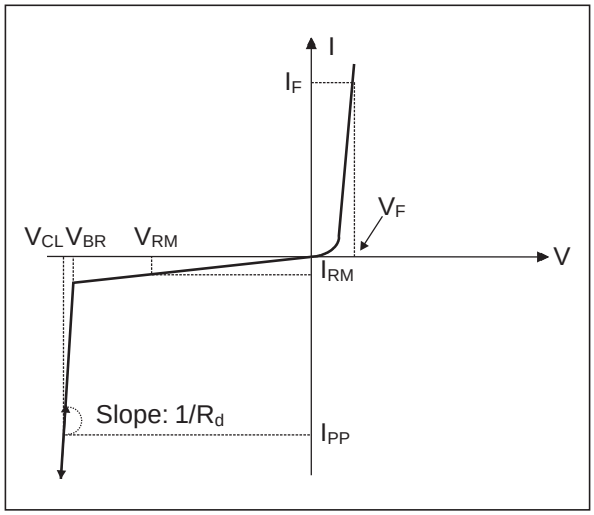
Note 1: for a surge greater than the maximum values, the diode will fail in short-circuit.

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient on printed circuit on recommended pad layout	220	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage tempature coefficient
V_F	Forward voltage drop
C	Capacitance per line
R_d	Dynamic resistance



Types	V_{BR} @ I_R			I_{RM} @ V_{RM}		Rd	αT	C
	min.	max.		max.		typ.	max.	typ. @ 0V
	V	V	mA	µA	V	Ω	10^{-4}/°C	pF
ESDALC6V1P6	6.1	7.2	1	0.5	3	1.5	4.5	12

Note 1 : Square pulse Ipp = 15A, tp=2.5µs.
Note 2 : $\Delta V_{BR} = \alpha T^* (Tamb - 25°C) * V_{BR} (25°C)$

Fig. 1: Relative variation of peak pulse power versus initial junction temperature.

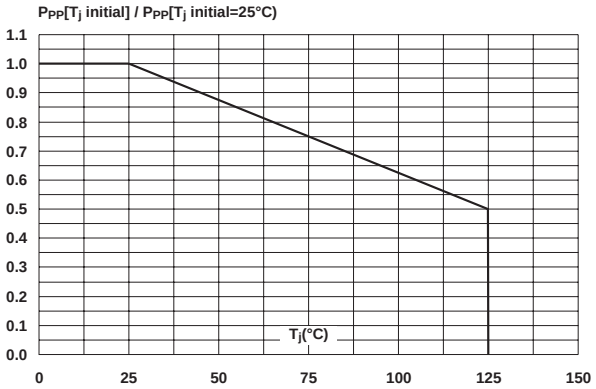


Fig. 2: Peak pulse power versus exponential pulse duration.

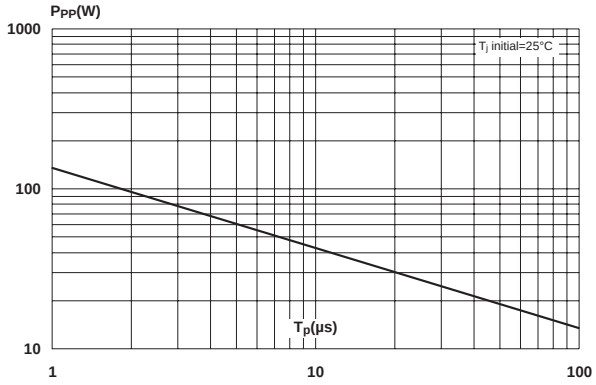


Fig. 3: Clamping voltage versus peak pulse current (typical values, rectangular waveform).

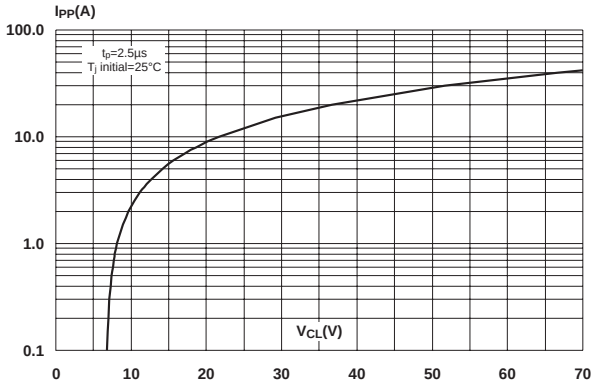


Fig. 4: Forward voltage drop versus peak forward current (typical values).

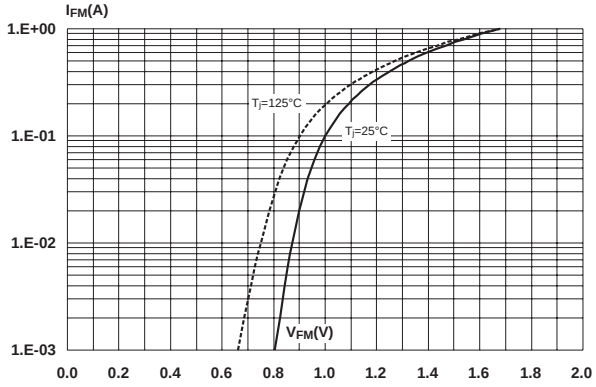


Fig. 5: Junction capacitance versus reverse voltage applied (typical values).

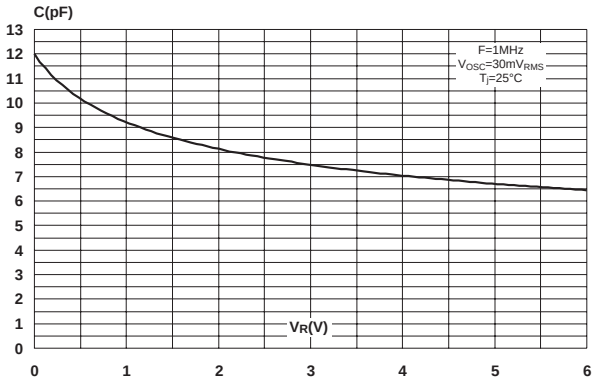
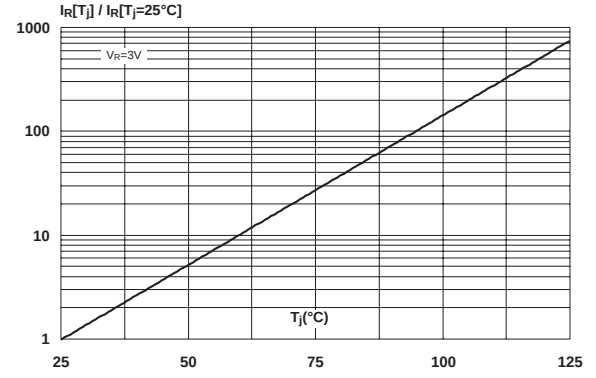


Fig. 6: Relative variation of leakage current versus junction temperature (typical values).



TECHNICAL INFORMATION

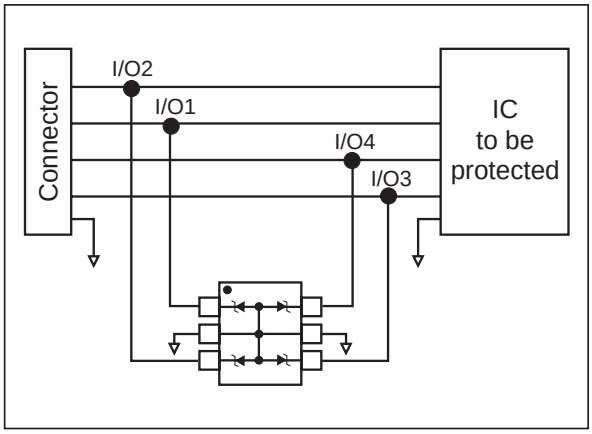
1. ESD protection by ESDALC6V1P6

With the focus of lowering the operation levels, the problem of malfunction caused by the environment is critical. Electrostatic discharge (ESD) is a major cause of failure in electronic systems.

As a transient voltage suppressor, the ESDALC6V1P6 is an ideal choice for ESD protection by suppressing ESD events. It is capable of clamping the incoming transient to a low enough level such that any damage is prevented on the device to be protected by ESDALC6V1P6.

ESDALC6V1P6 serves as a parallel protection element, connected between signal line and ground. As the transient rises above the operating voltage of the device, the ESDALC6V1P6 becomes a low impedance path diverting the transient current to ground.

Fig. A1: Application example.

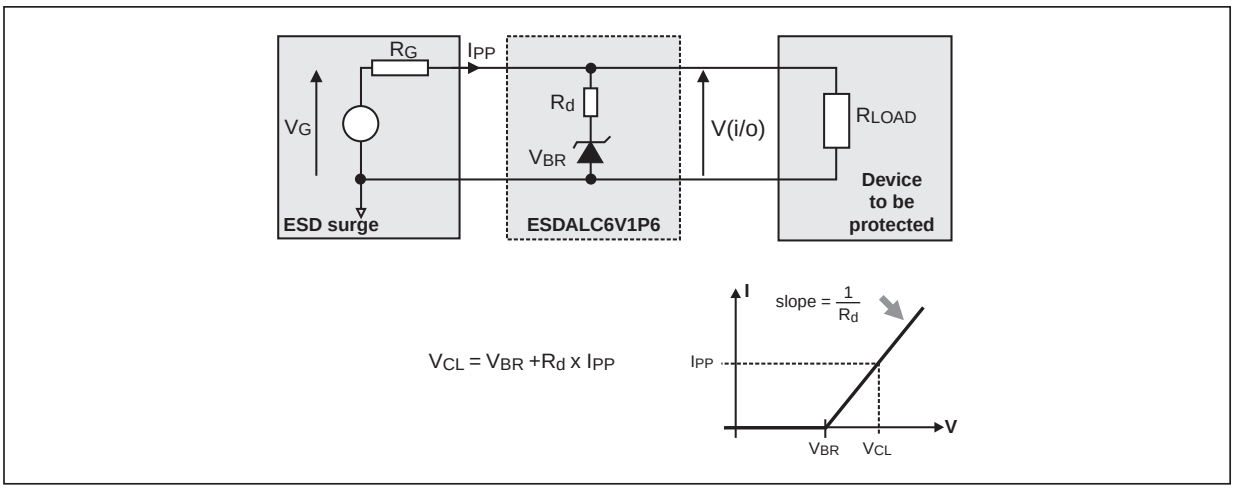


The clamping voltage is given by the following formula:

$$V_{CL} = V_{BR} + R_d.I_{PP}$$

As shown in figure A2, the ESD strikes are clamped by the transient voltage suppressor.

Fig. A2: ESD clamping behavior.



To have a good approximation of the remaining voltages at both Vi/o side, we provide the typical dynamical resistance value R_d. By taking into account the following hypothesis:

$$R_G > R_d \text{ and } R_{load} > R_d$$

we have:

$$V(i/o) = V_{BR} + R_d \times \frac{V_g}{R_g}$$

The results of the calculation done for V_G = 8kV, R_G = 330Ω (IEC61000-4-2 standard), V_{BR} = 6.4V (typ.) and R_d = 1.5Ω (typ.) give:

$$V(i/o) = 42.8 Volts$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be a few tenths of volts during a few ns at the Vi/o side.

Fig. A3: ESD test board.

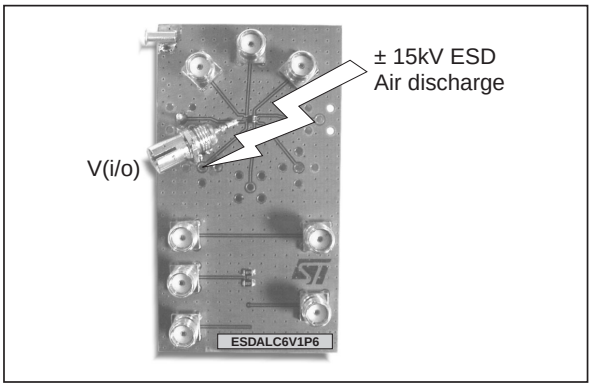
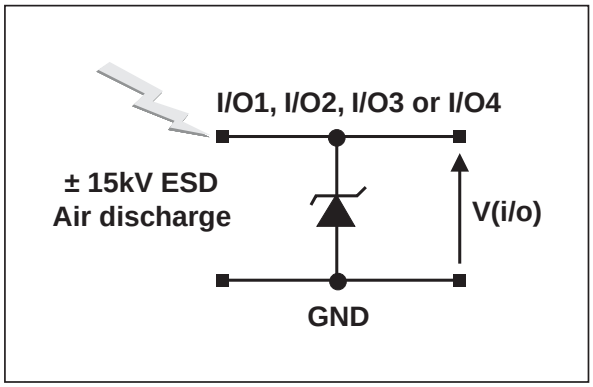
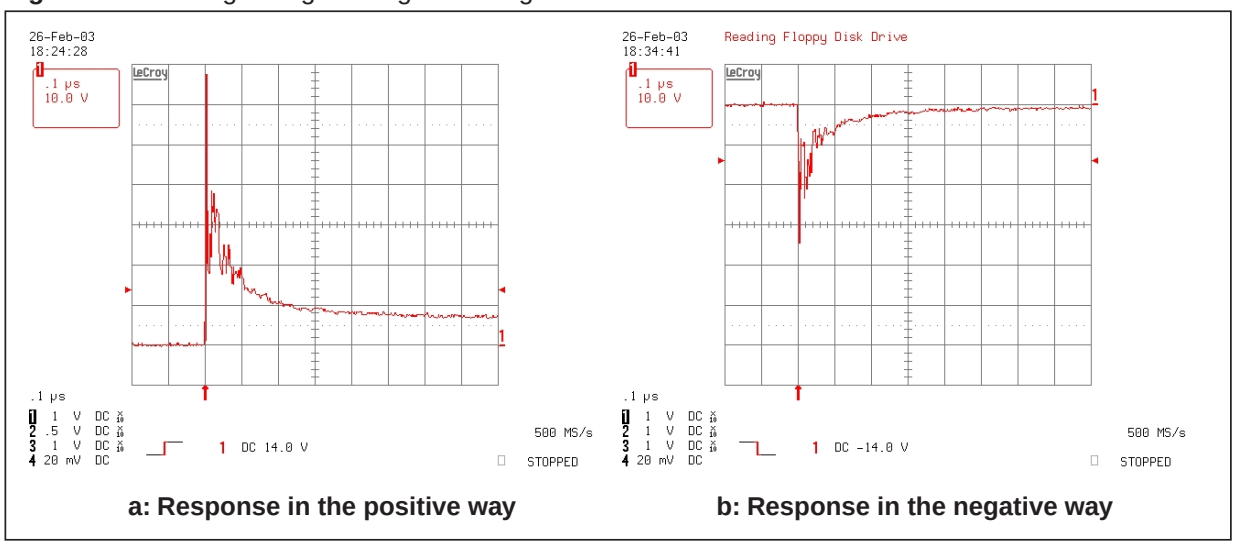


Fig. A4: ESD test configuration.



The measurements done here after show very clearly (figure A5) the high efficiency of the ESD protection: the clamping voltage V(i/o) becomes very close to V_{BR} (positive way, figure A5a) and $-V_F$ (negative way, figure A5b).

Fig. A5: Remaining voltage during ESD surge.



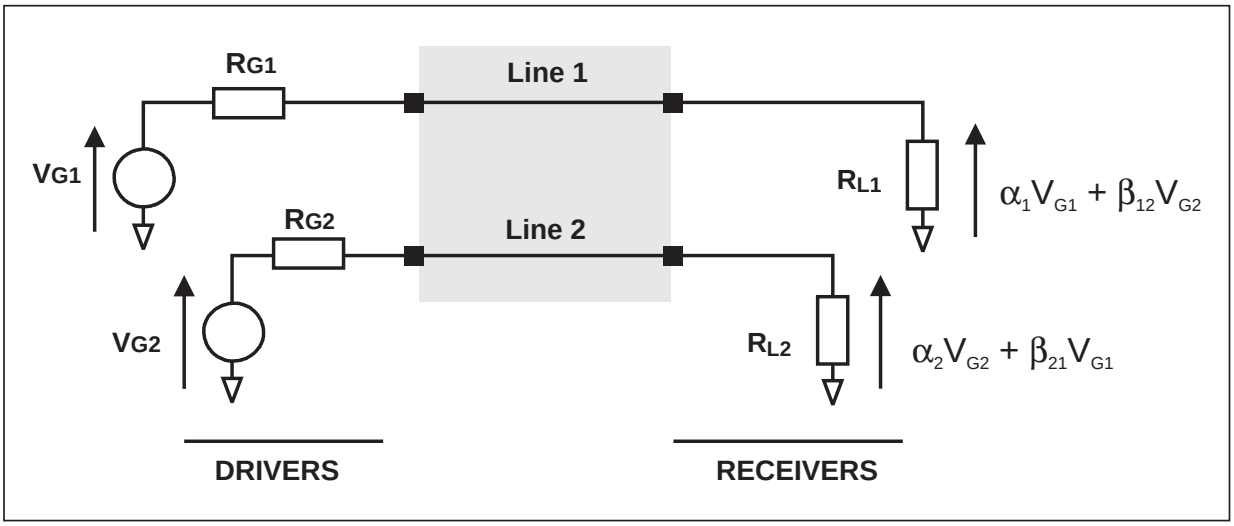
a: Response in the positive way

b: Response in the negative way

One can note that the ESDALC6V1P6 is not only acting for positive ESD surges but, also, for negative ones. For this kind of disturbances, it clamps close to ground voltage as shown in figure A5b.

2. Crosstalk behavior

Fig. A6: Crosstalk phenomenon**.**



The crosstalk phenomena are due to the coupling between 2 lines. Coupling factors (β12 or β21) increase when the gap across lines decreases, particularly in silicon dice. In the example above, the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G2}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Fig. A7: Analog crosstalk test configuration.

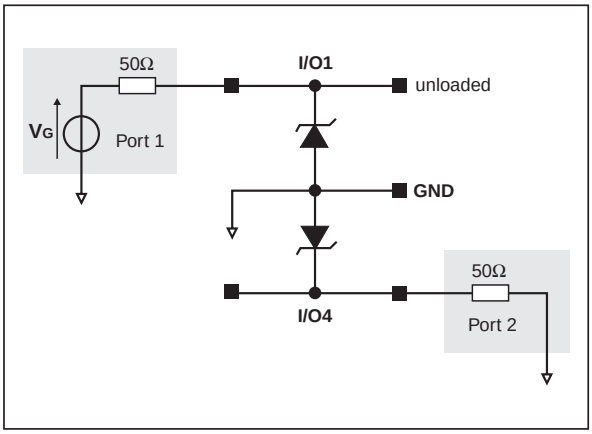


Fig. A8: Typical analog crosstalk response.

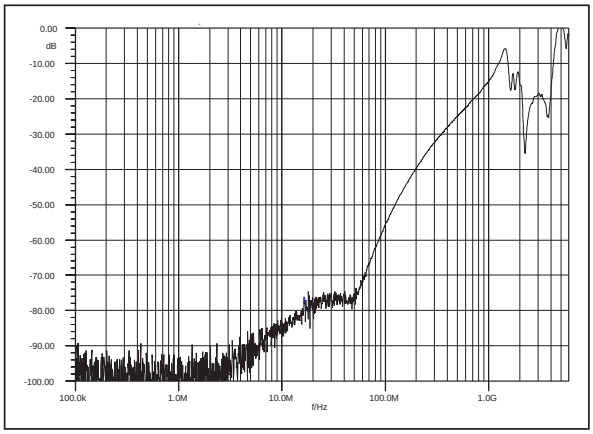


Figure A7 gives the measurement circuit for the analog crosstalk application. In figure 8, the curve shows the effect of the cell I/O1 on the cell I/O4. In usual frequency range of analog signals (up to 100 MHz) the effect on disturbed line is less than -55dB.

Fig. A9: Digital crosstalk test configuration.

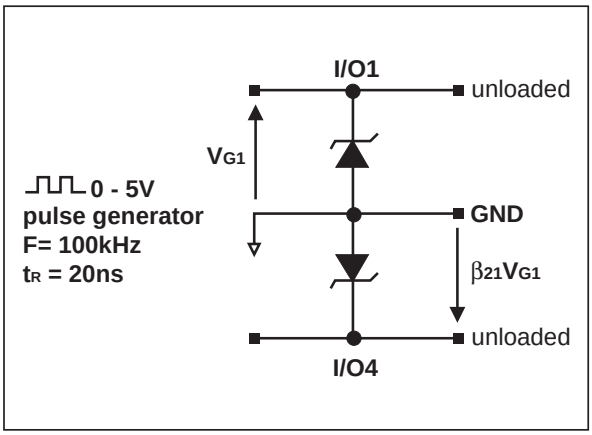


Fig. A10: Typical digital crosstalk response.

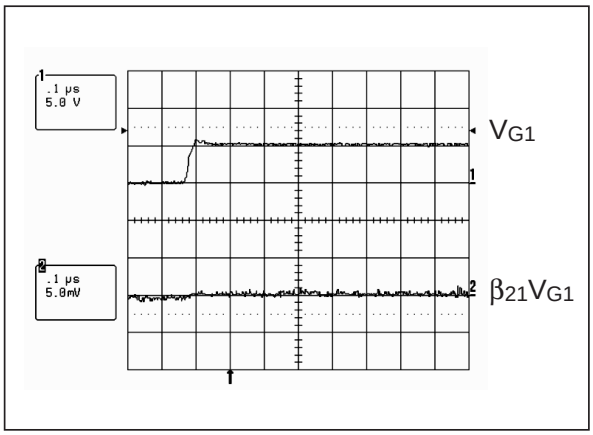


Figure A9 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A10 shows that in such a condition, ie signal from 0 to 5V and rise time of a few ns, the impact on the disturbed line is less than 5 mV peak to peak. No data disturbance was noted on the concerned line. The measurements performed with falling edges give an impact within the same range.

3. PCB layout recommendations

As ESD is a fast event, the di/dt caused by this surge is about 30A/ns (risetime=1ns, Ipeak=30A), that means each nH causes an overvoltage of 30V.

Thus, the circuit board layout is a critical design step in the suppression of ESD induced transients by reducing parasitic inductances. To ensure that, the following guidelines are recommended :

- The ESDALC6V1P6 should be placed as close as possible to the input terminals or connectors.
- The path length between the ESD suppressor and the protected line should be minimized.
- All conductive loops, including power and ground loops should be minimized.
- The ESD transient return path to ground should be kept as short as possible.
- The connections from the ground pins to the ground plane should be the shortest possible.

4. Comparison with varistors

	Varistors	TRANSIL™
Leakage current	--	+++
Protection efficiency	--	++
Ageing	--	++

Low leakage current for Transil™ device

- Improve the autonomy of portable equipments as mobile

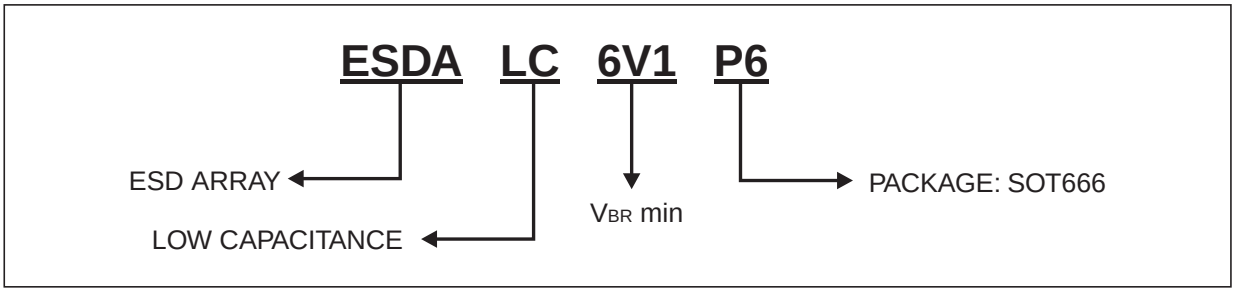
Better efficiency in terms of ESD protection by using Transil™ device

- Varistors are bidirectional devices and so are not suitable to protect sensitive ICs, because they will be submitted to high voltages in the negative way.
- Ratio V_{CL}/V_{BR} lower for Transil™ device
- Less dispersion in terms of V_{BR}

No ageing phenomena regarding ESD events with Transil™ device

- Higher efficiency in terms of ESD protection

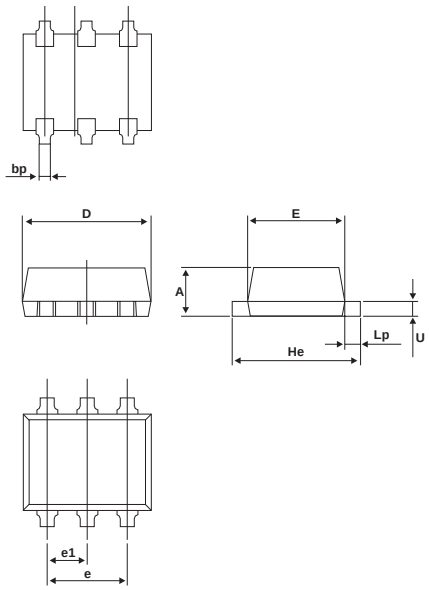
ORDER CODE



Ordering type	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1P6	D	SOT666	2.9 mg.	3000	Tape & reel

PACKAGE MECHANICAL DATA

SOT-666



REF.	DIMENSIONS			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.50	0.60	0.020	0.024
bp	0.17	0.27	0.007	0.011
c	0.08	0.18	0.003	0.007
D	1.50	1.70	0.060	0.067
E	1.10	1.30	0.043	0.051
e	1.00		0.040	
e1	0.50		0.020	
He	1.50	1.70	0.059	0.067
Lp	0.10	0.30	0.004	0.012

FOOT PRINT (in millimeters)