S6A0065

40 CH SEGMENT/COMMON DRIVER FOR DOT MATRIX LCD

June. 2001.

Ver. 0.0

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.

S6A0065 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	

CONTENTS

INTRODUCTION

The S6A0065 is a LCD driver IC which is fabricated by low power CMOS technology. Basically this IC consists of 20 x 2 bit bi-directional shift register, 20 x 2 bit data latch and 20 x 2 bit driver. (refer to Fig 1) This IC can be used as common or segment driver.

FUNCTION

— Dot matrix LCD driver with 40 channel output.

— Selects function to use common/segment drivers simultaneously.

— Input/Output signal

- Output: 20 x 2 channel waveform for LCD driving
- Input: Serial display data and control signal from the controller LSI.
  Bias voltage (V1-V6)

FEATURES

— Display driving bias: static - 1/5

— Power supply voltage: 2.7- 5.5V

— Supply voltage for display: 3.0 - 13.0V ($V_{LCD} = V_{DD} - V_{EE}$)

— Interface

Driver (cascade connection)	Controller
Other S6A0065, S6A2067	S6A0069 S6A0070 S6A0073

— CMOS Process

— 64QFP and bare chip available

BLOCK DIAGRAM

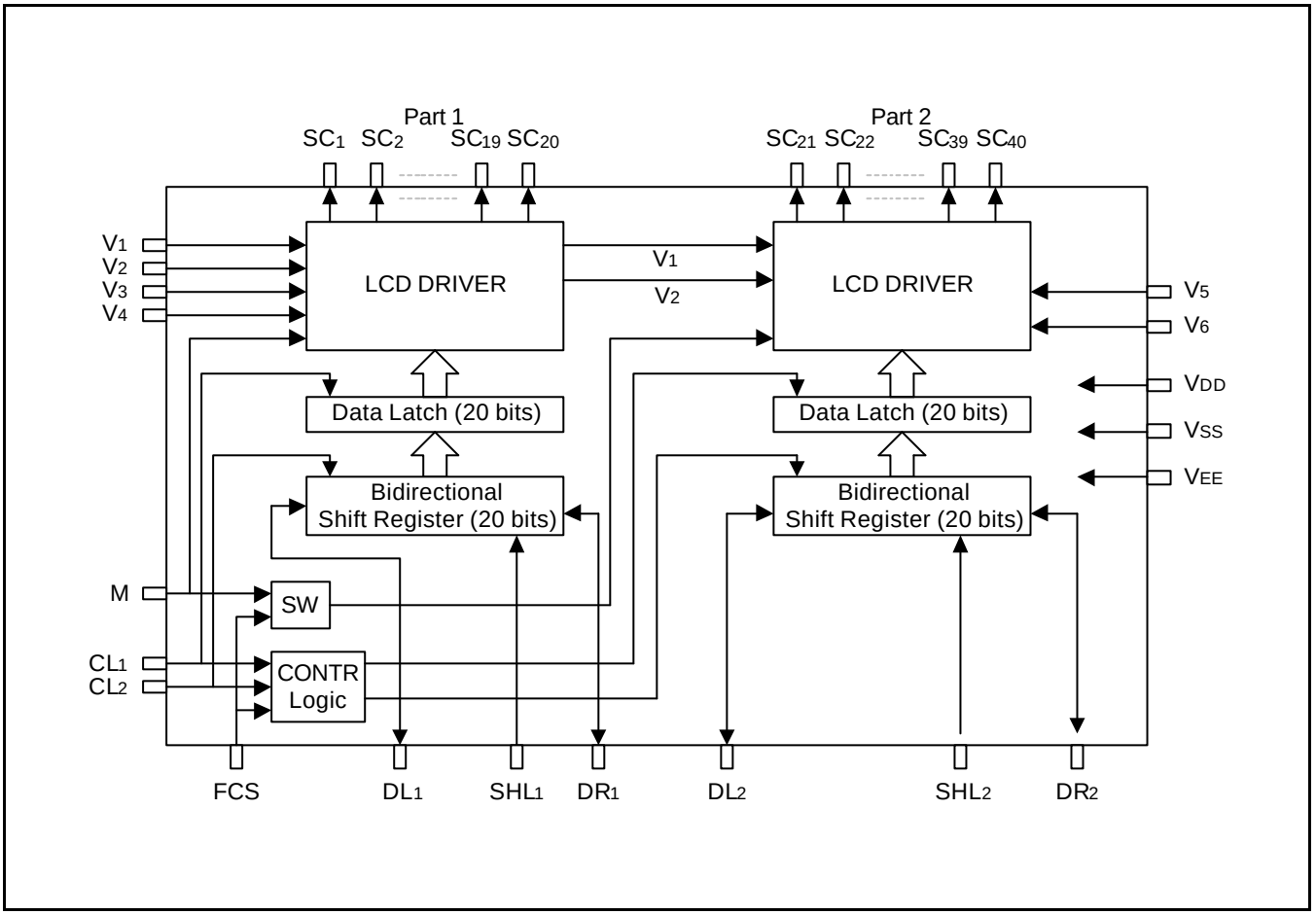


Figure 1. S6A0065 Functional Block Diagram

PIN CONFIGURATION

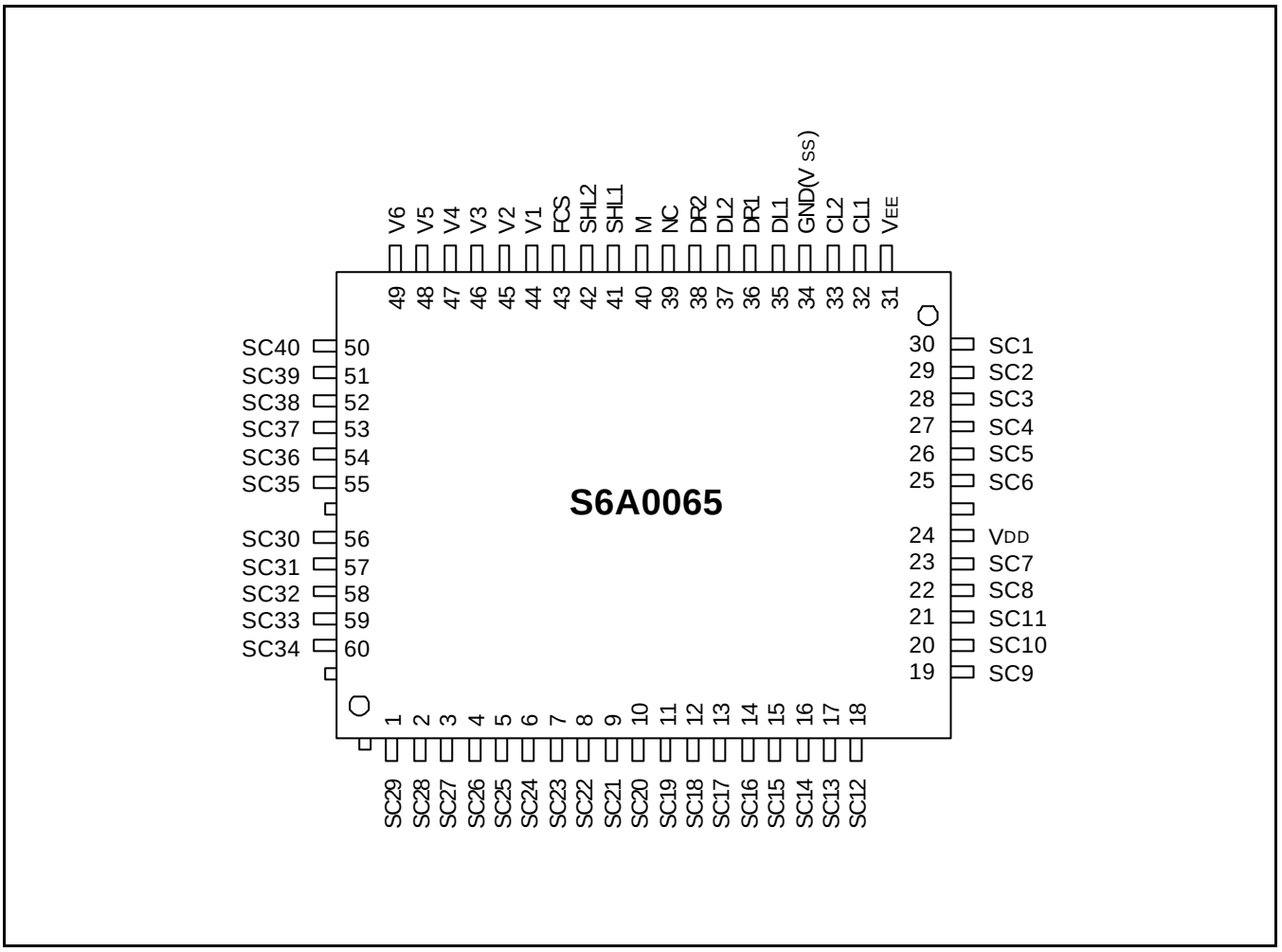
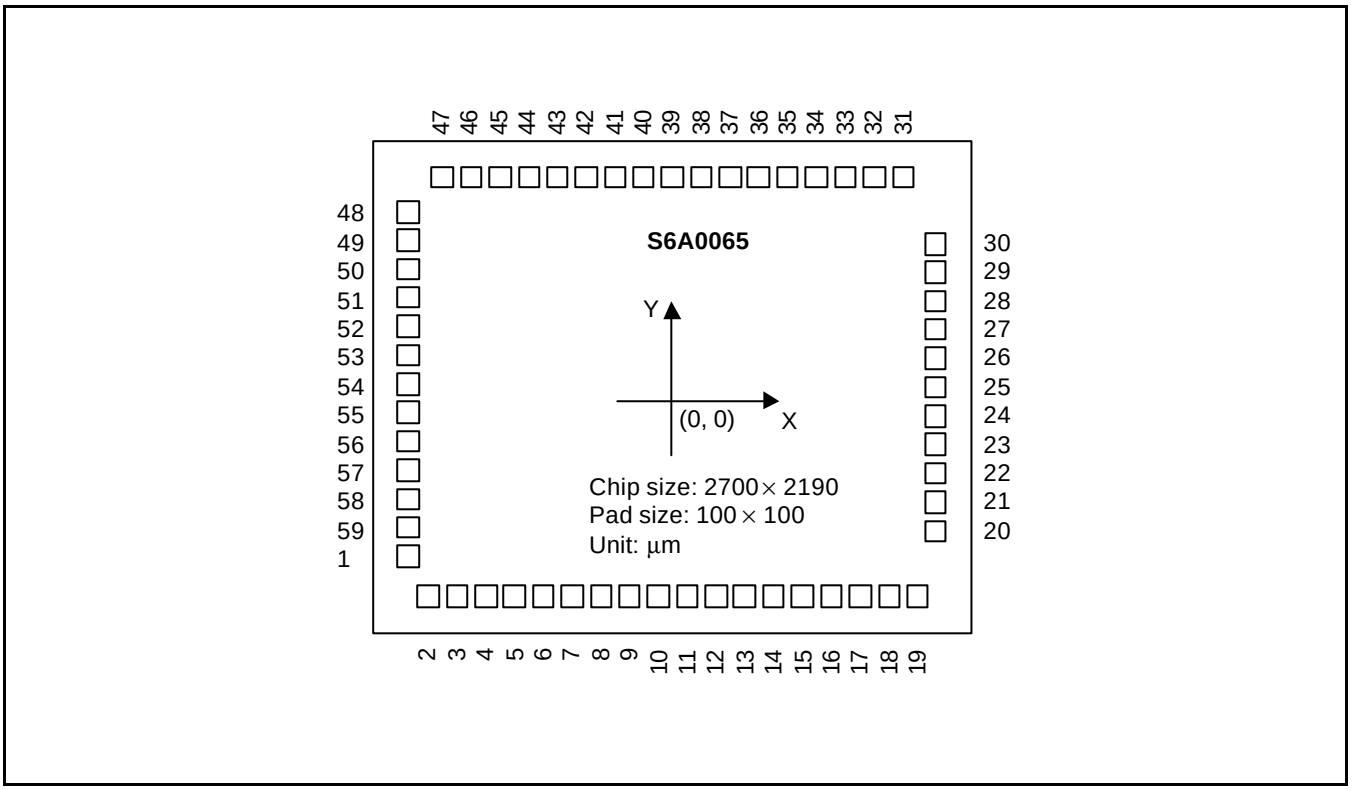


Figure 2. 60 QFP Top View

PAD DIAGRAM



NOTE: (0,0) is center in the chip

PAD CENTER COORDINATES

Pad Number	Pad Name	Coordinate		Pad Number	Pad Name	Coordinate	
		X	Y			X	Y
1	VEE	-1120.2	-642.5	31	SC28	1117.5	865.2
2	CL1	-1062.5	-865.2	32	SC27	992.5	865.2
3	CL2	-937.5	-865.2	33	SC26	867.5	865.2
4	VSS	-812.5	-865.2	34	SC25	742.5	865.2
5	DL1	-687.5	-865.2	35	SC24	617.5	865.2
6	DR1	-562.5	-865.2	36	SC23	492.5	865.2
7	DL2	-437.5	-865.2	37	SC22	367.5	865.2
8	DR2	-312.5	-865.2	38	SC21	242.5	865.2
9	M	-187.5	-865.2	39	SC20	117.5	865.2
10	SHL1	-62.5	-865.2	40	SC19	-7.5	865.2
11	SHL2	62.5	-865.2	41	SC18	-132.5	865.2
12	FCS	187.5	-865.2	42	SC17	-257.5	865.2
13	V1	332.5	-865.2	43	SC16	-382.5	865.2
14	V2	457.5	-865.2	44	SC15	-507.5	865.2
15	V3	582.5	-865.2	45	SC14	-632.5	865.2
16	V4	707.5	-865.2	46	SC13	-757.5	865.2
17	V5	832.5	-865.2	47	SC12	-882.5	865.2
18	V6	957.5	-865.2	48	SC9	-1120.2	857.2
19	SC40	1082.5	-865.2	49	SC10	-1120.2	732.5
20	SC39	1120.2	-627.5	50	SC11	-1120.2	607.5
21	SC38	1120.2	-502.5	51	SC8	-1120.2	482.5
22	SC37	1120.2	-377.5	52	SC7	-1120.2	357.5
23	SC36	1120.2	-252.5	53	VDD	-1120.2	232.5
24	SC35	1120.2	-127.5	54	SC6	-1120.2	107.5
25	SC30	1120.2	-2.5	55	SC5	-1120.2	-17.5
26	SC31	1120.2	122.5	56	SC4	-1120.2	-142.5
27	SC32	1120.2	247.5	57	SC3	-1120.2	-267.5
28	SC33	1120.2	372.5	58	SC2	-1120.2	-392.5
29	SC34	1120.2	497.5	59	SC1	-1120.2	-517.5
30	SC29	1120.2	622.5				

PIN DESCRIPTION

<table>
<tr><th>Pin (No.)</th><th>I/O</th><th colspan="2">Name</th><th>Description</th><th>Interface</th></tr>
<tr><td>V_{DD}(24)</td><td rowspan="3">Power</td><td colspan="2" rowspan="2">Operating Voltage</td><td>For logical circuit (2.7 to 5.5V)</td><td rowspan="3">Power Supply</td></tr>
<tr><td>GND(34)</td><td>0V (GND)</td></tr>
<tr><td>V_{EE}(31)</td><td colspan="2">Negative Supply Voltage</td><td>For LCD driver circuit</td></tr>
<tr><td>V1, V2 (44,45)</td><td>I</td><td colspan="2">Bias Voltage</td><td>Bias voltage level for LCD drive (select level)</td><td>Power</td></tr>
<tr><td>SC1 to SC20</td><td>O</td><td rowspan="4">Part 1</td><td>LCD driver</td><td>LCD driver output</td><td>LCD</td></tr>
<tr><td>V3, V4
(46, 47)</td><td>I</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (non-select level)</td><td>Power</td></tr>
<tr><td>SHL1(41)</td><td>I</td><td>Data interface</td><td>Selection of the shift direction of Part 1 shift register
<table><tr><th>SHL1</th><th>DL1</th><th>DR1</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL1, DR1
(35, 36)</td><td>I/O</td><td>Data input/output of Part 1 shift register</td><td>Controller or S6A0065</td></tr>
<tr><td>SC21 to SC40</td><td>O</td><td rowspan="4">Part 2</td><td>LCD driver</td><td>LCD driver output</td><td></td></tr>
<tr><td>V5, V6
(48, 49)</td><td>I</td><td>Bias Voltage</td><td>Bias voltage level for LCD drive (non-select level)</td><td>Power</td></tr>
<tr><td>SHL2(42)</td><td>I</td><td>Data interface</td><td>Selection of the shift direction of Part 2 shift register
<table><tr><th>SHL2</th><th>DL2</th><th>DR2</th></tr><tr><td>V_{DD}</td><td>out</td><td>in</td></tr><tr><td>V_{SS}</td><td>in</td><td>out</td></tr></table></td><td>V_{DD} or V_{SS}</td></tr>
<tr><td>DL2,DR2
(37, 38)</td><td>I/O</td><td>Data input/output of Part 2 shift register</td><td>Controller or S6A0065</td></tr>
<tr><td>M (40)</td><td>I</td><td colspan="2">Alternated signal for LCD driver output</td><td rowspan="3"><table><tr><th>PART</th><th>FCS</th><th>CL1</th><th>CL2</th><th>M polartty</th></tr><tr><td rowspan="2">1</td><td>Vss</td><td rowspan="2">latch clock</td><td rowspan="2">shift clock</td><td rowspan="2">M</td></tr><tr><td>VDD</td></tr><tr><td rowspan="2">2</td><td>Vss</td></tr><tr><td>VDD</td><td>latch clock</td><td>shift clock</td><td>$\overline{M}$</td></tr></table>
Shift/latch clock of display data and polarity of M signal are changed by FCS signal.
By setting FCS to V_{DD} level, user can select the function that use Part 1 as segment driver and Part 2 as common driver simultaneously.</td><td rowspan="3">Controller</td></tr>
<tr><td>CL1,CL2
(32,33)</td><td>I</td><td colspan="2">Data shift /latch clock</td></tr>
<tr><td>FCS(43)</td><td>I</td><td colspan="2">Mode selection</td></tr>
<tr><td>NC(39)</td><td></td><td colspan="2"></td><td>No connection pin</td><td>NC</td></tr>
</table>

MAXIMUM ABSOLUTE LIMIT

(T_A = 25°C)

Characteristic	Symbol	Value	Unit
Operating Voltage	V_{DD}	- 0.3 to + 7.0	V
Driver Supply Voltage	V_{LCD}	V_{DD} - 15.0 to V_{DD} + 0.3	V
Input Voltage 1	V_{IN1}	- 0.3 to V_{DD} + 0.3	V
Input Voltage 2 (V1 - V6)	V_{IN2}	V_{DD} + 0.3 to V_{EE} - 0.3	V
Operating Temperature	T_{OPR}	- 30 to + 85	°C
Storage Temperature	T_{SRG}	- 55 to + 125	°C

*****Voltage greater than above may damage the circuit

***** V_{EE}: connect a protection resistor (220Ω ± 5%)

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 2.7 - 5.5V, V_{DD}-V_{EE} = 3 - 13V, V_{SS} = 0V, T_A = -30 - +85°C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Operating Current *	I_{DD}	f_{CL2} = 400kHz	–	1	mA	–
Supply Current *	I_{EE}	f_{CL1} = 1kHz	–	10	µA	
Input High Voltage	V_{IH}	–	0.7V_{DD}	V_{DD}	V	CL1, CL2, DL1, DL2
Input Low Voltage	V_{IL}		0	0.3V_{DD}		DR1, DR2, SHL1, SHL2
Input Leakage Current	I_{LKG}	V_{IN} = 0 – V_{DD}	-5	5	µA	M, FCS
Output High Voltage	V_{OH}	I_{OH} = -0.4mA	V_{DD}-0.4	–	V	DL1, DL2, DR1, DR2
Output Low Voltage	V_{OL}	I_{OL} = +0.4mA	–	0.4		
Voltage Descending	V_{D1}	I_{ON} = 0.1mA for one of SC1 – SC40	–	1.1		V(V1-V6)-SC(SC1-SC40)
	V_{D2}	I_{ON} = 0.05mA for each SC1 – SC40	–	1.5		
Leakage Current	I_V	V_{IN} = V_{DD} – V_{EE} (Output SC1-SC40 : floating)	-10	10	µA	V1-V6

AC Characteristics

(V_{DD} = 2.7 to 5.5V, V_{DD}-V_{EE} = 3 to 13V, V_{SS} = 0V, T_A = -30 to + 85 °C)

Characteristic	Symbol	Test condition	Min	Max	Unit	Applicable pin
Data Shift Frequency	f_{CL}	–	–	400	kHz	CL2
Clock High Level Width	t_{WCKH}	–	800	–	ns	CL1, CL2
Clock Low Level Width	t_{WCKL}	–	800	–		CL2
Clock Set-up Time	t_{SL}	from CL2 to CL1	500	–		CL1, CL2
	t_{LS}	from CL1 to CL2	500	–		
Clock Rise/Fall Time	t_R/t_F	–	–	200		
Data Set-up Time	t_{SU}	–	300	–		DL1, DL2, DR1,
Data Hold Time	t_{DH}	–	300	–		DR2, FLM
Data Delay Time	t_D	C_L = 15pF	–	500		DL1, DL2, DR1, DR2

NOTE: Input/Output current is excluded; When input is at the intermediate level with CMOS, excessive current flows through the input circuit to the power supply, To avoid this, input level must be fixed at "H" or "L".

TIMING CHARACTERISTICS

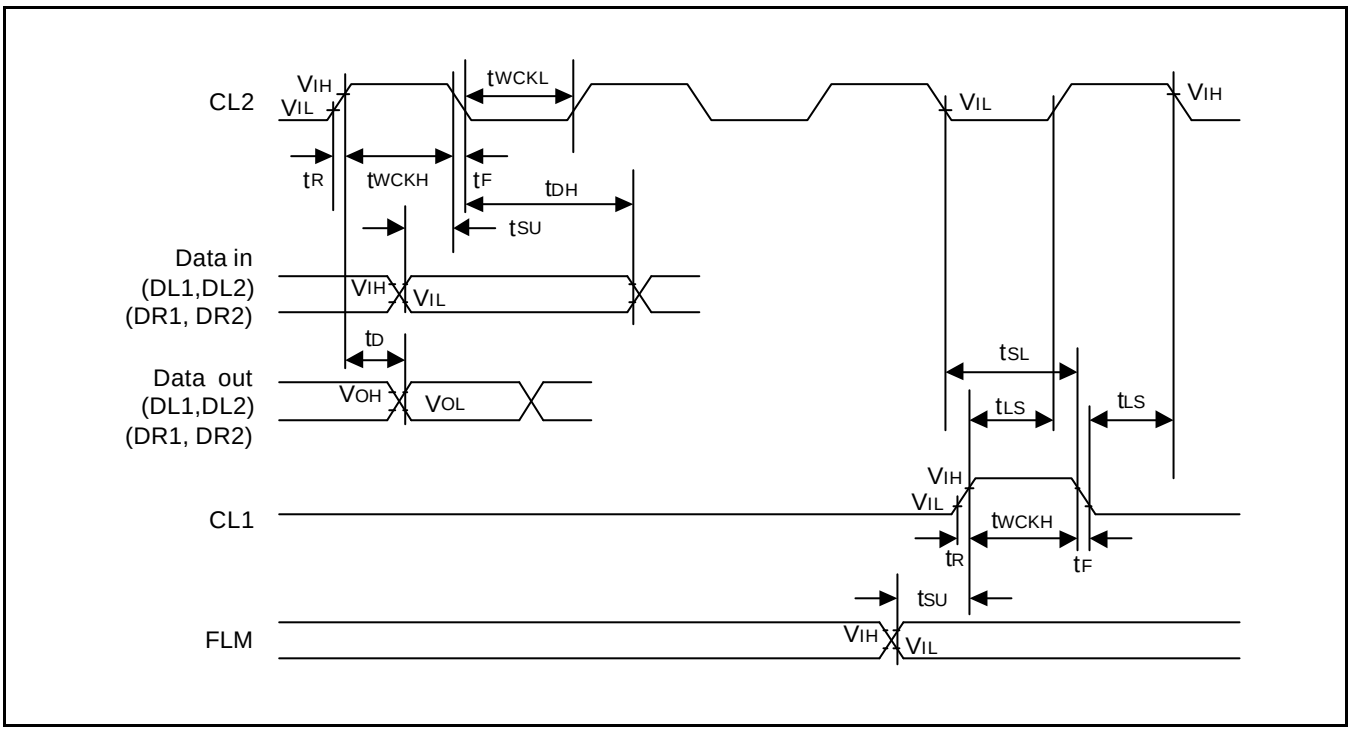


Figure 3. AC characteristics

FUNCTIONAL DESCRIPTION

1) To Drive Segment Type

When the FCS is connected to V_{SS}, S6A0065 (SC1-SC40) is operated as segment driver (refer to Figure 4).

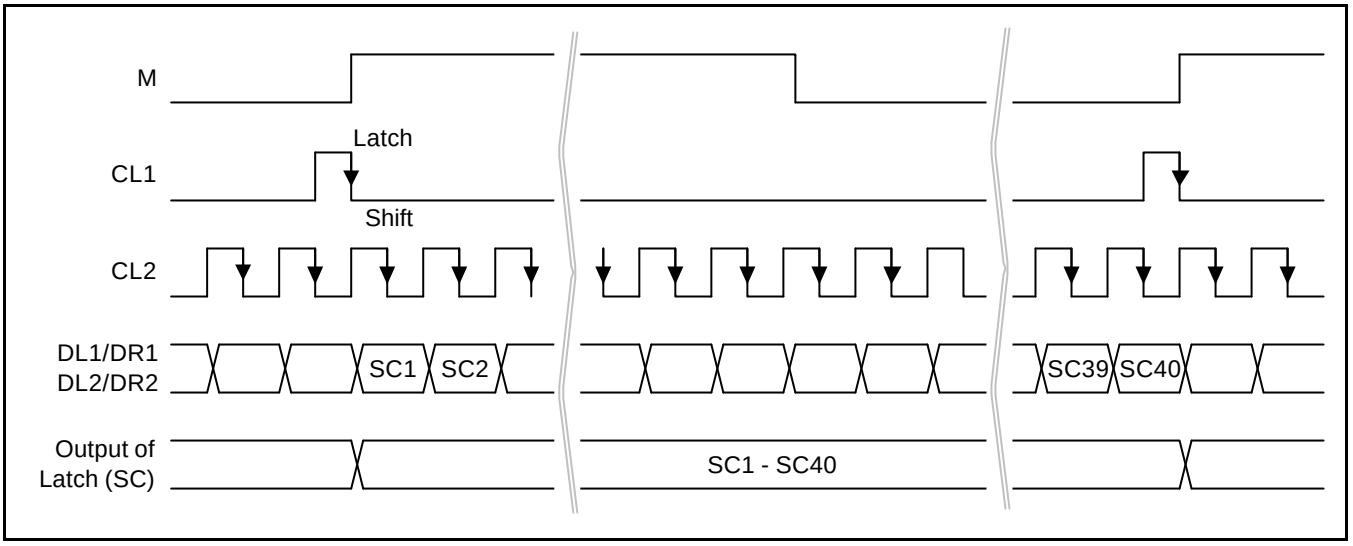


Figure 4. Segment Data Waveform

2) To Drive Common Type

When the FCS is connected to V_{DD}, only part2 (SC21-SC40) of S6A0065 is operated as common driver (refer to Figure 5).

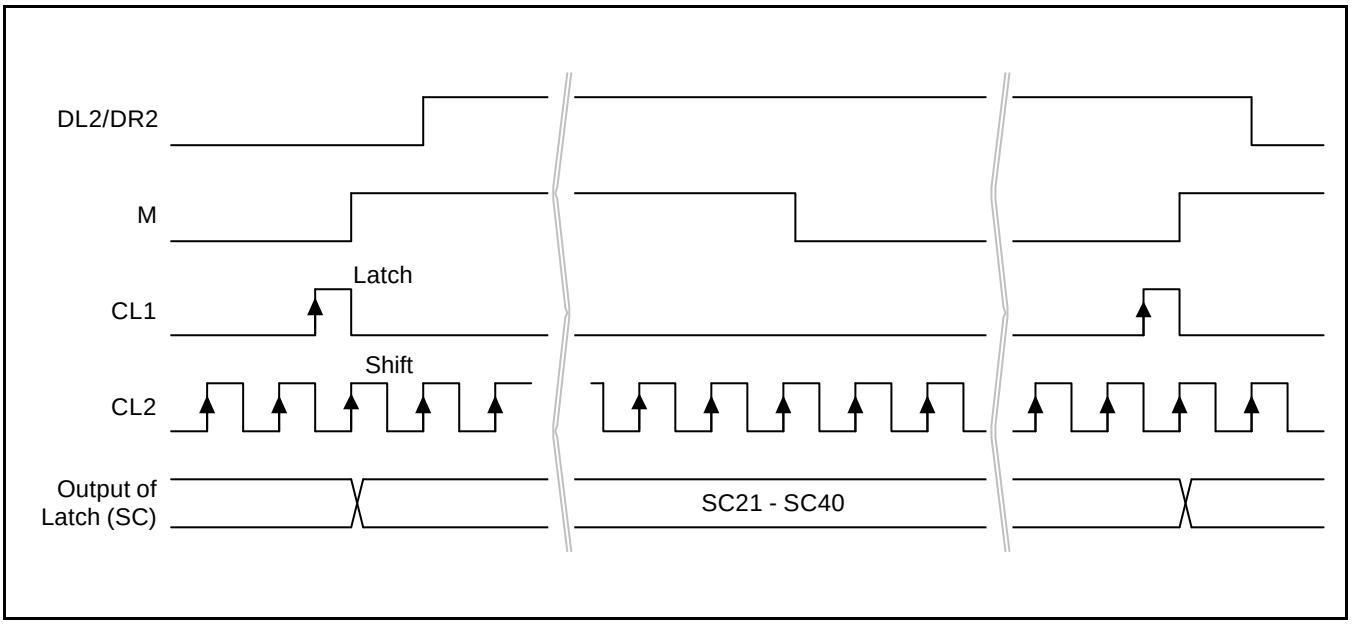


Figure 5. Common Data Waveforms

LCD OUTPUT WAVEFORMS

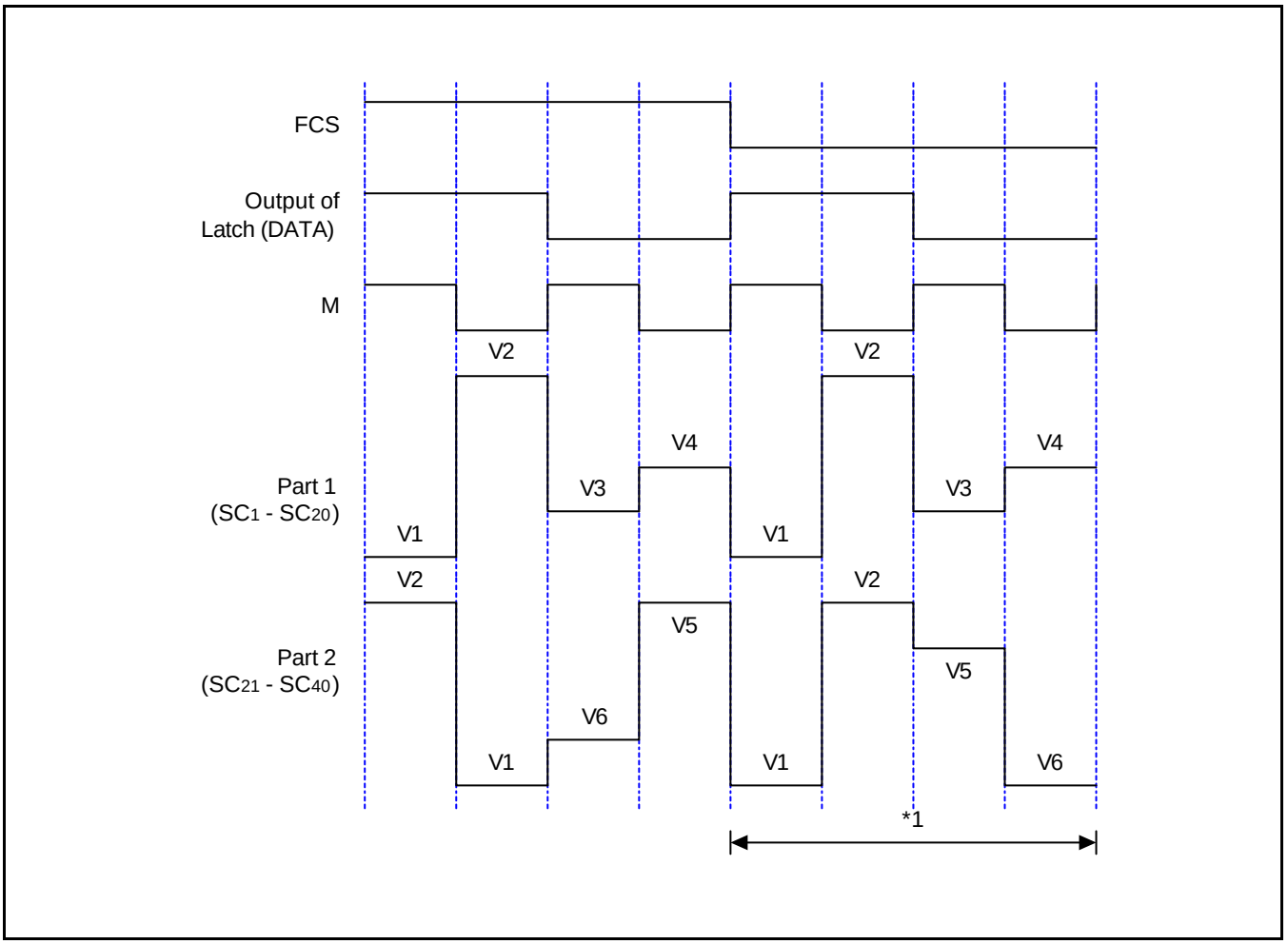
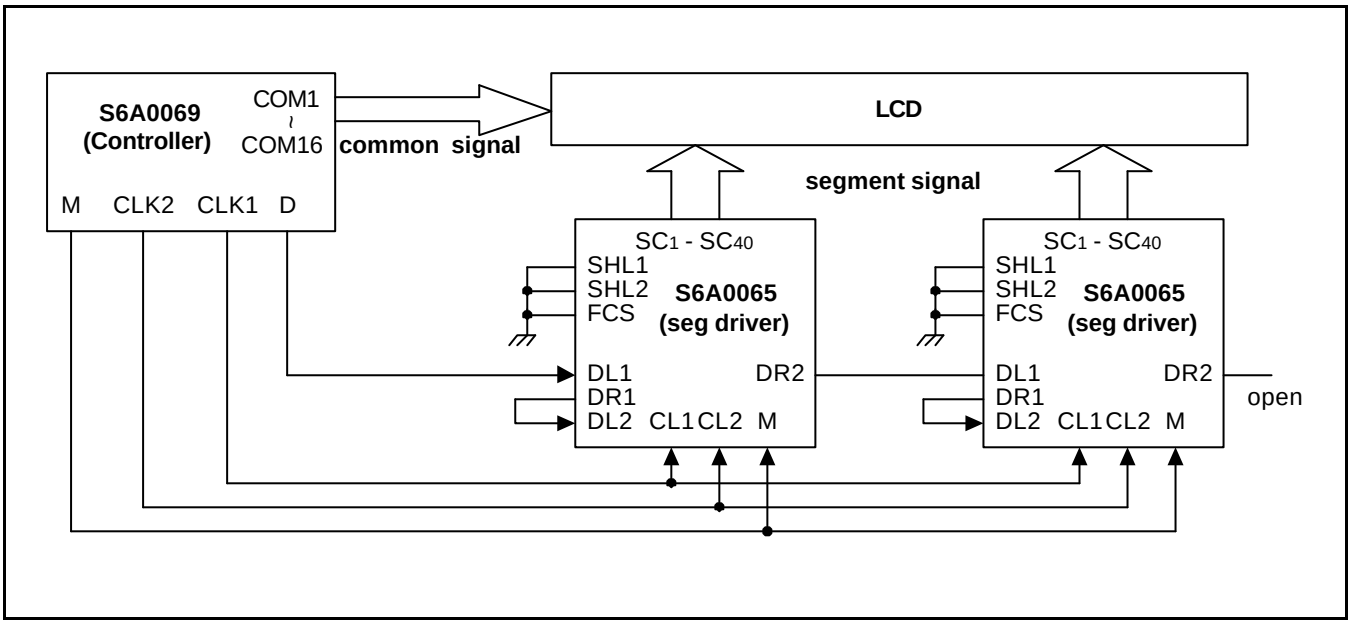


Figure 6. Output Waveforms

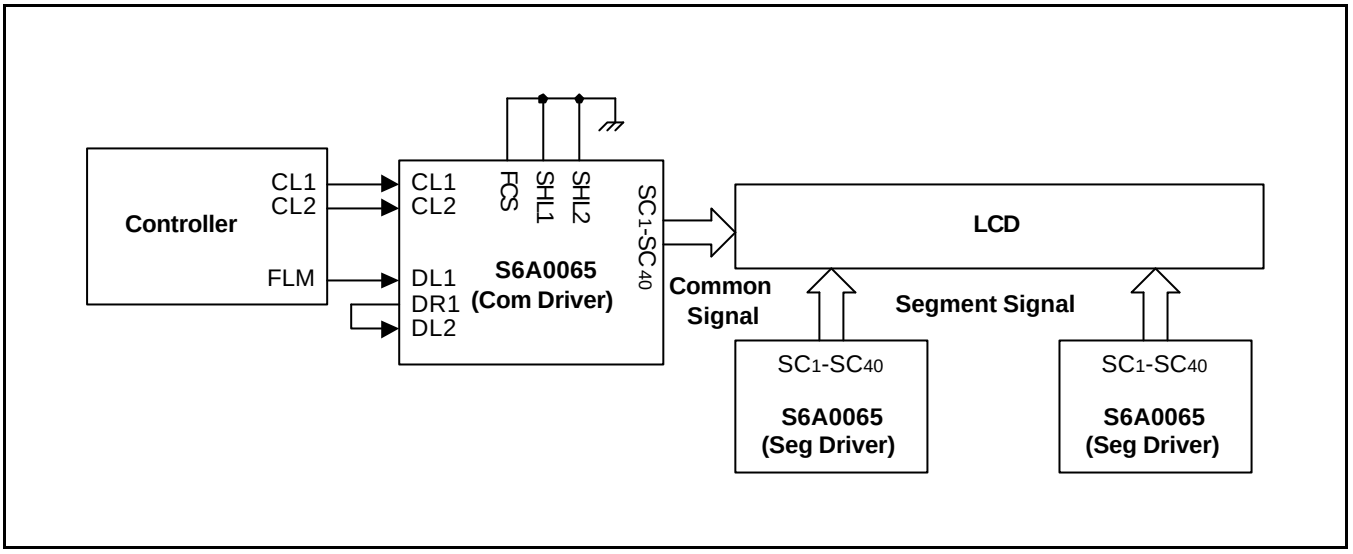
NOTE: To use for same function of part 1 and part 2, V3 and V5, V4 and V6 of power supply for LCD drive are short circuited respectively.

APPLICATION CIRCUIT

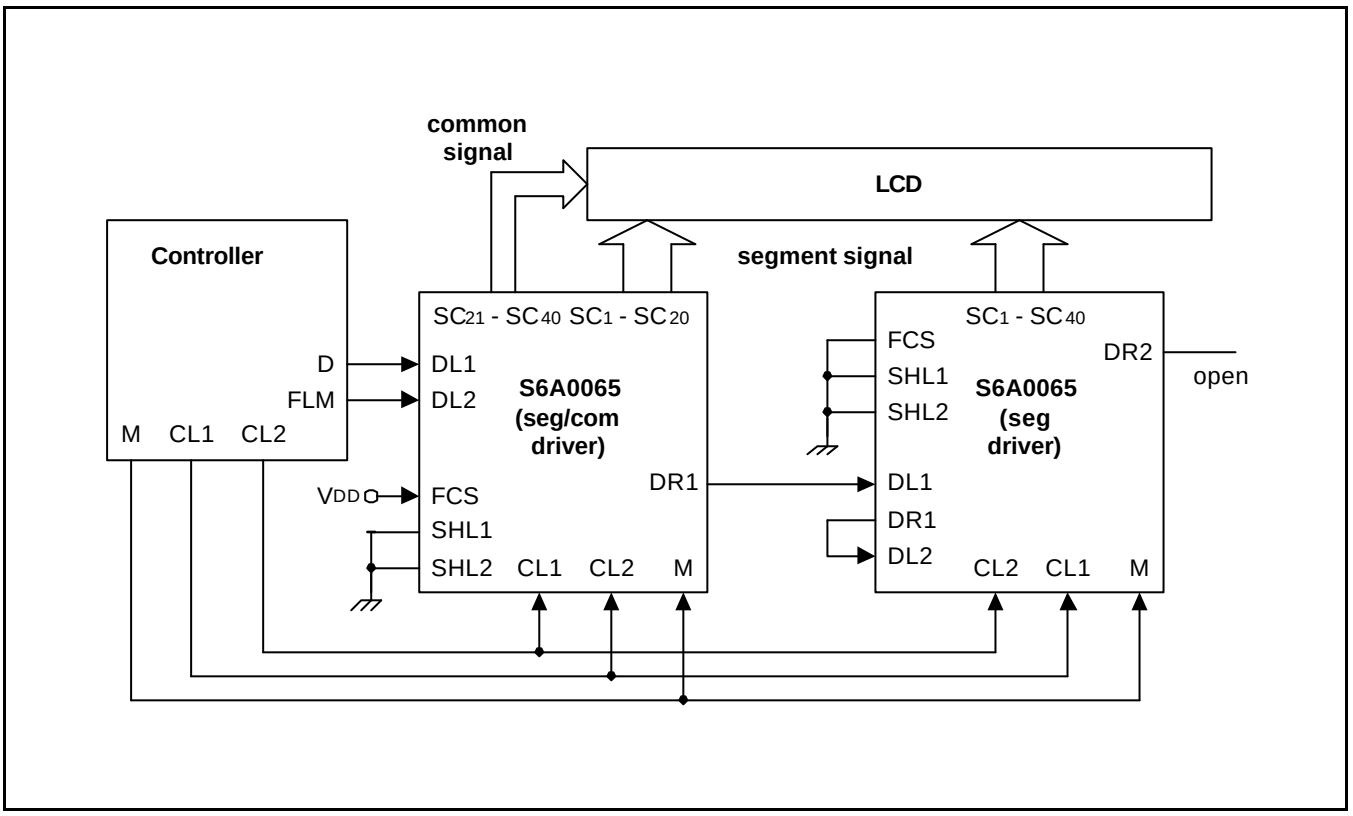
1) Segment Driver



2) Common Driver



3) Segment/Common Driver



NOTES