19-1215; Rev 1; 4/98

MAXIM

155Mbps Preamplifier for FDDI and ATM LAN Fiber Optic Receivers

General Description

The MAX3963 is a low-noise transimpedance preamplifier for FDDI and 155Mbps ATM optical receivers. The MAX3963's dynamic range is optimized for use in multimode LED-based applications.

The preamplifier converts a small photodiode current to a differential voltage, with typical transimpedance of 22kΩ. Input-referred noise of only 21nA allows detection of signals as small as 267nA, while pulse-width distortion is only 85ps with a 60µA input signal. In a 1300nm multimode receiver, with responsivity of 0.7A/W, the MAX3963's dynamic range spans from -36dBm to -13.7dBm. The circuit operates from a single +5V supply, and typically consumes only 60mW power.

The MAX3963 die includes a filter connection, which provides positive bias for the photodiode through a 1kΩ resistor to V_{CC}. This feature, combined with the small die size, allows the MAX3963 to fit easily into a TO-style package with a photodiode.

The differential outputs are back terminated with 60Ω per side, allowing the easy use of filters to improve sensitivity.

The MAX3963 is designed to be used with the MAX3964 limiting amplifier IC. It is available in an 8-pin SO package and as dice.

Applications

FDDI

155Mbps ATM

Features

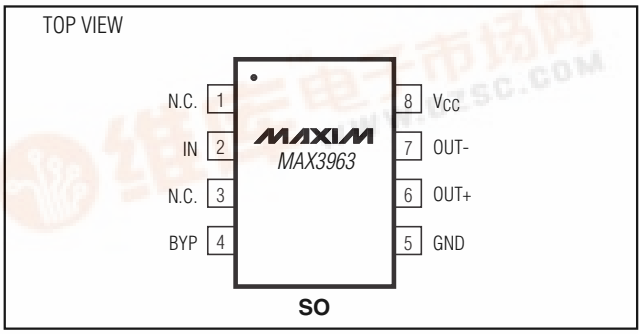
- ♦ 21nA Total RMS Noise
- ♦ 22kΩ Differential Transimpedance
- ♦ 180MHz Bandwidth
- ♦ 60mW Typical Power Consumption
- ♦ 60µA Peak Input Current
- ♦ Low, 85ps Pulse-Width Distortion

Ordering Information

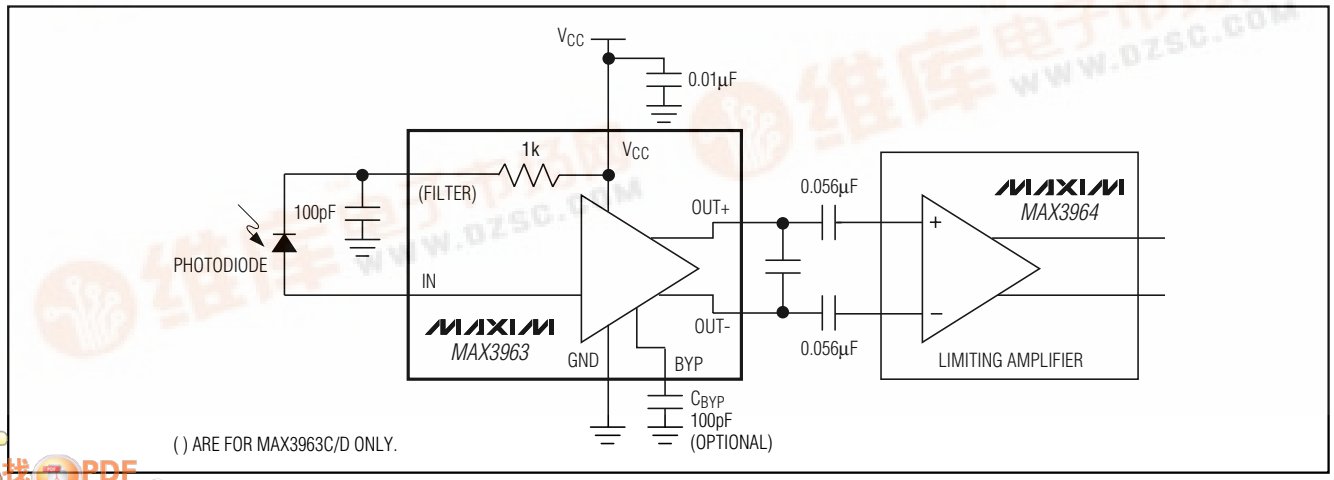
PART	TEMP. RANGE	PIN-PACKAGE
MAX3963CSA	0°C to +70°C	8 SO
MAX3963C/D	0°C to +70°C*	Dice

**Dice are designed to operate over a 0°C to +100°C junction temperature (T_J) range, but are tested and guaranteed at T_A = +25°C.*

Pin Configuration



Typical Application Circuit



155Mbps Preamplifier for FDDI and ATM LAN Fiber Optic Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....-0.5V to +7.0V
Continuous Current
IN.....5mA
OUT+, OUT-.....25mA
BYP 5mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C).....471mW

Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C
Operating Junction Temperature (die) .....-55°C to +150°C
Processing Temperature (die) .....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, C_{BYP} = 100pF, 1kΩ load between OUT+ and OUT-, T_A = 0°C to +70°C. Typical values are at V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Voltage	V_{IN}	Input = 0µA to 60µA		1.6	1.8	V
Supply Current	I_{CC}	Input = 0µA		12	20	mA
Small-Signal Transimpedance	z_{21}	Differential output, input < 60µA	17.5	22	26.3	kΩ
Output Common-Mode Voltage				V_{CC} - 2.85		V
Power-Supply Rejection Ratio	PSRR	f < 1MHz, referred to output	35			dB
Output Resistance (per side)	R_{OUT}		45	60	68	Ω
Maximum Differential Output Voltage	V_{OD} (MAX)	I_{IN} = 80µA			2.2	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, C_{BYP} = 100pF, C_{IN} = 1.15pF, T_A = +25°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Small-Signal Bandwidth	BW_{-3dB}	C_{OUT} = 5pF	100	180	220	MHz
Pulse-Width Distortion	PWD	I_{IN} = 60µAp-p (Note 4)		85	160	ps
RMS Noise Referred to Input	i_n	(Note 5)		21	24.5	nA
		(Note 6)		37		nA

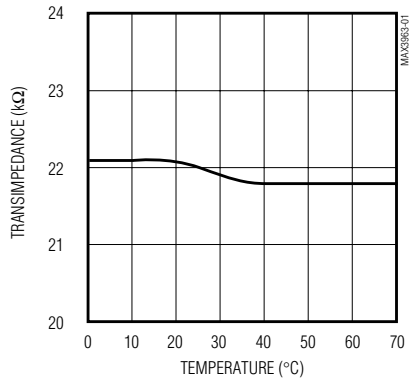
Note 1: Dice are tested at T_A = +25°C only.
Note 2: AC characteristics are guaranteed by design.
Note 3: C_{IN} is the total capacitance at IN. C_{OUT} is the differential output capacitive load.
Note 4: PWD = [(width of wider pulse) - (width of narrower pulse)] / 2. Input is a 155Mbps 1-0 pattern, with rise time approximately 2ns.
Note 5: Measured with a 117MHz, 3-pole Bessel filter.
Note 6: Measured with C_{OUT} = 5pF, T_A = +25°C.

155Mbps Preamplifier for FDDI and ATM LAN Fiber Optic Receivers

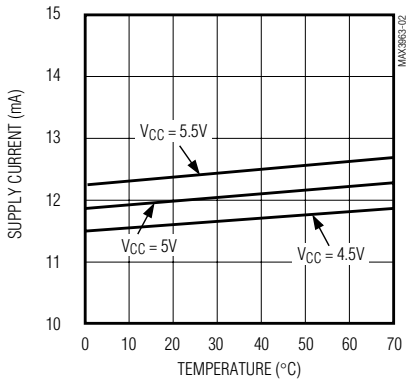
Typical Operating Characteristics

(V_{CC} = 5.0V, C_{BYP} = 100pF, C_{IN} = 1.3pF, T_A = +25°C, unless otherwise noted.)

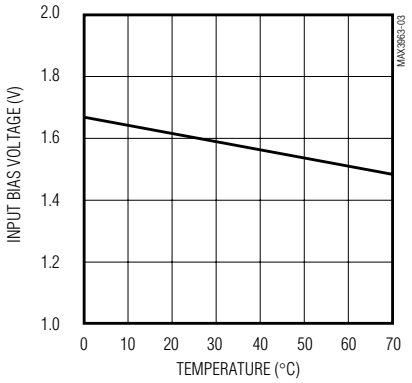
SMALL-SIGNAL TRANSIMPEDANCE vs. TEMPERATURE



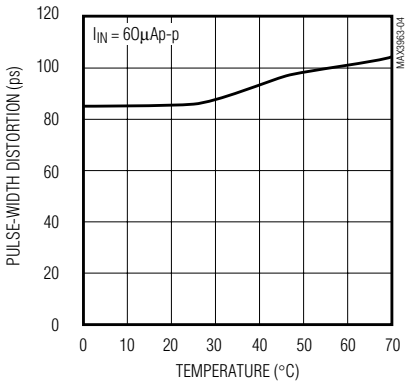
SUPPLY CURRENT vs. TEMPERATURE



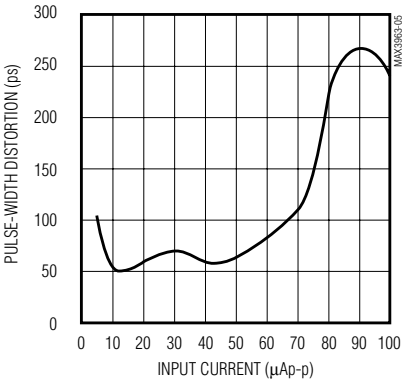
INPUT BIAS VOLTAGE (V_{IN}) vs. TEMPERATURE



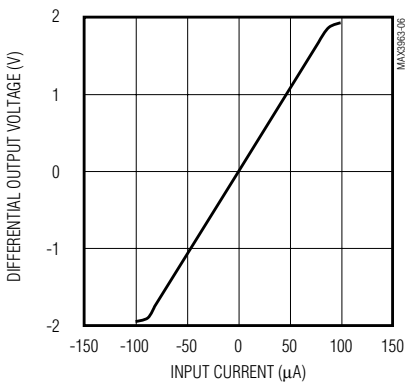
PULSE-WIDTH DISTORTION vs. TEMPERATURE



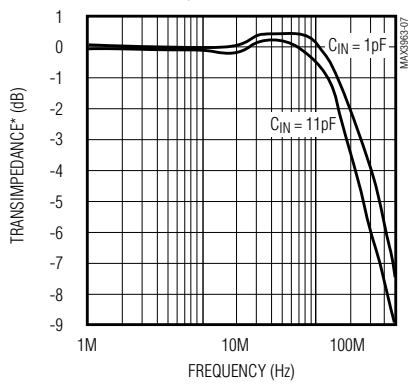
PULSE-WIDTH DISTORTION vs. INPUT CURRENT



DIFFERENTIAL OUTPUT VOLTAGE vs. INPUT CURRENT

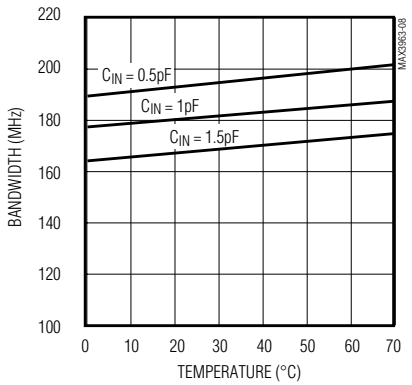


FREQUENCY RESPONSE

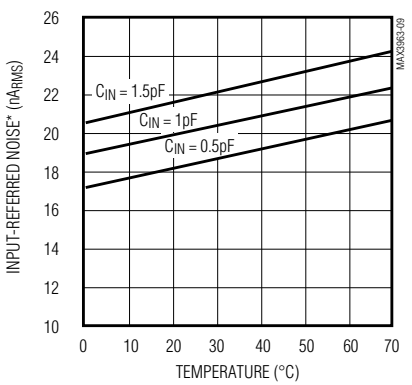


**RELATIVE TO TRANSIMPEDANCE AT DC*

BANDWIDTH vs. TEMPERATURE



INPUT-REFERRED RMS NOISE



**MEASURED WITH 4-POLE, 117MHz BESSEL FILTER*

155Mbps Preamplifier for FDDI and ATM LAN Fiber Optic Receivers

Pin Description

PIN	NAME	FUNCTION
1, 3	N.C.	No Connect. No internal connection to the die.
2	IN	Signal Input
4	BYP	Connection for optional noise-reducing capacitor
5	GND	Signal Ground
6	OUT+	Noninverting Voltage Output. Current flowing into IN causes V_{OUT+} to increase.
7	OUT-	Inverting Voltage Output. Current flowing into IN causes V_{OUT-} to decrease.
8	V_{CC}	Supply Voltage
—	FILTER*	Connection for 1kΩ filter resistor. This pad is accessible on the die only.

**MAX3963C/D (die) only.*

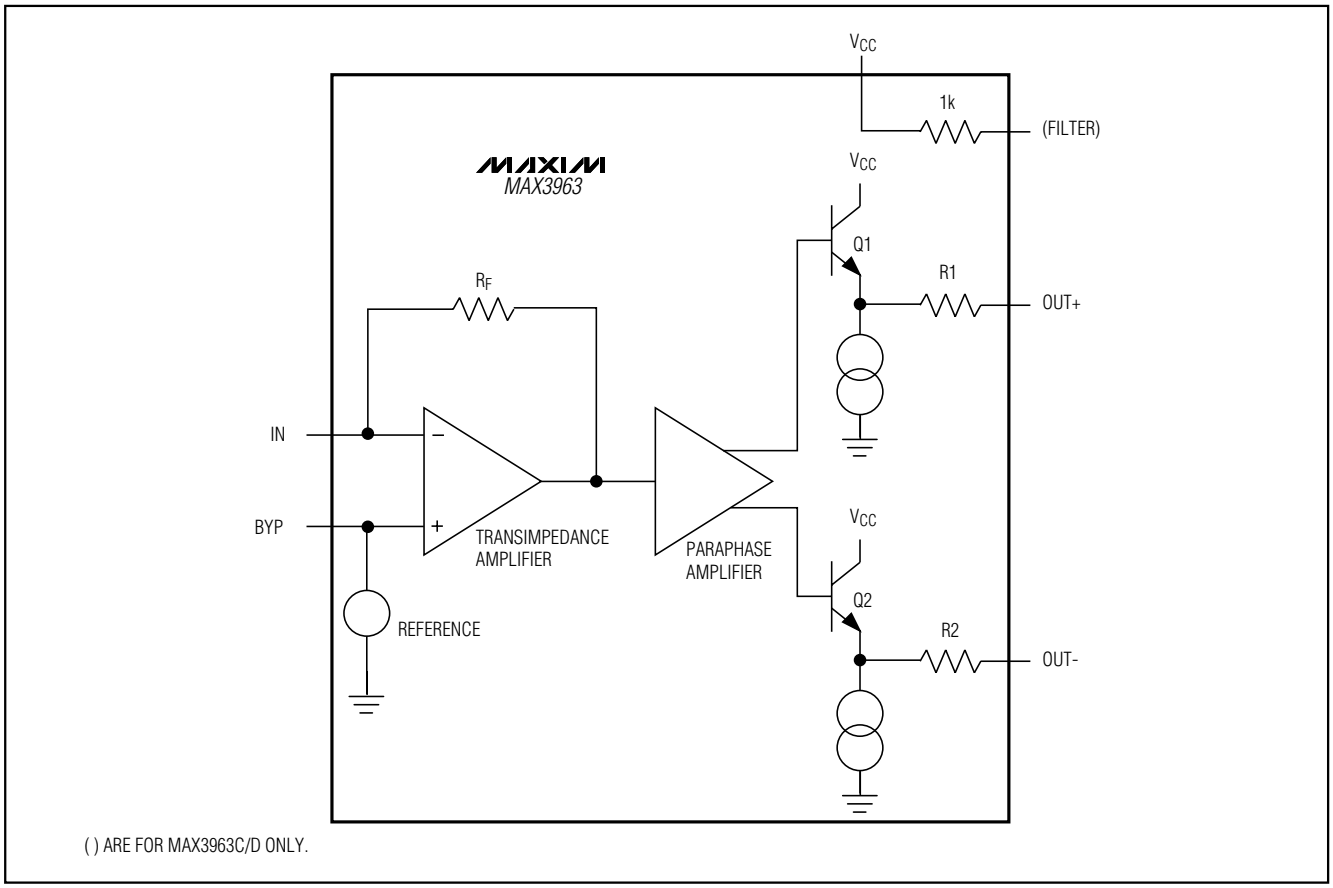


Figure 1. Functional Diagram

155Mbps Preamplifier for FDDI and ATM LAN Fiber Optic Receivers

Detailed Description

The MAX3963 transimpedance amplifier is designed for 155Mbps fiber optic applications. Figure 1 is a functional diagram of the MAX3963, which comprises a transimpedance amplifier and a paraphase amplifier with emitter-follower outputs.

Transimpedance Amplifier

The signal current at the input flows into the summing node of a high-gain amplifier. Shunt feedback through R_F converts this current to a voltage with a 10kΩ gain.

Paraphase Amplifier

The paraphase amplifier converts single-ended signals to differential signals and introduces a 2x voltage gain. This signal drives a pair of internally biased emitter followers, Q1 and Q2, which form the output stage. Resistors R1 and R2 provide back termination at the output, providing a 120Ω differential output impedance.

The output emitter followers are designed to drive a 1kΩ differential load between OUT+ and OUT-. Higher output impedances can also be driven, resulting in slightly increased gain and output voltage swing. The MAX3963 will not drive a 50Ω grounded load. The MAX3963 outputs may be AC coupled to a limiting amplifier.

Applications Information

Optical-Power Relations

Many of the MAX3963 specifications relate to the input signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. The relations shown in Table 1 are helpful for converting optical power to input signal when designing with the MAX3963. These relations are true if the average data duty cycle is 50%.

Calculating Sensitivity and Overload

Sensitivity Calculation

The MAX3963's input-referred RMS noise current (i_n) generally dominates receiver sensitivity. In a system where the bit error rate is 1E-10, the signal-to-noise ratio must always exceed 12.7. The sensitivity, expressed in average power, can be estimated as shown in the following equation:

$$\text{Sensitivity} = 10\log\left(\frac{12.7\, i_n\,(re + 1)}{2\rho\,(re - 1)} \times 1000\right)\text{dBm}$$

where ρ is the photodiode responsivity in A/W.

Input Overload

The overload is the largest input that the MAX3963 accepts while meeting specifications. A larger input causes increased pulse-width distortion.

$$\text{Overload} = 10\log\left(\frac{60\mu A}{2\rho} \times 1000\right)\text{dBm}$$

Table 1. Optical-Power Relations*

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVE}	$P_{AVE} = (P0 + P1) / 2$
Extinction Ratio	r_e	$r_e = P1 / P0$
Optical Power of a "1"	P1	$P1 = 2P_{AVE}\,(r_e) / (r_e + 1)$
Optical Power of a "0"	P0	$P0 = 2P_{AVE} / (r_e + 1)$
Signal Amplitude	P_{INPUT}	$P_{INPUT} = P1 - P0 = 2P_{AVE}\,(r_e - 1) / (r_e + 1)$

**Assuming 50% average data duty cycle*

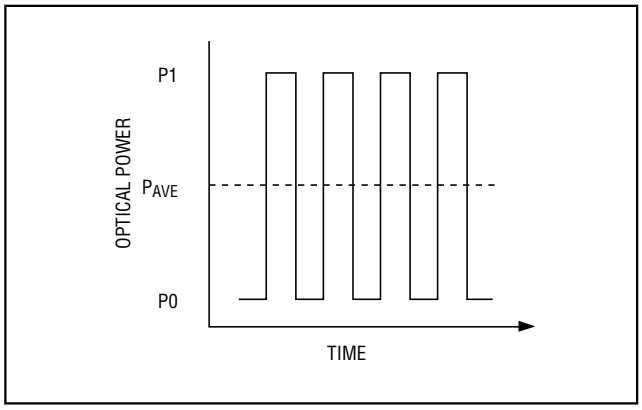


Figure 2. Optical-Power Definitions

155Mbps Preamplifier for FDDI and ATM LAN Fiber Optic Receivers

Output Filter

The MAX3963's noise can be reduced by filtering the output signal. For digital communications systems, a linear-phase filter with -3dB lowpass response of (0.7 x data rate) is recommended.

A single-pole filter implemented with a capacitor across the outputs also reduces noise, and consumes less board space than a linear-phase filter. The following equation represents the filter frequency:

$$f_{-3dB} = \frac{1}{2\pi\ R_{OUT}\ C_{OUT}}$$

where R_{OUT} is the MAX3963 differential output resistance (typically 120Ω), and C_{OUT} is the differential output load capacitance. For 155Mbps receivers, an 11pF capacitor is recommended.

Layout Considerations

Use good high-frequency design and layout techniques. The use of a multilayer circuit board with separate ground and V_{CC} planes is recommended. Bypass V_{CC} and connect the GND pin to the ground plane with traces kept as short as possible. Ensure that common-mode output capacitance is less than 2pF per output.

Low-Capacitance Input Design Considerations

Noise performance and bandwidth are adversely affected by stray capacitance on the input node. Every effort must be made to minimize capacitance on this pin. Select a low-capacitance photodiode, and use good high-frequency design and layout techniques. The MAX3963 is optimized for 1.0pF of capacitance on the input, approximately the capacitance of a photodetector diode packaged in a header.

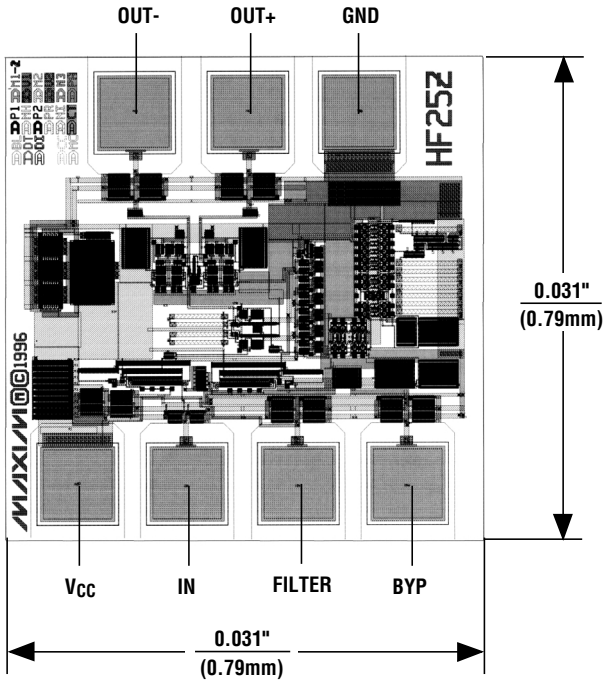
When using the SO package version of the MAX3963, the package capacitance is about 0.3pF. This means that great care must be used to reduce input capacitance. The PC board between the MAX3963 input and the photodiode can add parasitic capacitance. Keep the input line short, and remove power and ground planes beneath it.

Assembling the MAX3963 in die form provides the best possible performance. Parasitic capacitance can be reduced to a minimum, resulting in the lowest noise and the best bandwidth.

Wire Bonding

For high current density and reliable operation, the MAX3963 uses gold metalization. Make connections to the die with gold wire only, using ball-bonding techniques. Wedge bonding is not recommended. Die-pad size is 4mils square, with 6mil pitch. Die thickness is 15mils.

Chip Topography



TRANSISTOR COUNT: 116

SUBSTRATE CONNECTED TO GND