

7500-pixel CCD Linear Sensor (B/W)

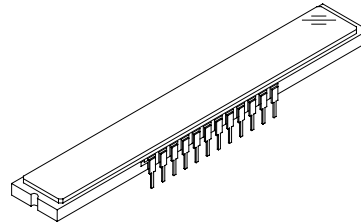
Description

The ILX512 is a reduction type CCD linear sensor developed for high resolution copiers. This sensor reads A3-size documents at a density of 600 DPI at high speed.

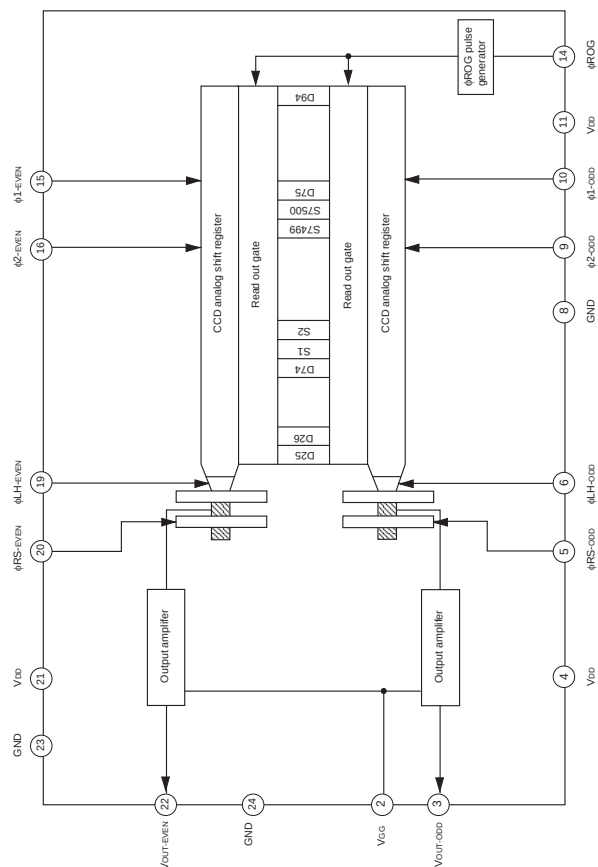
Features

- Number of effective pixels: 7500 pixels
- Pixel size: $7\ \mu\text{m} \times 7\ \mu\text{m}$ ($7\ \mu\text{m}$ pitch)
- Signal output phase of two-output:
Simultaneous output
(Alternate output is available)
- Ultra-high sensitivity and ultra-low lag
- Max data rate: 40 MHz
- Single 12 V power supply
- Input clock pulse: CMOS 5 V drive
- Package: 24-pin DIP (400 mil)

24 pin DIP (400mil)



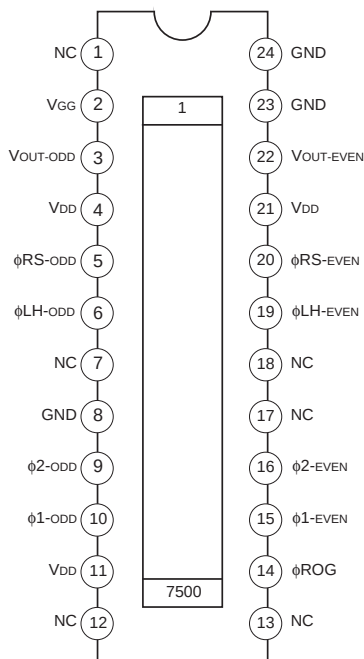
Block Diagram



Absolute Maximum Ratings

- Supply voltage VDD 15 V
- Operating temperature -10 to $+60$ $^{\circ}\text{C}$
- Storage temperature -30 to $+80$ $^{\circ}\text{C}$

Pin Configuration (TOP VIEW)



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Pin Description

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	NC	13	NC	NC
2	V _{GG}	Output circuit gate bias	14	φROG	Readout gate clock pulse input
3	V _{OUT-ODD}	Signal out (odd pixel)	15	φ1-EVEN	Clock pulse input (even pixel)
4	V _{DD}	12 V power supply	16	φ2-EVEN	Clock pulse input (even pixel)
5	φRS-ODD	Clock pulse input (odd pixel)	17	NC	NC
6	φLH-ODD	Clock pulse input (odd pixel)	18	NC	NC
7	NC	NC	19	φLH-EVEN	Clock pulse input (even pixel)
8	GND	GND	20	φRS-EVEN	Clock pulse input (even pixel)
9	φ2-ODD	Clock pulse input (odd pixel)	21	V _{DD}	12 V power supply
10	φ1-ODD	Clock pulse input (odd pixel)	22	V _{OUT-EVEN}	Signal out (even pixel)
11	V _{DD}	12 V power supply	23	GND	GND
12	NC	NC	24	GND	GND

Recommended Supply Voltage

Item	Min.	Typ.	Max.	Unit
V _{DD}	11.4	12	12.6	V

Clock Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of f1*, f2*	Cf1, Cf2	—	500	—	pF
Input capacity of fLH*	CfLH	—	10	—	pF
Input capacity of fRS*	CfRS	—	10	—	pF
Input capacity of fROG	CfROG	—	10	—	pF

*It indicates that φ1-ODD, φ1-EVEN as φ1, φ2-ODD, φ2-EVEN as φ2, φLH-ODD, φLH-EVEN as φLH, φRS-ODD, φRS-EVEN as φRS.

Clock Frequency

Item	Symbol	Min.	Typ.	Max.	Unit
φ1, φ2, φLH, φRS	fφ1, fφ2, fφLH, fφRS	—	1	20	MHz
Data rate	fφR	—	2	40	MHz

Input Clock Pulse Voltage Condition

Item		Min.	Typ.	Max.	Unit
φ1, φ2, φLH, φRS, φROG pulse voltage	High level	4.75	5.0	5.25	V
	Low level	—	0	0.1	V

Electrooptical Characteristics (Note 1)(Ta = 25 °B, V_{DD} = 12 V, Data rate f_{DR}=2 MHz, Simultaneous output, Input clock =5 Vp-p

Light source = 3200 K, IR cut filter CM-500S (t = 1.0 mm))

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	9	12	15	V/(lx·s)	Note2
Sensitivity 2	R2	—	27.4	—	V/(lx·s)	Note3
Sensitivity nonuniformity	PRNU	—	4	10	%	Note4
Saturation output voltage	V _{SAT}	1.0	1.5	—	V	Note5
Saturation exposure	SE	0.067	0.125	—	lx·s	Note6
Register imbalance	RI	—	2	7	%	Note7
Dark voltage average	V _{DRK}	—	0.3	2.0	mV	Note8
Dark signal nonuniformity	DSNU	—	0.6	5.0	mV	Note9
Image lag	IL	—	0.02	—	%	Note10
Supply current	I _{VDD}	—	30	60	mA	—
Total transfer efficiency	TTE	92	98	—	%	—
Output impedance	Z _o	—	150	—	Ω	—
Offset level	V _{OS}	—	6.5	—	V	Note11
Dynamic range	DR	500	5000	—	—	Note12

Note

- 1) In accordance with the given electrooptical characteristics, the even black level is defined as the average value of D6, D8 to D24. The odd black level is defined as the average value of D5, D7 to D23.
- 2) For the sensitivity test, light is applied with a uniform intensity of illumination.
- 3) W lamp (2854K).
- 4) PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 2.
V_{OUT}=500mV (Typ.)

$$\text{PRNU} = \frac{(V_{\text{MAX}} - V_{\text{MIN}})/2}{V_{\text{AVE}}} \times 100 (\%)$$

Where the 7500 pixels are divided into blocks of 110 (the last block is 120), even and odd pixels, respectively. The maximum output of each block is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

- 5) Use below the minimum value of the saturation output voltage.

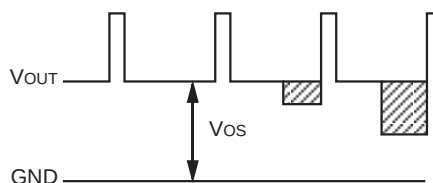
- 6) Saturation exposure is defined as follows. $\text{SE} = \frac{V_{\text{SAT}}}{R1}$

- 7) RI is defined as indicated below. V_{OUT}=500 mV (Typ.)

$$\text{RI} = \left(\frac{|V_{\text{ODD-AVE}} - V_{\text{EVEN-AVE}}|}{\frac{V_{\text{ODD-AVE}} + V_{\text{EVEN-AVE}}}{2}} \right) \times 100 (\%)$$

Where average of odd pixels output is set to V_{ODD-AVE}, even pixels to V_{EVEN-AVE}.

- 8) Optical signal accumulated time τ_{int} stands at 10 ms.
- 9) The difference between the maximum and average values of the dark output voltage is calculated for even and odd respectively. The larger value is defined as the dark signal nonuniformity. Optical signal accumulated time τ_{int} stands at 10 ms.
- 10) $V_{OUT} = 500 \text{ mV}$ (Typ.)
- 11) V_{os} is defined as indicated bellow.

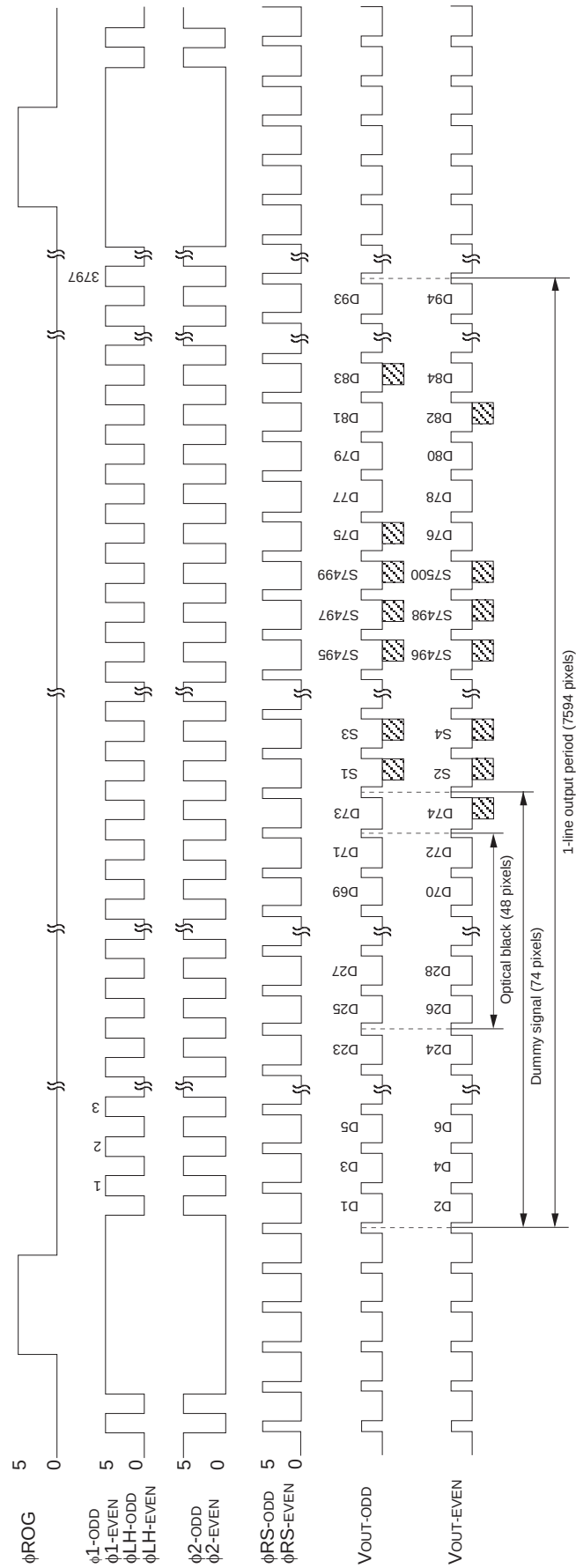


- 12) Dynamic range is defined as follows.

$$DR = \frac{V_{SAT}}{V_{DRK}}$$

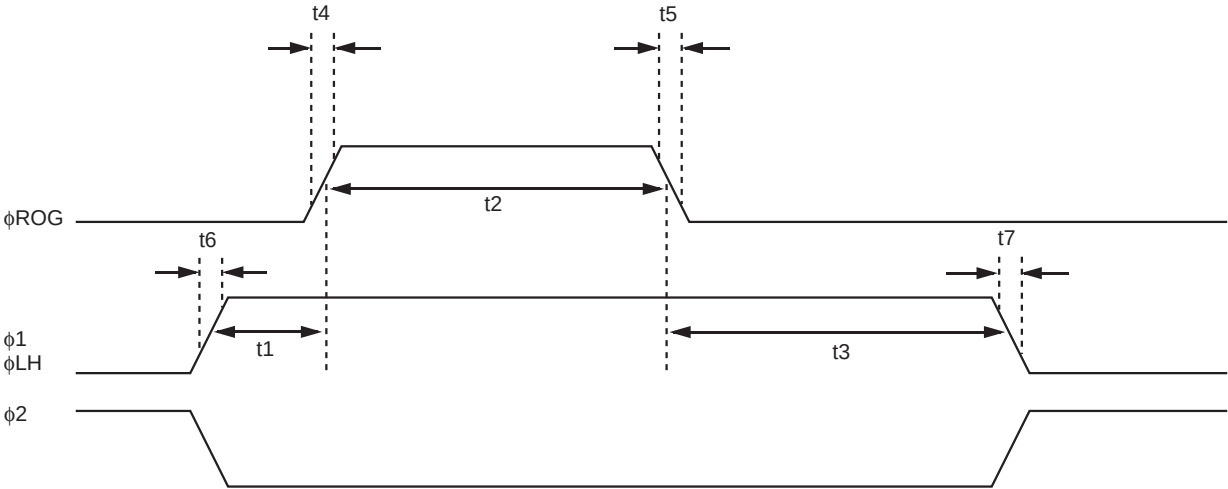
When the optical signal accumulated time is shorter, the dynamic range gets wider because the optical signal accumulated time is in proportion to the dark voltage.

Clock Timing Chart 1 (simultaneous output)

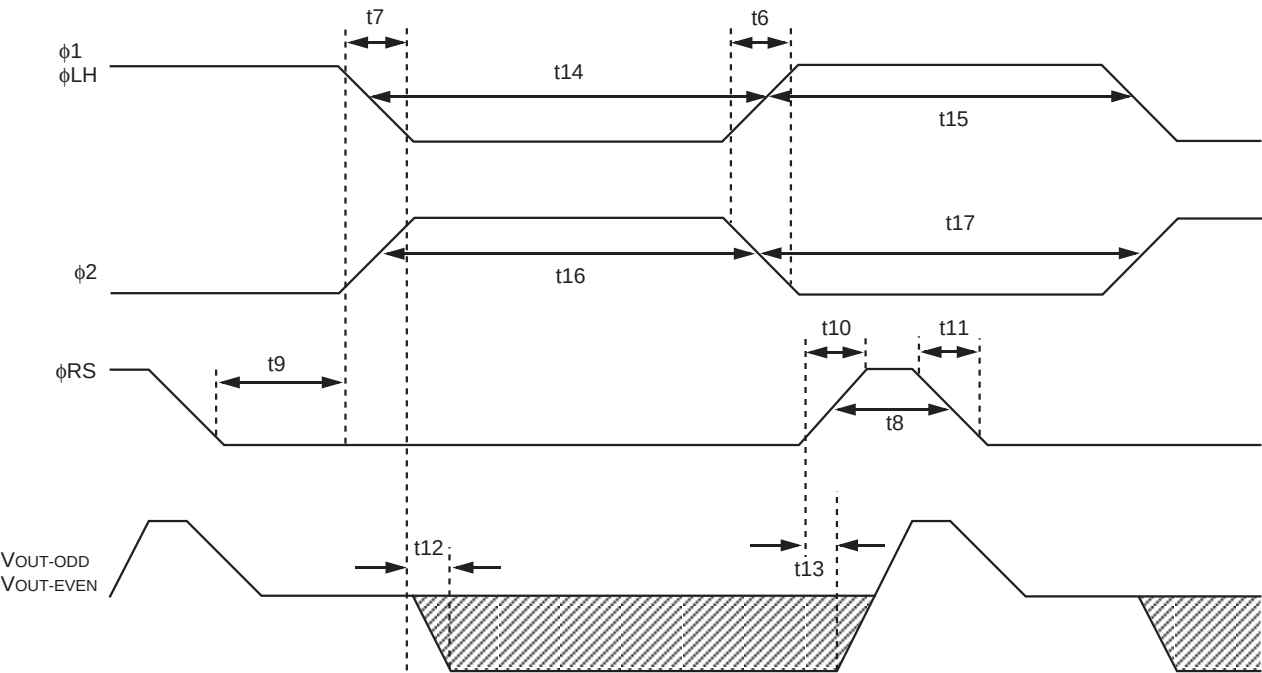


Note) The transfer pulses (ϕ 1, ϕ 2, ϕ LH) must have more than 3797 cycles.

Clock Timing Chart 2



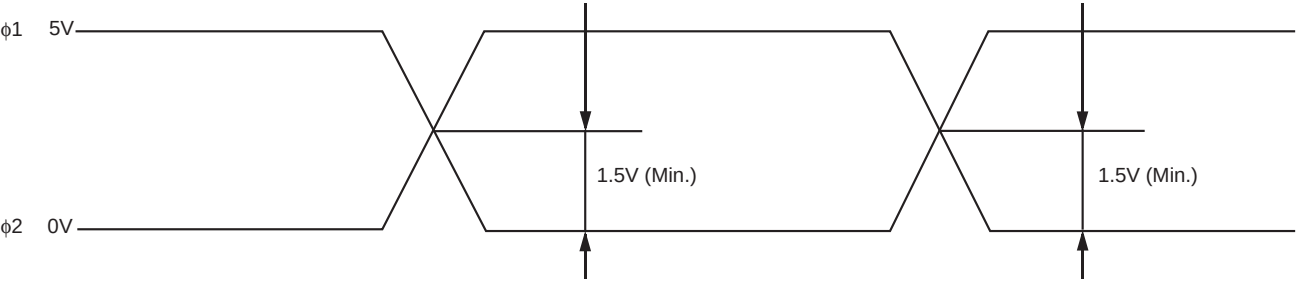
Clock Timing Chart 3



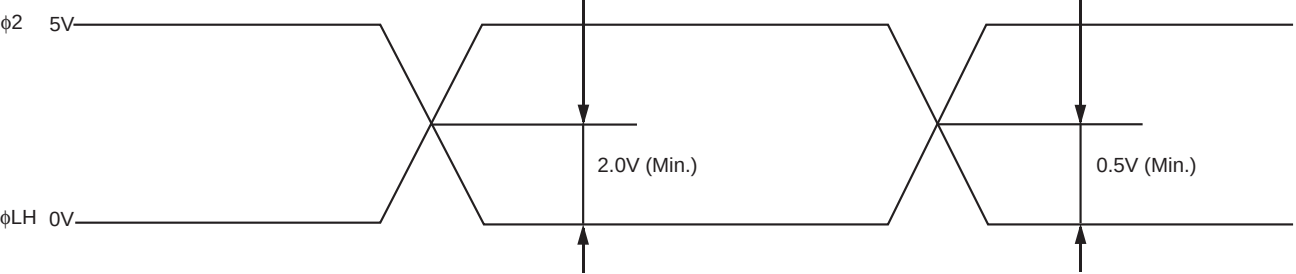
Clock timing of ϕ_1 , ϕ_2 , ϕ_{LH} , ϕ_{RS} , and V_{OUT} at odd or even are the same as timing chart 3 in the case of alternate output.

Clock Timing Chart 4

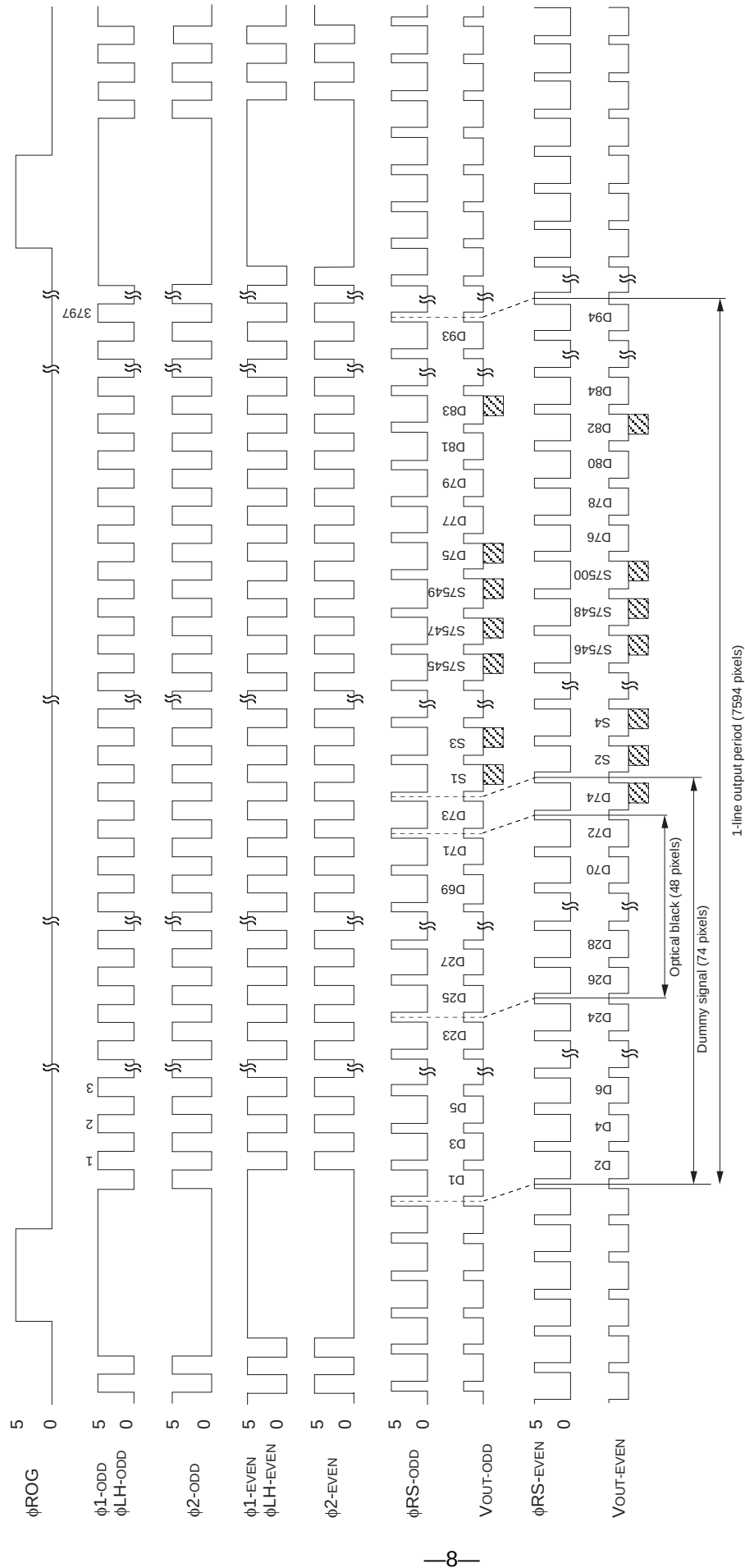
Cross point $\phi 1$ and $\phi 2$



Cross point ϕLH and $\phi 2$



Clock Timing Chart 5 (alternate output)*



Note) The transfer pulses (ϕ 1, ϕ 2, ϕ LH) must have more than 3797 cycles.

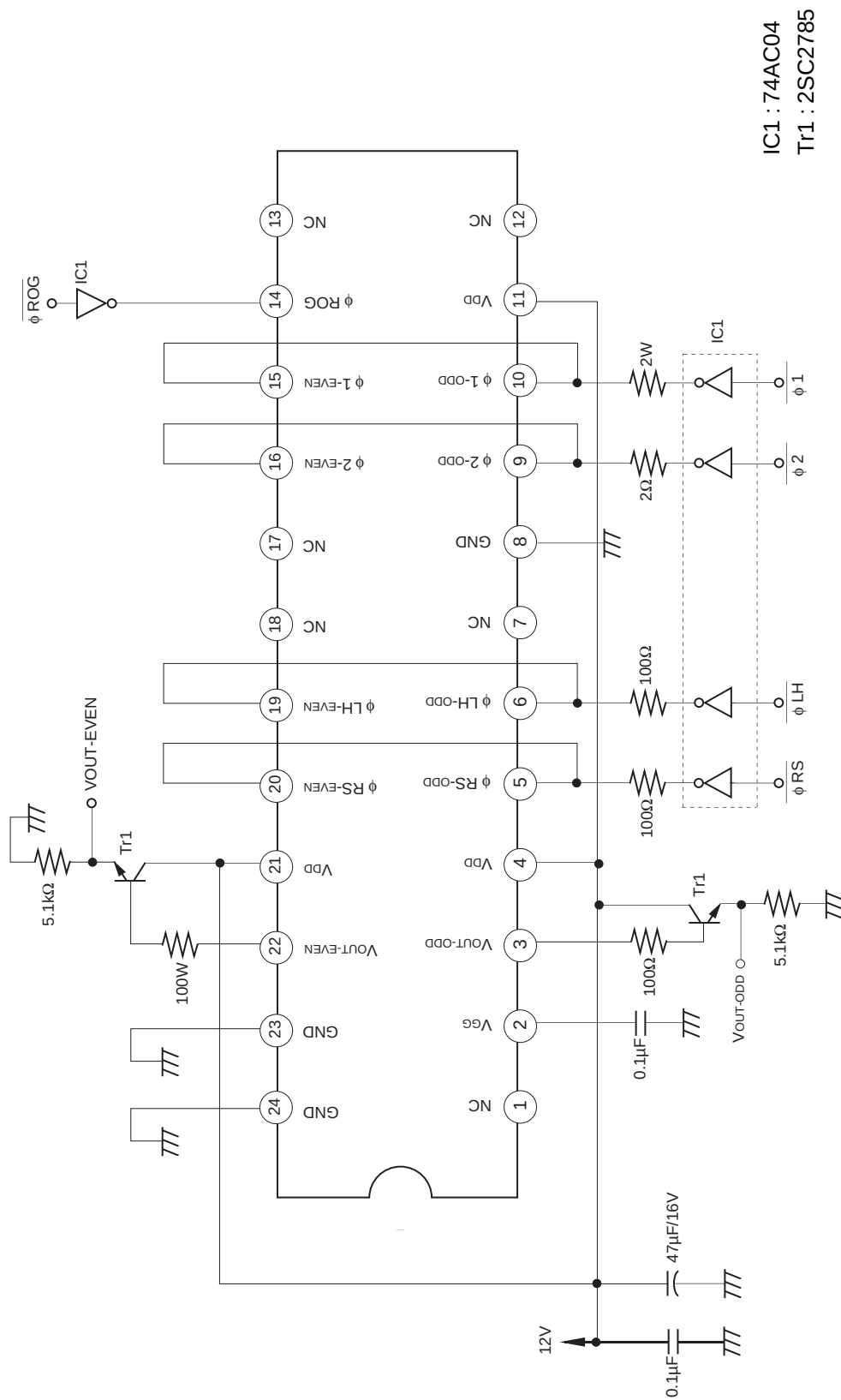
*Alternate output is available by making ϕ 1-EVEN, ϕ 2-EVEN, ϕ LH-EVEN, ϕ RS-EVEN delayed to ϕ 1-ODD, ϕ 2-ODD, ϕ LH-ODD, ϕ RS-ODD for half a cycle.

Clock Pulse Recommended Timing

	Symbol	Min.	Typ.	Max.	Unit
ϕ ROG, ϕ 1 pulse timing	t1	50	100	—	ns
ϕ ROG pulse high level period	t2	1000	1500	—	ns
ϕ ROG, ϕ 1 pulse timing	t3	1000	1500	—	ns
ϕ ROG pulse rise time	t4	0	5	10	ns
ϕ ROG pulse fall time	t5	0	5	10	ns
ϕ 1 pulse rise time / ϕ 2 pulse fall time	t6	0	20	60	ns
ϕ 1 pulse fall time / ϕ 2 pulse rise time	t7	0	20	60	ns
ϕ RS pulse high level period	t8	20	250*	—	ns
ϕ RS, ϕ LH pulse timing	t9	0	250*	—	ns
ϕ RS pulse rise time	t10	0	10	30	ns
ϕ RS pulse fall time	t11	0	10	30	ns
Signal output delay time	t12	—	8	—	ns
	t13	—	8	—	ns
ϕ 1, ϕ LH pulse low level period/ ϕ 2 pulse high level period	t14, t16	25	500*	—	ns
ϕ 1, ϕ LH pulse high level period/ ϕ 2 pulse low level period	t15, t17	25	500*	—	ns

(*) These timing is the recommended condition under $f_{\phi 1}=1$ MHz.

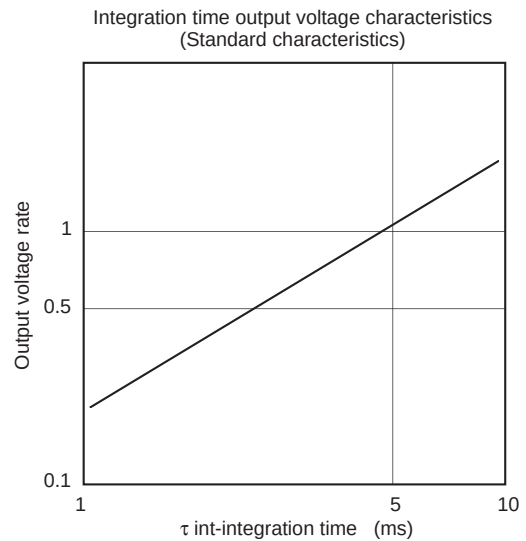
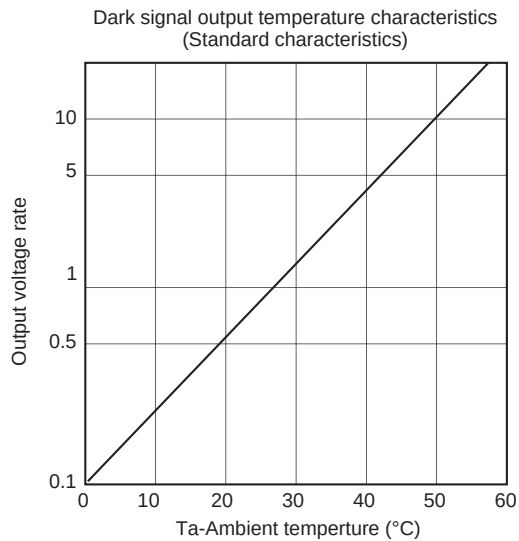
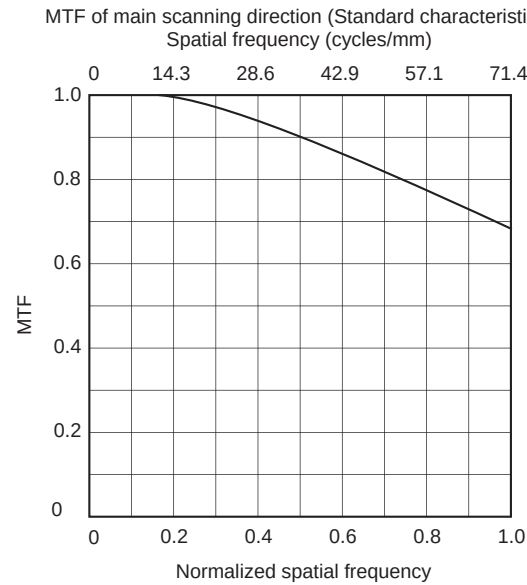
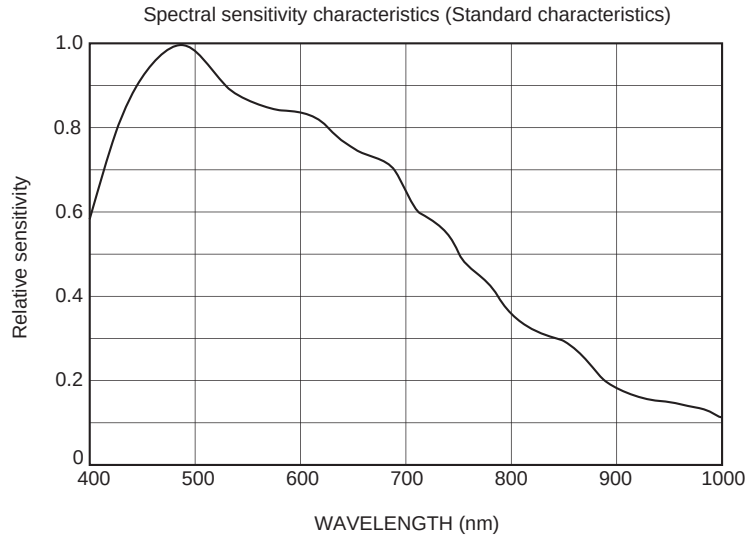
Application Circuit* (Simultaneous output)



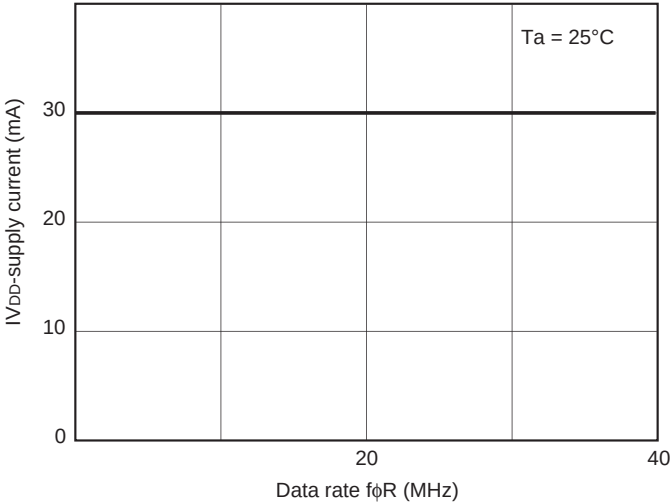
*Data rate $f_R = 2 \text{ MHz}$

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

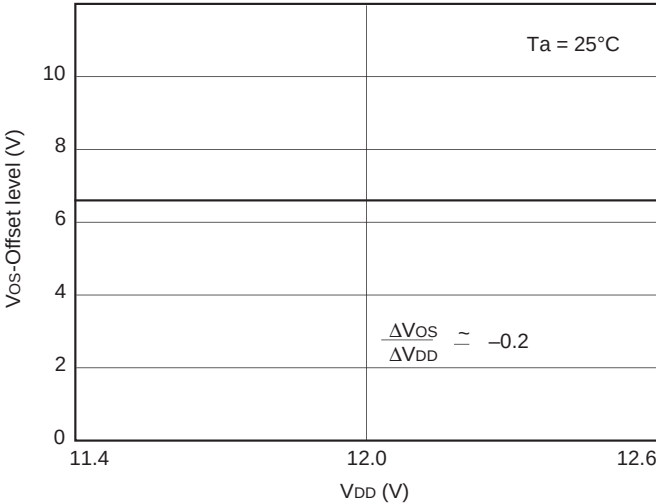
Example of Representative Characteristics



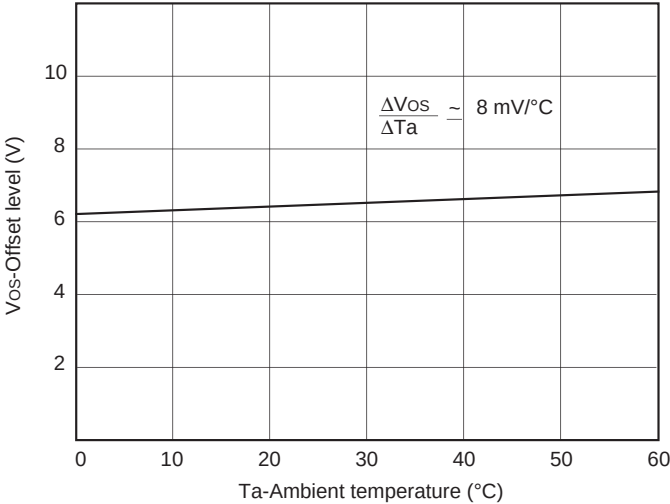
Operational frequency response of supply current
(Standard characteristics)



Offset level vs. V_{DD} characteristics
(Standard characteristics)



Offset level vs. Temperature characteristics
(Standard characteristics)



Notes of Handling

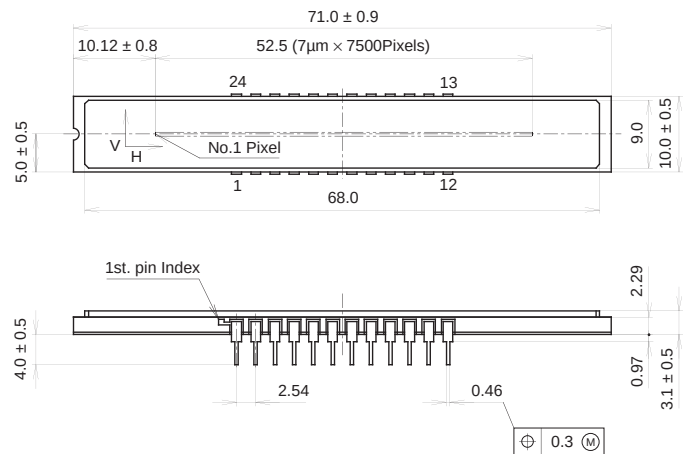
- 1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.

 - a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
 - b) When handling directly use an earth band.
 - c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
 - d) Ionized air is recommended for discharge when handling CCD image sensor.
 - e) For the shipment of mounted substrates, use boxes treated for prevention of static charges.
- 2) Soldering
 - a) Make sure the package temperature does not exceed 80 °C.
 - b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30 W soldering iron and solder each pin in less then 2 seconds. For repairs and remount, cool sufficiently.
 - c) To dismount an imaging device, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.
- 3) Dust and dirt protection
 - a) Operate in clean environments.
 - b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
 - c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
 - d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
- 4) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
- 5) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

Package Outline Unit : mm

24Pin DIP (400mil)



PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.8g