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Winbond Electronics Corp.

166MHZ CLOCK FOR SIS CHIPSET

W83194BR-640

Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
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LIFE SUPPORT APPLICATIONS

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Publication Release Date: April. 2001
Revision 1.0

1. GENERAL DESCRIPTION

The W83194BR-640 is a Clock Synthesizer for SiS 640 chipset. W83194BR-640 provides all clocks required for high-speed RISC or CISC microprocessor such as Intel Pentium II, Pentium III and Celeron, and also provides 16 different frequencies of CPU clocks frequency setting. All clocks are externally selectable with smooth transitions. The W83194BR-640 makes SDRAM in synchronous or asynchronous frequency with CPU clocks.

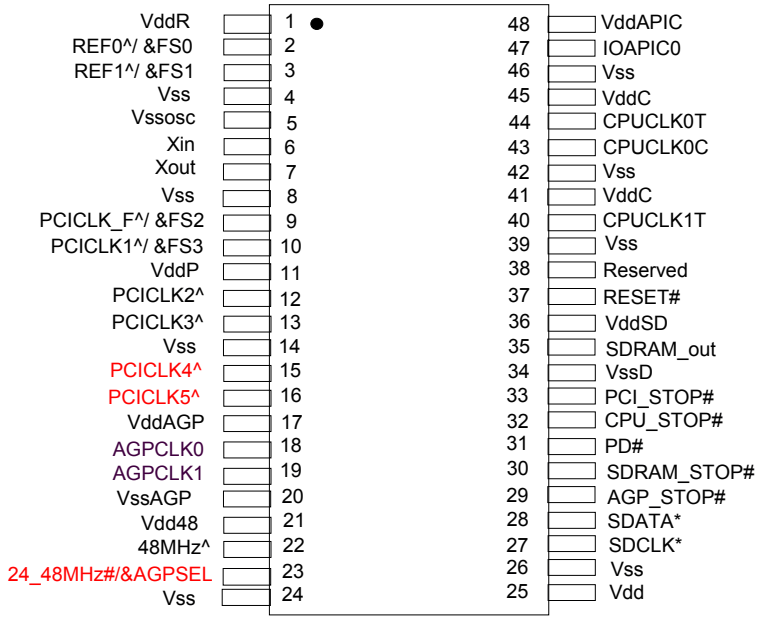
The W83194BR-640 provides step-less frequency programming by controlling the VCO freq. and the programmable AGP, PCI clock output divisor ratio. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal. Spread spectrum built in at ±0.5% or ±0.25% to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I^2C interface

The W83194BR-640 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

2. PRODUCT FEATURES

- Supports Intel Slot 1 and Socket 370 CPUs with I^2C.
- 2 CPU clocks
- 2 AGP clocks
- 1 SDRAM output clock for chipset
- 1 IOAPIC clock
- 6 PCI synchronous clocks.
- Optional single or mixed supply:
  (Others Vdd = 3.3V, VddLCPU=2.5V)
- Skew --- CPU to CPU < 175ps, CPU to SDRAM < 250ps, PCI to PCI < 500ps, AGP to AGP < 175ps
- Smooth frequency switch with selections from 66 to 200mhz
- I^2C 2-Wire serial interface and I^2C read back
- 0.5%, 0.25%center type, 0~0.5% down type spread spectrum to reduce EMI
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- 48 MHz for USB
- 24 MHz for super I/O
- Packaged in 48-pin SSOP

3. PIN CONFIGURATION



4. PIN DESCRIPTION

IN - Input
OUT - Output
I/O - Bi-directional Pin
- Active Low
* - Internal 120kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	6	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	7	OUT	Crystal output at 14.318MHz nominally.

4.2 CPU, SDRAM, PCI Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
IOAPIC0	47	OUT	16.7/33MHz APIC clock for CPU and Chipset by I2C byte 7 bit 3
CPUCLK0T CPUCLK0C	44,43	OUT	True CPU clock output and Complementary CPU clock output. This pin will be stopped by CPU_STOP#
CPUCLK1T	40	OUT	Low skew (< 250ps) clock outputs for host CPU clock output for chipset and CPU, When byte 9 bit 6 = 0 This pin will not be stopped by CPU_STOP#
SDRAM_out	35	OUT	SDRAM clock output which have syn. or asyn. Frequencies as CPU clocks. The clock phase is the same as CPUCLK0T and CPUCLK1T.
PCICLK_F^/ &FS2	9	I/O	Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. Internal 120KΩ pull-down PCI free running clock during normal operation. PCI output has 1.5X drive strength.
PCICLK 1^/ &FS3	10	I/O	Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks. Internal 120KΩ pull-down PCI clock during normal operation. PCI output has 1.5X drive strength.
PCICLK ^[2:5]	12,13,15,16	OUT	Low skew (< 250ps) PCI clock outputs. PCI outputs have 1.5X drive strength.
RESET#	37	OD	Open Drain, 4ms low active pulse when Watch Dog time out, the all clock output recover to hardware FS0-FS3 setting.

4.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	28	I/O	Serial data of I²C 2-wire control interface
*SDCLK	27	IN	Serial clock of I²C 2-wire control interface

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0^/&FS0	2	I/O	3.3V, 14.318MHz reference clock output. Internal 120kΩ pull-down.This pin has 1.5X drive strength. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and

			PCI clocks.
REF1^/&FS1	3	I/O	3.3V, 14.318MHz reference clock output. Internal 120kΩ pull-down.This pin has 1.5X drive strength. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
24_48MHz#/ &AGPSEL	23	I/O	24MHz or 48MHz selected by Register. AGPSEL at initial power up for H/W selecting the output frequency of AGP clocks. Internal 120KΩ pull-down.
48MHz ^	22	O	48MHz output for USB. This pin has 1.5X drive strength.

4.5 Power Management Pins

SYMBOL	PIN	FUNCTION
AGP_STOP#	29	AGP clock stop control pin.
SDRAM_STOP#	30	SDRAM clock stop control pin.
PD#	31	Power Down pin, if PD#=0, all clocks are stopped.
CPU_STOP#	32	CPU clock stop control pin.
PCI_STOP#	33	PCI clock stop control pin.

4.6 Power Pins

SYMBOL	PIN	FUNCTION
VddR	1	Power supply for REF. 3.3V
VddAPIC	48	Power supply for IOAPIC0, 2.5V.
Vdd	25	Power supply for core logic. 3.3V
VddC	41,45	Power supply for CPUCLK1T and CPUCLK0T, CPUCLK1T, IOAPIC0, 2.5V.
VddAGP	17	Power supply for AGP outputs.
VddP	11	Power supply for PCI outputs.
VddSD	36	Power supply for SDRAM and 48/24MHz outputs.
Vdd48	21	Power supply for 48/24MHz outputs.
Vss	4,5,8,14,20,26,46,39,42	Circuit Ground.

5. FREQUENCY SELECTION BY HARDWARE

				VCO	CPU	SDRAM	PCI	AGP0	AGP1	CPU	SDRAM	PCI	AGPSEL =0	AGPSEL =1
FS3	FS2	FS1	FS0	(MHz)	ratio	ratio	ratio	ratio	ratio	(MHz)	(MHz)	(MHz)	(MHz)	(MHz)
0	0	0	0	399.6	6	6	2	6	8	66.6	66.6	33.3	66.6	50
0	0	0	1	400	4	4	3	6	8	100	100	33.3	66.6	50
0	0	1	0	498	3	3	5	8	10	166	166	33.2	62.5	50
0	0	1	1	399	3	3	4	6	8	133	133	33.3	66.6	50
0	1	0	0	399.6	6	4	2	6	8	66.6	100	33.3	66.6	50
0	1	0	1	400	4	6	3	6	8	100	66.6	33.3	66.6	50
0	1	1	0	400	4	3	3	6	8	100	133	33.3	66.6	50
0	1	1	1	399	3	4	4	6	8	133	100	33.3	66.6	50
1	**0**	**0**	**0**	**336**	**3**	**3**	**3**	**5**	**6**	**112**	**112**	**37.3**	**67.2**	**56**
1	0	0	1	372	3	3	4	6	8	124	124	31	62	46.5
1	0	1	0	414	3	3	4	6	8	138	138	34.5	69	51.8
1	0	1	1	300	2	2	5	5	6	150	150	30	60	50
1	1	0	0	399.6	6	3	2	6	8	66.6	133	33.3	66.6	50
1	1	0	1	498	4	3	4	8	10	124.5	166	31.13	62.5	50
1	1	1	0	300	2	3	5	5	6	150	100	30	60	50
1	1	1	1	480	3	4	5	8	10	160	120	32	60	48

6. FUNCTION DESCRIPTION

6.1 2-WIRE I^2C CONTROL INTERFACE

The clock generator is a slave I2C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83194BR-640 initializes with default register settings, and then it ptional to use the 2-wire control interface.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I^2C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I^2C controller :

Clock Address A(6:0) & R/W	Ack	8 bits dummy Command code	Ack	8 bits dummy Byte count	Ack	Byte0,1,2... until Stop

Set R/W to 1 when read back the data sequence is as follows, [1101 0011] :

Clock Address A(6:0) & R/W	Ack	Byte 0	Ack	Byte 1	Ack	Byte2, 3, 4... until Stop

6.2 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

6.2.1 Register 4: CPU Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (for frequency table selection by software via I^2C)
6	0	-	SSEL2 (for frequency table selection by software via I^2C)
5	0	-	SSEL1 (for frequency table selection by software via I^2C)
4	0	-	SSEL0 (for frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 1,2, 7:4
2	0	-	SSEL4 (for frequency table selection by software via I^2C)
1	0	-	SSEL5 (for frequency table selection by software via I^2C)
0	0	-	0 = Running 1 = Tri-state all outputs

Frequency table by I2C

SEL5	SEL4	SEL3	SEL2	SEL1	SEL0	VCO (MHz)	CPU ratio	SDRAM ratio	PCI ratio	AGP0 ratio	AGP1 ratio	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGP0 (MHz)	AGP1 (MHz)
0	0	0	0	0	0	399.6	6	6	2	6	8	66.6	66.6	33.3	66.6	50
0	0	0	0	0	1	400	4	4	3	6	8	100	100	33.3	66.6	50
0	0	0	0	1	0	498	3	3	5	8	10	166	166	33.2	62.5	50
0	0	0	0	1	1	399	3	3	4	6	8	133	133	33.3	66.6	50
0	0	0	1	0	0	399.6	6	4	2	6	8	66.6	100	33.3	66.6	50
0	0	0	1	0	1	400	4	6	3	6	8	100	66.6	33.3	66.6	50
0	0	0	1	1	0	400	4	3	3	6	8	100	133	33.3	66.6	50
0	0	0	1	1	1	399	3	4	4	6	8	133	100	33.3	66.6	50
0	**0**	**1**	**0**	**0**	**0**	**336**	**3**	**3**	**3**	**5**	**6**	**112**	**112**	**37.3**	**67.2**	**56**
0	0	1	0	0	1	372	3	3	4	6	8	124	124	31	62	46.5
0	0	1	0	1	0	414	3	3	4	6	8	138	138	34.5	69	51.8
0	0	1	0	1	1	300	2	2	5	5	6	150	150	30	60	50
0	0	1	1	0	0	399.6	6	3	2	6	8	66.6	133	33.3	66.6	50
0	0	1	1	0	1	498	4	3	4	8	10	124.5	166	31.13	62.5	50
0	0	1	1	1	0	300	2	3	5	5	6	150	100	30	60	50
0	0	1	1	1	1	480	3	4	5	8	10	160	120	32	60	48
0	1	0	0	0	0	420	6	4	2	6	8	70	105	35	70	52.5
0	1	0	0	0	1	432	6	4	2	6	8	72	108	36	72	54
0	1	0	0	1	0	333.2	4	3	3	6	8	83.3	111.07	27.77	55.53	41.65
0	1	0	0	1	1	388	4	3	3	6	8	97	129.33	32.33	64.67	48.5
0	1	0	1	0	0	408	4	3	3	6	8	102	136	34	68	51
0	1	0	1	0	1	416	4	3	3	6	8	104	138.67	34.67	69.33	52
0	1	0	1	1	0	420	4	3	3	6	8	105	140	35	70	52.5
0	1	0	1	1	1	428	4	3	3	6	8	107	142.67	35.67	71.33	53.5
0	1	1	0	0	0	412	4	6	3	6	8	103	68.67	34.33	68.67	51.5
0	1	1	0	0	1	420	4	6	3	6	8	105	70	35	70	52.5
0	1	1	0	1	0	424	4	4	3	6	8	106	106	35.33	70.67	53
0	1	1	0	1	1	428	4	4	3	6	8	107	107	35.67	71.33	53.5
0	1	1	1	0	0	412	4	4	3	6	8	103	103	34.33	68.67	51.5
0	1	1	1	0	1	420	4	4	3	6	8	105	105	35	70	52.5
0	1	1	1	1	0	424	4	4	3	6	8	106	106	35.33	70.67	53

0	1	1	1	1	1	432	4	4	3	6	8	108	108	36	72	54
SEL5	**SEL4**	**SEL3**	**SEL2**	**SEL1**	**SEL0**	**VCO (MHz)**	**CPU ratio**	**SDRAM ratio**	**PCI ratio**	**AGP0 ratio**	**AGP1 ratio**	**CPU (MHz)**	**SDRAM (MHz)**	**PCI (MHz)**	**AGP0 (MHz)**	**AGP1 (MHz)**
1	0	0	0	0	0	390	3	3	4	6	8	130	130	32.5	65	48.75
1	0	0	0	0	1	405	3	3	4	6	8	135	135	33.75	67.5	50.63
1	0	0	0	1	0	408	3	3	4	6	8	136	136	34	68	51
1	0	0	0	1	1	417	3	3	4	6	8	139	139	34.75	69.5	52.13
1	0	0	1	0	0	420	3	3	4	6	8	140	140	35	70	52.5
1	0	0	1	0	1	426	3	3	4	6	8	142	142	35.5	71	53.25
1	0	0	1	1	0	429	3	3	4	6	8	143	143	35.75	71.5	53.63
1	0	0	1	1	1	435	3	3	4	6	8	145	145	36.25	72.5	54.38
1	0	1	0	0	0	390	3	3	5	6	8	130	130	26	65	48.75
1	0	1	0	0	1	405	3	3	5	6	8	135	135	27	67.5	50.63
1	0	1	0	1	0	414	3	3	5	6	8	138	138	27.6	69	51.75
1	0	1	0	1	1	426	3	3	5	6	8	142	142	28.4	71	53.25
1	0	1	1	0	0	411	3	3	5	6	8	137	137	27.4	68.5	51.38
1	0	1	1	0	1	417	3	3	5	6	8	139	139	27.8	69.5	52.13
1	0	1	1	1	0	423	3	3	5	6	8	141	141	28.2	70.5	52.88
1	0	1	1	1	1	426	3	3	5	6	8	142	142	28.4	71	53.25
1	1	0	0	0	0	390	3	4	4	6	8	130	97.5	32.5	65	48.75
1	1	0	0	0	1	396	3	4	4	8	10	132	99	33	49.5	39.6
1	1	0	0	1	0	408	3	4	4	8	10	136	102	34	51	40.8
1	1	0	0	1	1	411	3	4	4	8	10	137	102.75	34.25	51.38	41.1
1	1	0	1	0	0	414	3	4	4	8	10	138	103.5	34.5	51.75	41.4
1	1	0	1	0	1	426	3	4	4	8	10	142	106.5	35.5	53.25	42.6
1	1	0	1	1	0	432	3	4	4	8	10	144	108	36	54	43.2
1	1	0	1	1	1	438	3	4	4	8	10	146	109.5	36.5	54.75	43.8
1	1	1	0	0	0	450	3	4	5	8	10	150	112.5	30	56.25	45
1	1	1	0	0	1	459	3	4	5	8	10	153	114.75	30.6	57.38	45.9
1	1	1	0	1	0	468	3	4	5	8	10	156	117	31.2	58.5	46.8
1	1	1	0	1	1	489	3	4	5	8	10	163	122.25	32.6	61.13	48.9
1	1	1	1	0	0	498	3	4	5	8	10	166	124.5	33.2	62.25	49.8
1	1	1	1	0	1	525	3	4	5	8	10	175	131.25	35	65.63	52.5
1	1	1	1	1	0	534	3	4	5	8	10	178	133.5	35.6	66.75	53.4
1	1	1	1	1	1	549	3	4	5	8	10	183	137.25	36.6	68.63	54.9

6.2.2 Register 5 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	0 = 0.5% down type spread 1= Center type spread.
5	0	-	0 = Normal 1 = Spread Spectrum enabled
4	0	-	0 = ±0.25% Center type Spread Spectrum Modulation 1 = ±0.5% Center type Spread Spectrum Modulation
3	1	43	CPUCLK0C (Active / Inactive)
2	1	44	CPUCLK0T (Active / Inactive)
1	1	40	CPUCLK1T (Active / Inactive)
0	1	-	Reserved

6.2.3 Register 6: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	19	AGPCLK1 (Active / Inactive)
6	1	18	AGPCLK0 (Active / Inactive)
5	1	16	PCICLK5 (Active / Inactive)
4	1	15	PCICLK4 (Active / Inactive)
3	1	13	PCICLK3 (Active / Inactive)
2	1	12	PCICLK2 (Active / Inactive)
1	1	10	PCICLK1 (Active / Inactive)
0	1	9	PCICLK_F (Active / Inactive)

6.2.4 Register 7: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	23	24_48MHz (Active / Inactive)
6	1	22	48MHz (Active / Inactive)
5	1	47	IOAPIC0 (Active/Inactive)
4	1	-	24/48 MHz Frequency Control 1=24MHz 0=48MHz
3	1	-	IOAPIC Frequency Control 1=PCI / 2, 0=PCI
2	1	-	Reserved
1	1	3	REF1 (Active / Inactive)
0	1	2	REF0 (Active / Inactive)

6.2.5 Register 8: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	X	23	Latched AGPSEL#
6	X	10	Latched FS3#
5	X	9	Latched FS2#
4	X	3	Latched FS1#
3	X	2	Latched FS0#
2	**1**	**-**	**ACskew2 (AGP to CPU skew program bit)**
1	**0**	**-**	**ACskew1 (AGP to CPU skew program bit)**
0	**0**	**-**	**ACskew0 (AGP to CPU skew program bit)**

6.2.6 Register 9: SDRAM Register(1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	CPUCLK1 Free-run Control 1=CPUCLK1 can stopped by CPU_STOP# , 0= CPUCLK1 Free-run
5	1	-	Reserved
4	X	-	Latched AGP_STOP#
3	X	-	Latched CPU_STOP#
2	X	-	Latched PCI_STOP#
1	X	-	Latched SDR_STOP#
0	X	-	Latched PD#

6.2.7 Register 10: Watchdog Timer Register

Bit	@PowerUp	Pin	Description
7	0	-	Enable Count 1 = start timer 0 = stop timer
6	X	-	Second timeout status (READ ONLY)
5	0	-	Second count 5
4	0	-	Second count 4
3	0	-	Second count 3
2	0	-	Second count 2
1	0	-	Second count 1
0	0	-	Second count 0

6.2.8 Register 11: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 8
6	1	-	Test 1 (Internal test use)
5	0	-	Test 0 (Internal test use)
4	0	-	M value bit 4
3	0	-	M value bit 3
2	0	-	M value bit 2
1	0	-	M value bit 1
0	0	-	M value bit 0

6.2.9 Register 12: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 7
6	0	-	N value bit 6
5	0	-	N value bit 5
4	0	-	N value bit 4
3	0	-	N value bit 3
2	0	-	N value bit 2
1	0	-	N value bit 1
0	0	-	N value bit 0

6.2.10 Register 13: Spread Specturn Range Control Register

Bit	@PowerUp	Pin	Description
7	0	-	Spread spectrum up count 3
6	0	-	Spread spectrum up count 2
5	0	-	Spread spectrum up count 1
4	0	-	Spread spectrum up count 0
3	0	-	Spread spectrum down count 3
2	0	-	Spread spectrum down count 2
1	0	-	Spread spectrum down count 1
0	0	-	Spread spectrum down count 0

6.2.11 Register 14: Divisor Register

Bit	@PowerUp	Pin	Description
7	0	-	0: use frequency table 1: use M/N register to program frequency The equation is **VCO freq. = 14.318MHz * (N+4)/ M**
6	0	-	Ratio SEL3 (See ratio selection table)
5	0	-	Ratio SEL2 (See ratio selection table)
4	0	-	Ratio SEL1 (See ratio selection table)
3	0	-	Ratio SEL0 (See ratio selection table)
2	0	-	Reserve
1	0	-	Reserve
0	0	-	Reserve

6.2.12 Register 15: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	**0**	**-**	**Winbond Chip ID**
6	**1**	**-**	**Winbond Chip ID**
5	**1**	**-**	**Winbond Chip ID**
4	**0**	**-**	**Winbond Chip ID**
3	**0**	**-**	**Winbond Chip ID**
2	**0**	**-**	**Winbond Chip ID**
1	**1**	**-**	**Winbond Chip ID**
0	**0**	**-**	**Winbond Chip ID**

6.2.13 Register 16: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	**1**	**-**	**Winbond Chip ID**
6	**0**	**-**	**Winbond Chip ID**
5	**1**	**-**	**Winbond Chip ID**
4	**0**	**-**	**Winbond Chip ID**
3	**0**	**-**	**Version ID**
2	**0**	**-**	**Version ID**
1	**0**	**-**	**Version ID**
0	**1**	**-**	**Version ID**

RATIO SELECTION TABLE

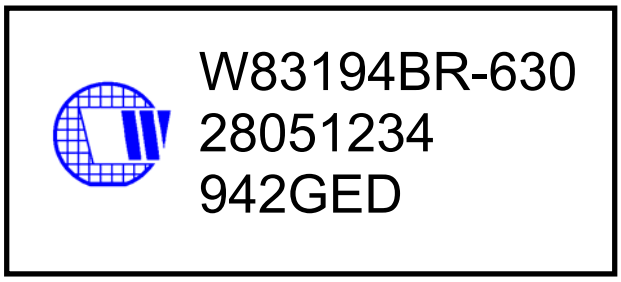
Reg10 bit6	Reg10 Bit5	Reg10 bit4	Reg10 bit3	VCO/ CPU	VCO/ SDRAM	VCO/ PCI
SSEL3	SSEL2	SSEL1	SSEL0	ratio	ratio	ratio
0	0	0	0	2	2	5
0	0	0	1	2	3	5
0	0	1	0	3	3	3
0	0	1	1	3	3	4
0	1	0	0	3	3	5
0	1	0	1	3	4	4
0	1	1	0	3	4	5
0	1	1	1	4	3	3
1	0	0	0	4	3	4
1	0	0	1	4	4	3
1	0	1	0	4	6	3
1	0	1	1	6	3	2
1	1	0	0	6	4	2
1	1	0	1	6	6	2
1	1	1	0	6	6	3
1	1	1	1	6	6	4

Reg10 bit2	Reg10 bit1	Reg10 bit0	VCO/AGP
AGP2	AGP1	AGP0	ratio
0	0	0	3
0	0	1	5
0	1	0	6
0	1	1	8
1	0	0	4
1	0	1	-
1	1	0	-
1	1	1	10

7. ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-640	48 PIN SSOP	Commercial, 0°C to +70°C

8. HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-640

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 942 G E D

942: packages made in '99, week 42

G: assembly house ID; O means OSE, G means GR

E: Internal use code

D: IC revision

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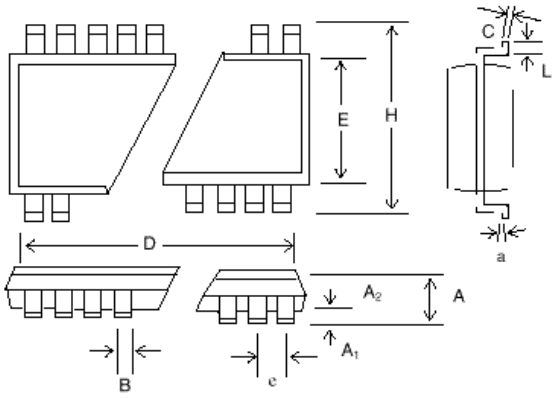
9. PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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