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FAIRCHILD SEMICONDUCTOR™

March 1997
Revised March 1999

74VHCT240A
Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHCT240A is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHCT240A is an inverting 3-STATE buffer having two active-LOW output enables. This device is designed to be used as 3-STATE memory address drivers, clock drivers, and bus oriented transmitter/receivers.

Protection circuits ensure that 0V to 7V can be applied to the input and output (Note 1) pins without regard to the supply voltage. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

Note 1: Outputs in OFF-State

Features

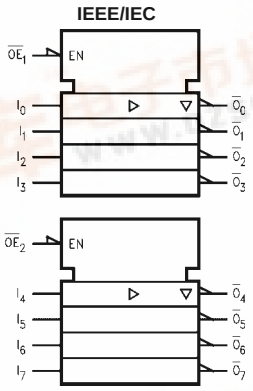
- High Speed: t_{PD} = 5.6 ns (typ) at V_{CC} = 5V
- Power down protection is provided on inputs and outputs
- Low power dissipation: I_{CC} = 4 µA (max) @ T_A = 25°C
- Pin and function compatible with 74HCT240

Ordering Code:

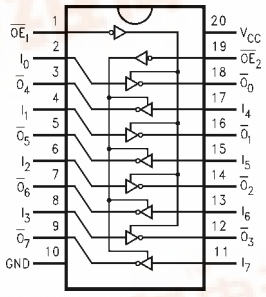
Order Number	Package Number	Package Description
74VHCT240AM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74VHCT240ASJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT240AMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT240AN	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs 3-STATE Outputs

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Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

H - HIGH Voltage Level
L - LOW Voltage Level
X - Immaterial
Z - High Impedance

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	
(Note 3)	−0.5V to V_{CC} + 0.5V
(Note 4)	−0.5V to +7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK}) (Note 5)	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±75 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 6)

Supply Voltage (V_{CC})	4.5V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	
(Note 3)	0V to V_{CC}
(Note 4)	0V to +5.5V
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 5.0V ± 0.5V	0 ns/V ~ 20 ns/V

Note 2: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 3: HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.

Note 4: When outputs are in OFF-State or when V_{CC} = OV.

Note 5: V_{OUT} < GND, V_{OUT} > V_{CC} (Outputs Active).

Note 6: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	4.5	2.0			2.0		V		
		5.5	2.0			2.0				
V_{IL}	LOW Level Input Voltage	4.5			0.8		0.8	V		
		5.5			0.8		0.8			
V_{OH}	HIGH Level Output Voltage	4.5	4.40	4.50		4.40		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 µA
			3.94			3.80		V		I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	4.5		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 µA
					0.36		0.44	V		I_{OL} = 8 mA
I_{OZ}	3-STATE Output Off-State Current	5.5			±0.25		±2.5	µA	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND	
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	µA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			4.0		40.0	µA	V_{IN} = V_{CC} or GND	
I_{CCT}	Maximum I_{CC}/Input	5.5			1.35		1.50	mA	V_{IN} = 3.4V Other Input = V_{CC} or GND	
I_{OFF}	Output Leakage Current (Power Down State)	0.0			0.5		5.0	µA	V_{OUT} = 5.5V	

Noise Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C		Units	Conditions
			Typ	Limits		
V_{OLP} (Note 7)	Quiet Output Maximum Dynamic V_{OL}	5.0	0.9	1.1	V	C_L = 50 pF
V_{OLV} (Note 7)	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.9	−1.1	V	C_L = 50 pF
V_{IHD} (Note 7)	Minimum HIGH Level Dynamic Input Voltage	5.0		2.0	V	C_L = 50 pF
V_{ILD} (Note 7)	Maximum LOW Level Dynamic Input Voltage	5.0		0.8	V	C_L = 50 pF

Note 7: Parameter guaranteed by design.

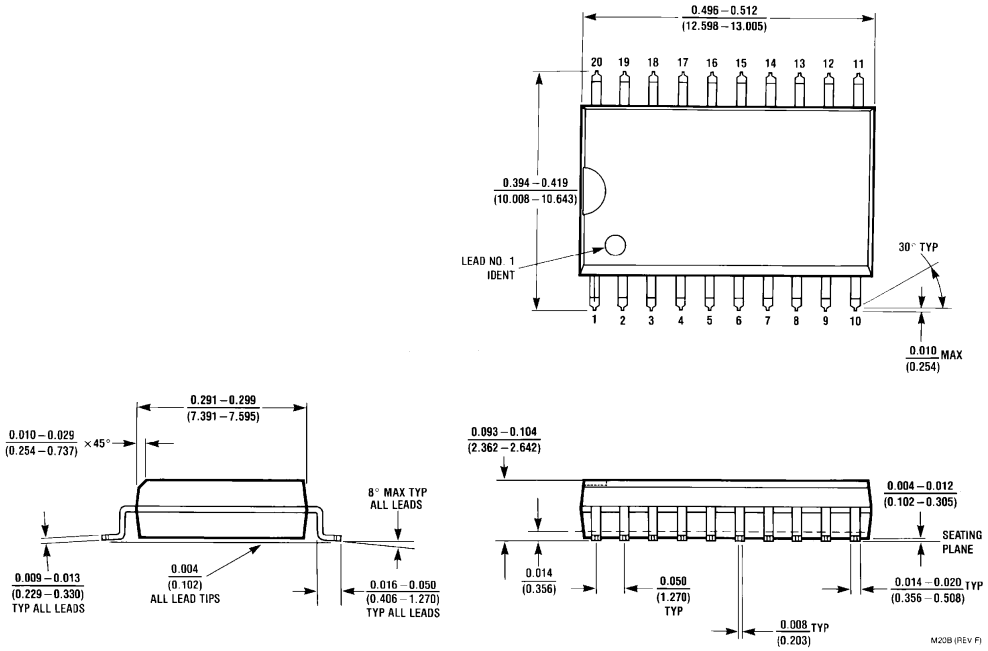
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	
			Min	Typ	Max	Min	Max			
t_{PLH}	Propagation Delay	5.0 ± 0.5		5.6	7.8	1.0	9.0	ns		$C_L = 15$ pF
t_{PHL}	Time			6.1	8.8	1.0	10.0			$C_L = 50$ pF
t_{PZL}	3-STATE Output	5.0 ± 0.5		6.5	10.4	1.0	12.5	ns	$R_L = 1$ kΩ	$C_L = 15$ pF
t_{PZH}	Enable Time			7.3	11.4	1.0	13.5			$C_L = 50$ pF
t_{PLZ}	3-STATE Output	5.0 ± 0.5		7.0	11.4	1.0	13.0	ns	$R_L = 1$ kΩ	$C_L = 50$ pF
t_{PHZ}	Disable Time									
t_{OSLH}	Output to	5.0 ± 0.5			1.0		1.0	ns	(Note 8)	
t_{OSHL}	Output Skew									
C_{IN}	Input			4	10		10	pF	V_{CC} = Open	
	Capacitance									
C_{OUT}	Output			9				pF	$V_{CC} = 5.0$V	
	Capacitance									
C_{PD}	Power Dissipation			19				pF	(Note 9)	
	Capacitance									

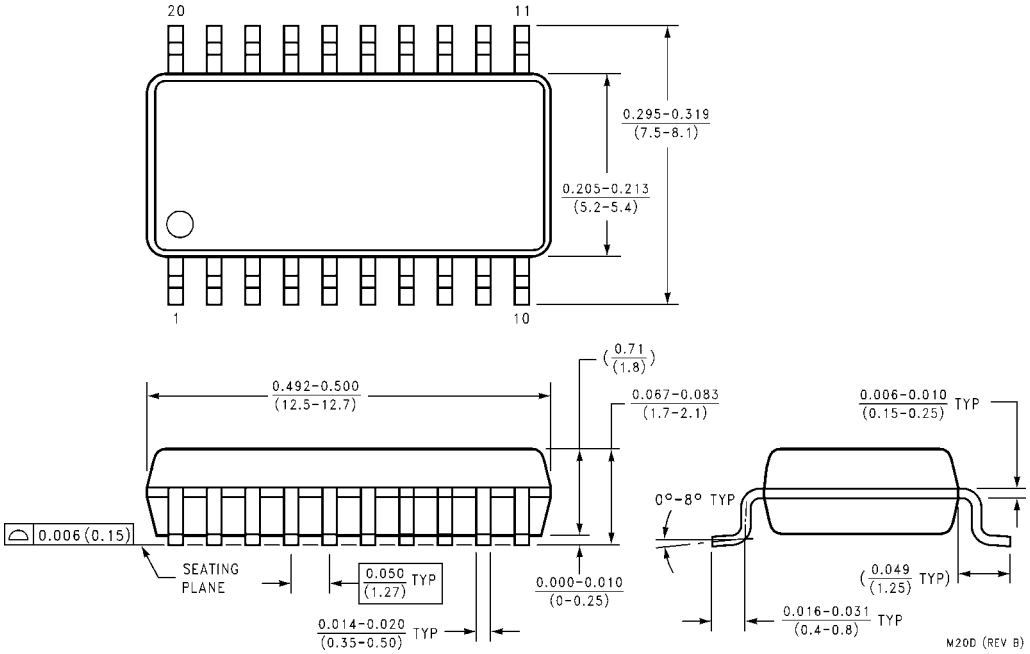
Note 8: Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$

Note 9: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/8$ (per F/F). The total C_{PD} when n pcs. of the Octal D Flip-Flop operates can be calculated by the equation: C_{PD} (total) = 20 + 12n.

Physical Dimensions inches (millimeters) unless otherwise noted

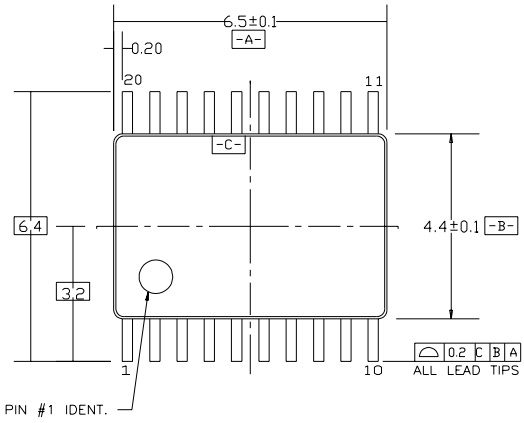


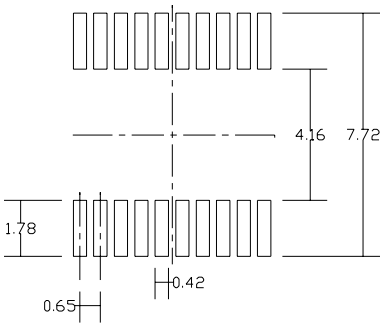
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B



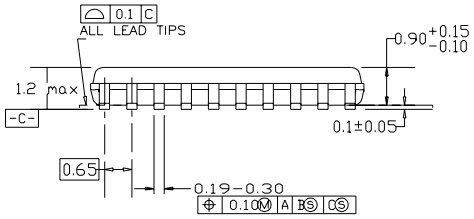
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

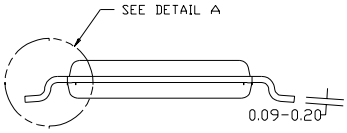
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



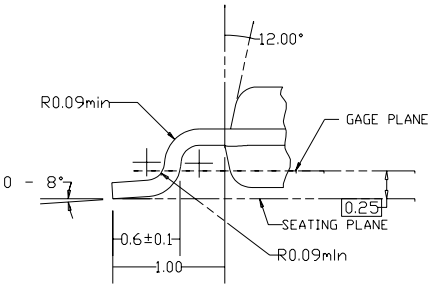


LAND PATTERN RECOMMENDATION





DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

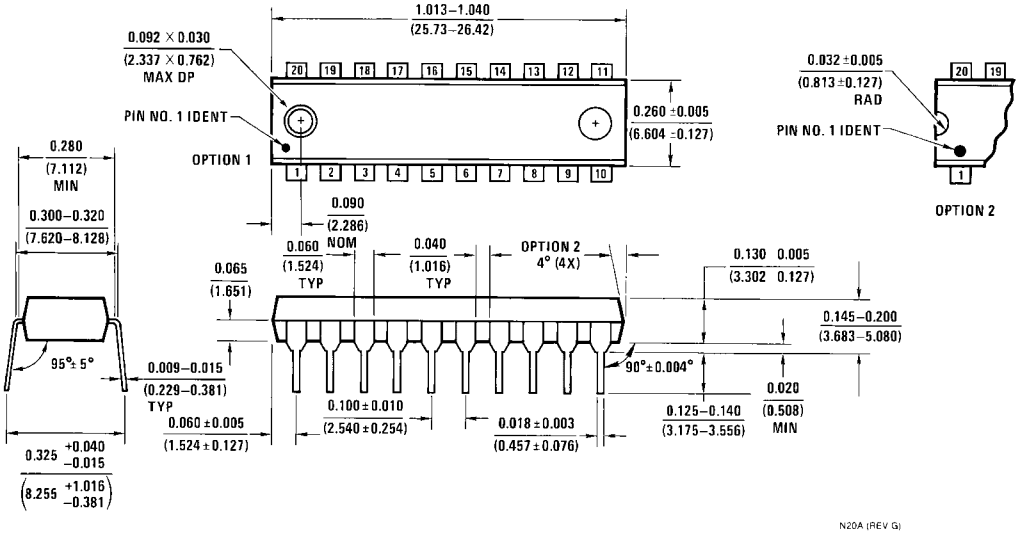
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A

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